



32-Channel Sample/Hold Amplifier with Output Clamping Diodes

MAX5167

General Description

The MAX5167 contains 32 sample-and-hold amplifiers driven by a single multiplexed input. The control logic addressing the outputs is a simple 5-wire input to the multiplexer. Additional logic allows two devices to function as a single 64-channel unit. Clamping diodes on each output allows clamping between two external reference voltages. The MAX5167 is available with an output impedance of 50Ω, 500Ω, or 1kΩ.

The MAX5167 operates with +10V and -5V supplies, and a separate +5V digital logic supply. Manufactured with a proprietary BiCMOS process, it provides high accuracy, fast acquisition time, low droop rate, and a low hold step. The MAX5167 has a typical linearity error of less than 0.01% and can accurately acquire an 8V step input signal to 0.01% accuracy in 2.5μs within the +7V to -4V input signal range. Transitions from sample mode to hold mode result in only a 0.5mV error. While in hold mode, the output voltage slowly droops at a rate of 1mV/s.

The MAX5167 is available in a 48-pin TQFP package and is specified for both the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges.

Applications

- Automatic Test Systems (ATE)
- Industrial Process Controls
- Arbitrary Function Generators
- Avionics Equipment

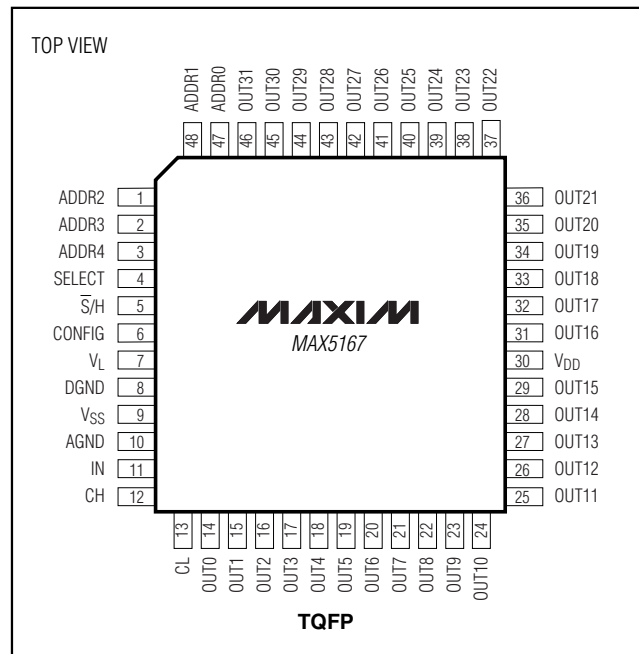
Features

- ◆ 32-Channel Sample/Hold
- ◆ Output Clamps on Each Channel
- ◆ 0.01% Accuracy of Acquired Signal
- ◆ 0.01% Linearity Error
- ◆ Fast Acquisition Time: 2.5μs
- ◆ Low Droop Rate: 1mV/s
- ◆ Low Hold Step: 0.25mV
- ◆ Wide Output Voltage Range: +7V to -4V

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	R _{OUT} (Ω)
MAX5167LCCM	0°C to +70°C	48 TQFP	50
MAX5167MCCM	0°C to +70°C	48 TQFP	500
MAX5167NCCM	0°C to +70°C	48 TQFP	1k
MAX5167LECM	-40°C to +85°C	48 TQFP	50
MAX5167MECM	-40°C to +85°C	48 TQFP	500
MAX5167NECM	-40°C to +85°C	48 TQFP	1k

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND	-0.3V to +11.0V	Maximum Current into Out ₋	± 10mA
V _{SS} to AGND	-6.0V to +0.3V	Maximum Current into Logic Inputs	± 20mA
V _{DD} to V _{SS}	+15.75V	Continuous Power Dissipation (T _A = +70°C)	
V _L to DGND	-0.3V to +6.0V	48-Pin TQFP (derate 12.5mW/°C above +70°C)	1000mW
V _L to AGND	-0.3V to +6.0V	Operating Temperature Ranges	
DGND to AGND	-0.3V to +2.0V	MAX5167_CCM	0°C to +70°C
IN, OUT ₋	V _{SS} to V _{DD}	MAX5167_ECM	-40°C to +85°C
Logic Inputs to DGND	-0.3V to +6.0V	Storage Temperature Range	-65°C to +150°C
CH, C _L to AGND	-6.0V to +11.0V	Lead Temperature (soldering, 10s)	+300°C
Maximum Current into C _L and C _H	± 80mA		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10.0V, V_{SS} = -5.0V, V_L = +5.0V ±5%, AGND = DGND = 0, R_L = 5kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SECTION							
Linearity Error		-4.0V < V _{IN} < +7V R _L = ∞			0.01	0.08	%
Hold Step	V _{HS}	IN = AGND			0.25	1.00	mV
Droop Rate		IN = AGND	T _A = +25°C		1	40	mV/s
Offset Voltage	V _{OS}	IN = AGND	T _A = +25°C	-30	-5	+30	mV
		+15°C ≤ T _A ≤ +65°C (Note 1)			20	40	μV/°C
Output Voltage Range	V _{OUT₋}	R _L = ∞		V _{SS} + 0.75		V _{DD} - 2.4	V
Analog Crosstalk		8V step with 500ns rising edge (Note 1)	C _L = 250pF for MAX5167L	-72	-76		dB
			C _L = 10nF for MAX5167M/67N	-72	-76		
Input Capacitance	C _{IN}	(Note 1)			10	20	pF
DC Output Impedance	R _{OUT₋}	R _L = ∞, C _L = 250pF	MAX5167L	35	50	65	Ω
			MAX5167M	350	500	650	
			MAX5167N	700	1000	1300	
Output Source Current	I _{SOURCE}	V _{IN} = 0, sample mode		2			mA
Output Sink Current	I _{SINK}	V _{IN} = 0, sample mode		2			mA
Output Clamp High	V _{CH}			V _{SS}		V _{DD}	V
Output Clamp Low	V _{CL}			V _{SS}		V _{DD}	V
TIMING PERFORMANCE							
Acquisition Time	t _{AQ}	8V step to 0.08%, R _L = ∞, Figure 2	T _A = +25°C		2.5	4	μs
		100mV step to ±1mV, R _L = ∞, Figure 2	T _A = +25°C		1		
Hold Mode Settling Time	t _H	To ±1mV of final value Figure 2 (Note1)			1	2	μs
Aperture Delay	t _{AP}	Figure 2 (Note1)				200	ns

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +10.0V$, $V_{SS} = -5.0V$, $V_L = +5.0V \pm 5\%$, $AGND = DGND = 0$, $R_L = 5k\Omega$, $C_L = 50pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
\overline{S}/H Pulse Width	t_{PW}	Figure 2 (Note1)	200			ns
Data Setup Time	t_{DS}	Figure 2 (Note1)	50			ns
Data Hold Time	t_{DH}	Figure 2 (Note1)	150			ns
DIGITAL INPUTS						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_I	$IN = DGND$ or V_{CC}	-1		+1	μA
POWER SUPPLIES						
Positive Analog Supply	V_{DD}	(Note 2)	9.5	10	10.5	V
Negative Analog Supply	V_{SS}	(Note 2)	-4.75	-5	-5.45	V
Digital Logic Supply	V_L		4.75	5	5.25	V
Positive Analog Supply Current	I_{DD}	$R_L = \infty$			36	mA
Negative Analog Supply Current	I_{SS}	$R_L = \infty$			36	mA
Digital Logic Supply Current	I_L	$ADDR_ = DGND$ or V_L , $\overline{S}/H = DGND$ or V_L			0.5	mA
		$ADDR_ = +0.8V$ or $+2.0V$, $\overline{S}/H = +0.8V$ or $+2.0V$			5	mA
Power-Supply Rejection Ratio	PSRR	For V_{DD} and V_{SS} , sample mode, $IN = AGND$	-60	-75		dB

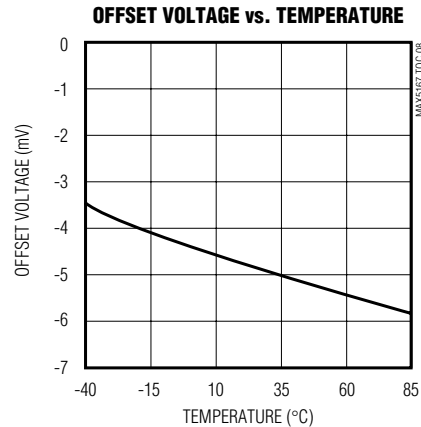
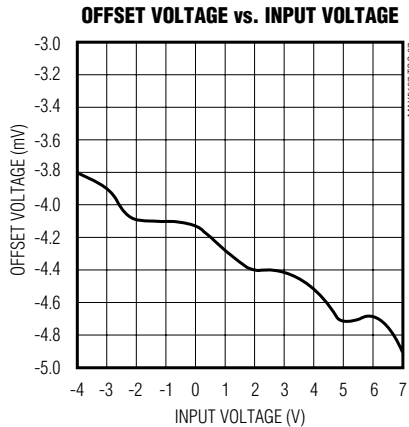
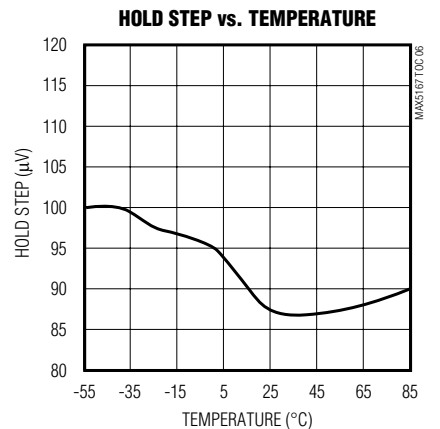
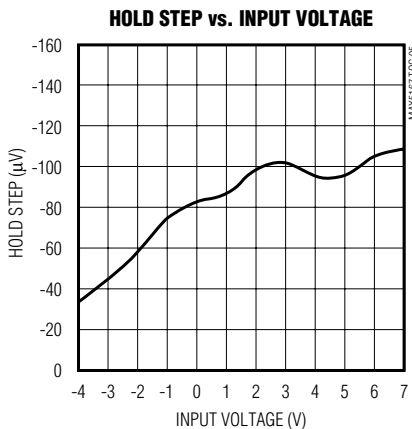
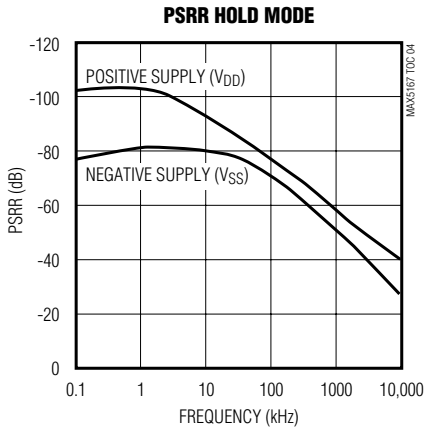
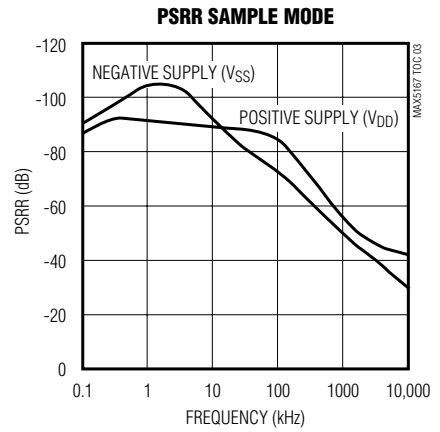
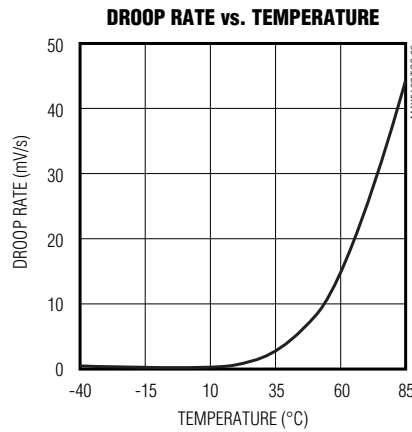
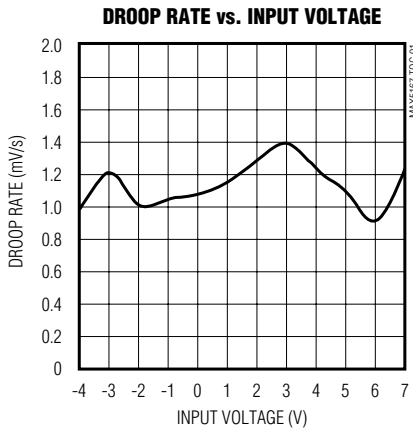
Note 1: Guaranteed by design.

Note 2: Do not exceed the absolute maximum rating for V_{DD} to V_{SS} of +15.75V (see *Absolute Maximum Ratings*).

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Typical Operating Characteristics

($V_{DD} = +10V$, $V_{SS} = -5V$, $V_L = +5V$, $V_{IN} = +5V$, $R_L = \infty$, $C_L = 0$, $AGND = DGND = 0$, $V_{CH} = V_{DD}$, $V_{CL} = V_{SS}$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

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PIN	NAME	FUNCTION
1	ADDR2	Bit 2 of the Address Decoder
2	ADDR3	Bit 3 of the Address Decoder
3	ADDR4	Bit 4 of the Address Decoder
4	SELECT	Enables the \overline{S}/H pin. The polarity of SELECT is determined by the state of the CONFIG pin. If CONFIG is low, then SELECT is active-high. If CONFIG is high, then SELECT is active-low. When SELECT is not in its active state, all 32 channels are in hold mode independent of the \overline{S}/H pin.
5	\overline{S}/H	Puts the selected channel into sample mode when low. Places all channels into hold mode when high.
6	CONFIG	Sets the polarity of the SELECT pin.
7	V _L	+5V Logic Supply
8	DGND	Digital GND
9	V _{SS}	-5V Analog Supply
10	AGND	Analog GND
11	IN	Input Pin
12	CH	Clamp High Pin
13	CL	Clamp Low Pin
14–29	OUT0–OUT15	Output 0–15 Pin
30	V _{DD}	+10V Analog Supply
31–46	OUT16–OUT31	Output 16–31 Pin
47	ADDR0	Bit 0 of the Address Decoder
48	ADDR1	Bit 1 of the Address Decoder

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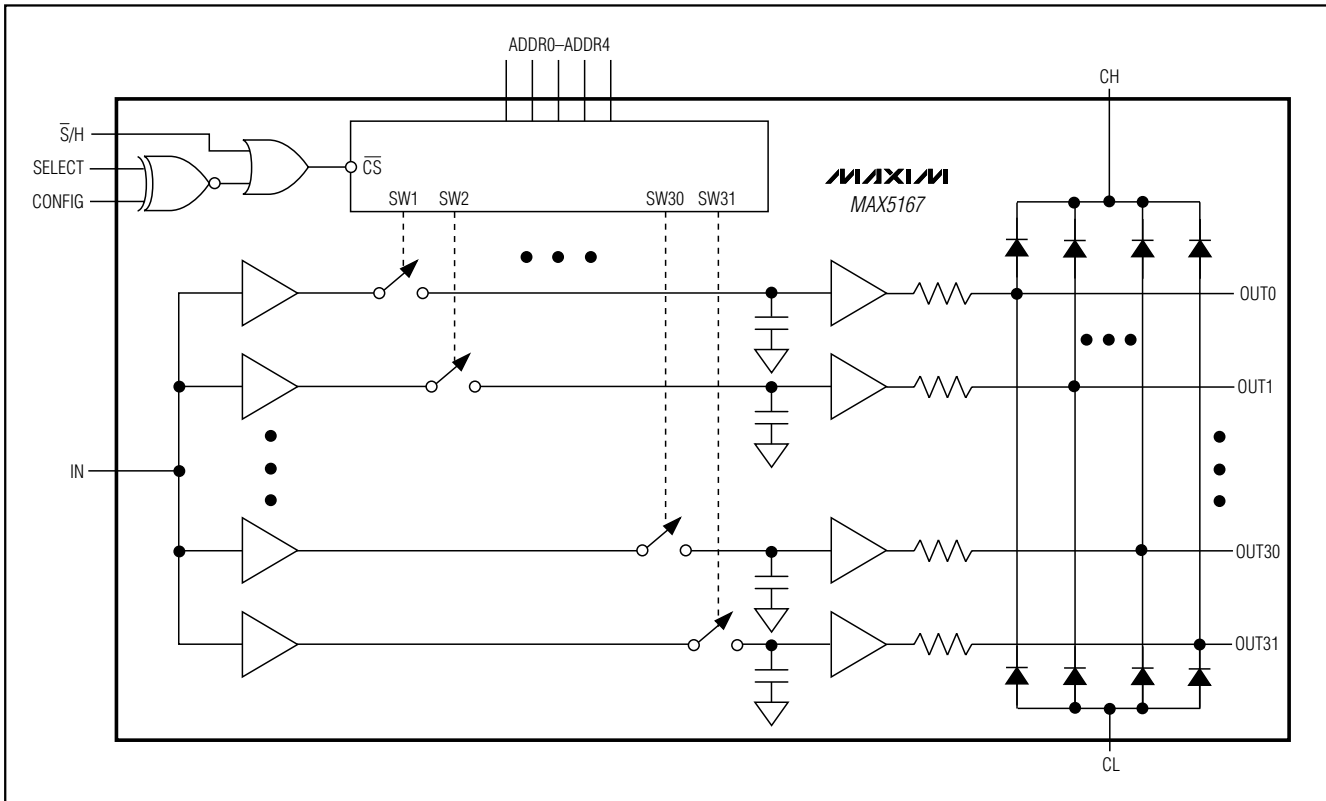


Figure 1. Functional Diagram

Detailed Description

Digital Interface

The MAX5167 has three logic control inputs and five address lines. The address lines are inputs to a demultiplexer that selects one of the 32 outputs in a standard addressing scheme (Table 1). The analog input is connected to the addressed sample/hold when directed by the control logic (Table 2).

The three logic control lines determine the state of the addressed sample/hold. The normal circuit connection for this device is to hardwire CONFIG and SELECT to opposing logic voltages. When SELECT and CONFIG are in opposite states (one high and the other low), the five address lines select one of the sample/holds. Use the $\overline{S/H}$ line to place the selected channel into sample or hold mode. The other 31 channels will remain in hold mode.

If an active-high sampling mode is desired, tie $\overline{S/H}$ and CONFIG low. In this case, SELECT controls the addressed channel with a high state putting that channel into sample mode.

The SELECT and CONFIG pins allow the design of a virtual 64-channel device using two of the MAX5167s. See the *Applications Information* section for more information about the 64 output addressing scheme.

Sample/Hold

The MAX5167 contains 32 buffered sample/hold circuits with internal hold capacitors. Internal hold capacitors minimize leakage current, dielectric absorption, feedthrough, and required board space. The value of the hold capacitor affects acquisition time and droop rate. Smaller capacitance allows faster acquisition times but increases the droop rate. Larger values increase hold acquisition time. The hold capacitor used in the MAX5167 provides fast 2.5 μ s (typ) acquisition time while maintaining a relatively low 1mV/s (typ) droop rate, making the sample/hold ideal for high-speed sampling.

Sample Mode

When SELECT and CONFIG are in opposing logic states, the $\overline{S/H}$ line controls the mode of operation. Sample mode is entered when $\overline{S/H}$ is low. During sample mode, the selected multiplexer channel connects to IN, allowing the

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Table 1. Channel/Output Selection

ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	OUTPUT
0	0	0	0	0	VOUT0 is selected
0	0	0	0	1	VOUT1 is selected
0	0	0	1	0	VOUT2 is selected
0	0	0	1	1	VOUT3 is selected
0	0	1	0	0	VOUT4 is selected
0	0	1	0	1	VOUT5 is selected
0	0	1	1	0	VOUT6 is selected
0	0	1	1	1	VOUT7 is selected
0	1	0	0	0	VOUT8 is selected
0	1	0	0	1	VOUT9 is selected
0	1	0	1	0	VOUT10 is selected
0	1	0	1	1	VOUT11 is selected
0	1	1	0	0	VOUT12 is selected
0	1	1	0	1	VOUT13 is selected
0	1	1	1	0	VOUT14 is selected
0	1	1	1	1	VOUT15 is selected
1	0	0	0	0	VOUT16 is selected
1	0	0	0	1	VOUT17 is selected
1	0	0	1	0	VOUT18 is selected
1	0	0	1	1	VOUT19 is selected
1	0	1	0	0	VOUT20 is selected
1	0	1	0	1	VOUT21 is selected
1	0	1	1	0	VOUT22 is selected
1	0	1	1	1	VOUT23 is selected
1	1	0	0	0	VOUT24 is selected
1	1	0	0	1	VOUT25 is selected
1	1	0	1	0	VOUT26 is selected
1	1	0	1	1	VOUT27 is selected
1	1	1	0	0	VOUT28 is selected
1	1	1	0	1	VOUT29 is selected
1	1	1	1	0	VOUT30 is selected
1	1	1	1	1	VOUT31 is selected

Table 2. Logic Table for CONFIG, SELECT, and \bar{S}/H

\bar{S}/H (SAMPLE/HOLD)	CONFIG	SELECT	CHANNEL FUNCTION
0	0	0	Hold
0	0	1	Sampling
0	1	0	Sampling
0	1	1	Hold
1	X	X	Hold

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hold capacitor to acquire the input signal. To guarantee an accurate sample, maintain sample mode for at least 4 μ s. The output of the sample/hold amplifier tracks the input after 4 μ s. Only the addressed channel on the selected multiplexer samples the input; all other channels remain in hold mode.

Hold Mode

No matter what the condition of the other control lines, $\overline{S}/H = \text{high}$ places the MAX5167 into an all-channel hold mode. Hold mode disables the multiplexer and disconnects all 32 sample/holds from the input. When a channel is disconnected, the hold capacitor maintains the sampled voltage at the output with a 1mV/s typical droop rate (towards V_{DD}).

Hold Step

When switching between sample mode and hold mode, the voltage of the hold capacitor changes due to charge injection from stray capacitance. This voltage change, called hold step, is minimized by limiting the amount of stray capacitance seen by the hold capacitor. The MAX5167 limits the hold step to 0.25mV (typ). An output capacitor to ground can be used to filter out this small hold-step error.

Output

The MAX5167 contains an output buffer for each multiplexer channel (32 total), so the hold capacitor sees a high-impedance input that reduces the droop rate. The capacitor droops at 1mV/s (typ) while in hold mode. The buffer also provides a low output impedance; however, the device contains output resistors in series with the buffer output (Figure 1) for selected output filtering. To provide greater design flexibility, the MAX5167 is available with an output impedance of 50 Ω , 500 Ω , or 1k Ω .

Output loads increase the analog supply current (I_{DD} and I_{SS}). Excessive loading of the output(s) drastically increases power dissipation. Do not exceed the maximum power dissipation specified in the *Absolute Maximum Ratings*.

The resistor-divider formed by the output resistor (R_O) and load impedance (R_L) scales the sampled voltage (V_{SAMP}). Determine the output voltage ($V_{OUT_}$) as follows:

$$\text{Voltage Gain} = A_V = R_L / (R_L + R_O)$$

$$V_{OUT_} = V_{SAMP} \times A_V$$

The maximum output voltage range depends on the analog supply voltages available and the scaling factor used:

$$(V_{SS} + 0.75V) \times A_V \leq V_{OUT_} \leq (V_{DD} - 2.4V) \times A_V$$

when $R_L = \infty$, then $A_V = 1$, and this equation becomes:

$$(V_{SS} + 0.75V) \leq V_{OUT} \leq (V_{DD} - 2.4V)$$

Output Clamp

The MAX5167 clamps the output between two externally applied reference voltages. Internal diodes connect all outputs to the clamping voltages, restricting the output voltage to:

$$(V_{CH} + 0.7V) \leq V_{OUT_} \leq (V_{CL} - 0.7V)$$

When the clamping voltage exceeds the maximum output voltage, the maximum output voltage will be the limiting factor. To disable output clamping, connect CH to V_{DD} and CL to V_{SS} to set the clamping voltages beyond the maximum output voltage range. The clamping diodes allow the MAX5167 to be used with other devices requiring restricted input voltages.

Timing Definitions

Acquisition time (t_{AQ}) is the time the MAX5167 must remain in sample mode for the hold capacitor to acquire an accurate sample. The hold-mode settling time (t_H) is the time necessary for the output voltage to settle to its final value. Aperture delay (t_{AP}) is the time interval required to disconnect the input from the hold capacitor. The hold pulse width (t_{PW}) is the time the MAX5167 must remain in hold mode while the address is changed. Data setup time (t_{DS}) is the time an address must be maintained at the digital input pins before the address becomes valid. Data hold time (t_{DH}) is the time an address must be maintained after the device is placed in hold mode (Figure 2).

Applications Information

Multiplexing a DAC

Figure 3 shows a typical demultiplexer application. Different digital codes are converted by the digital-to-analog converter (DAC) and then stored on 32 different channels of the MAX5167. The 40mV/s (max) droop rate requires refreshing the hold capacitors every 250ms before the voltage droops by 1/2LSB for an 8-bit DAC with a 5V full-scale voltage.

Virtual 64 Output Sample and Hold

Two MAX5167s can be configured to operate as a single 64 output sample and hold. The upper and lower addressed devices are identified by CONFIG's logic level. Connect the CONFIG pin of the upper device low, making its SELECT pin active-high. Connect the CONFIG pin of the lower device high to make the SELECT pin active-low. Figure 4 shows how to configure the devices.

The devices now use only six address lines and a single \overline{S}/H control to decode 64 outputs. Address lines A0–A4 from the control logic connect to ADDR0–ADDR4 on

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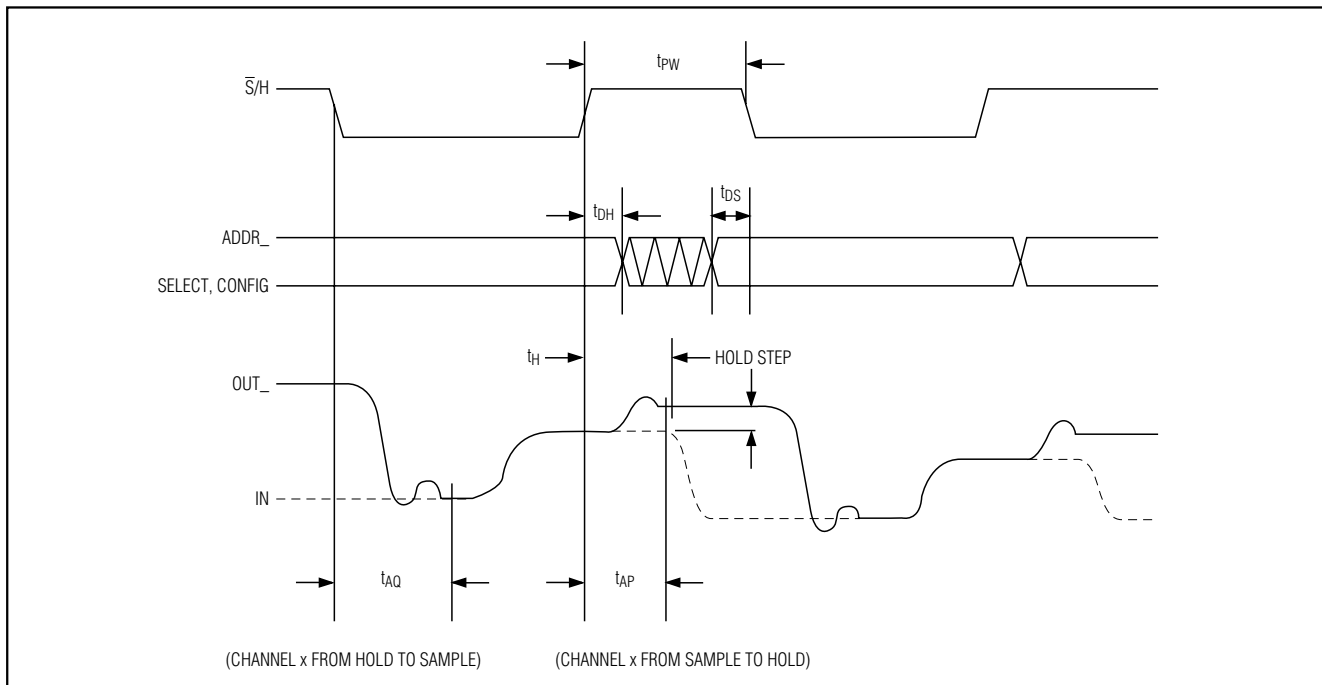


Figure 2. Timing Diagram

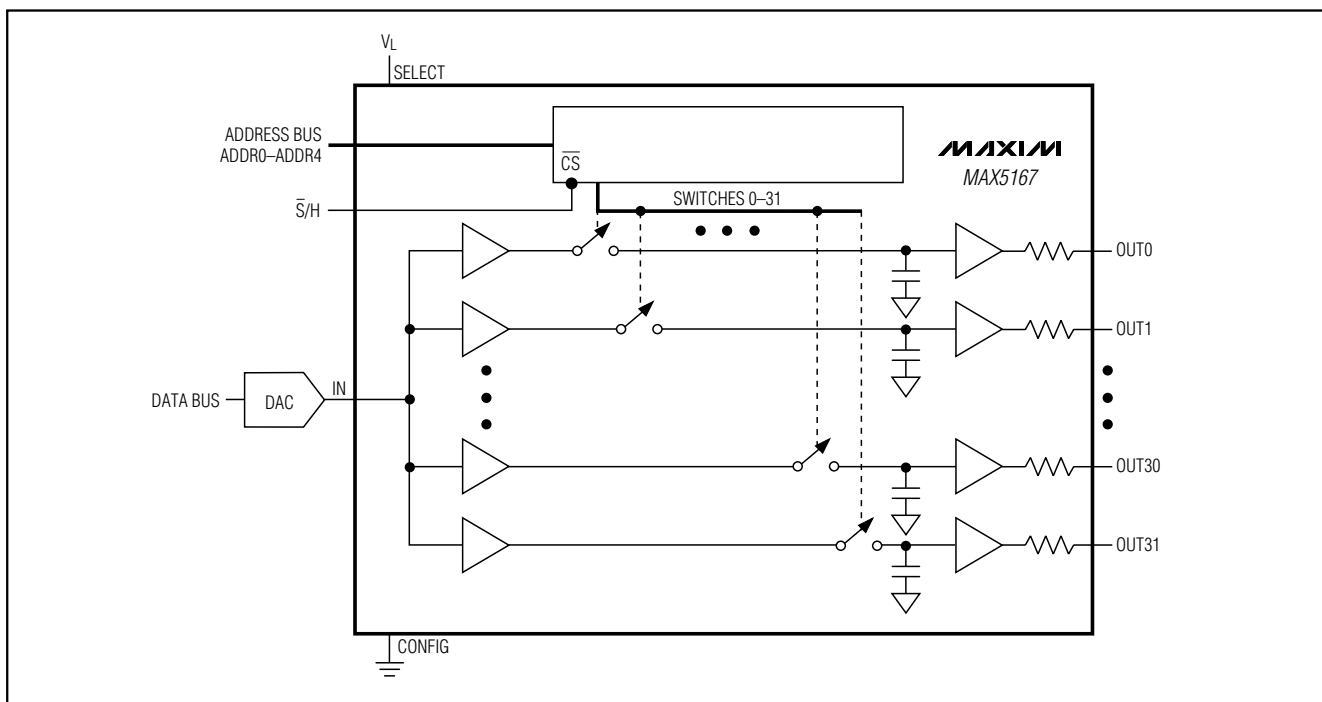


Figure 3. Multiplexing a DAC

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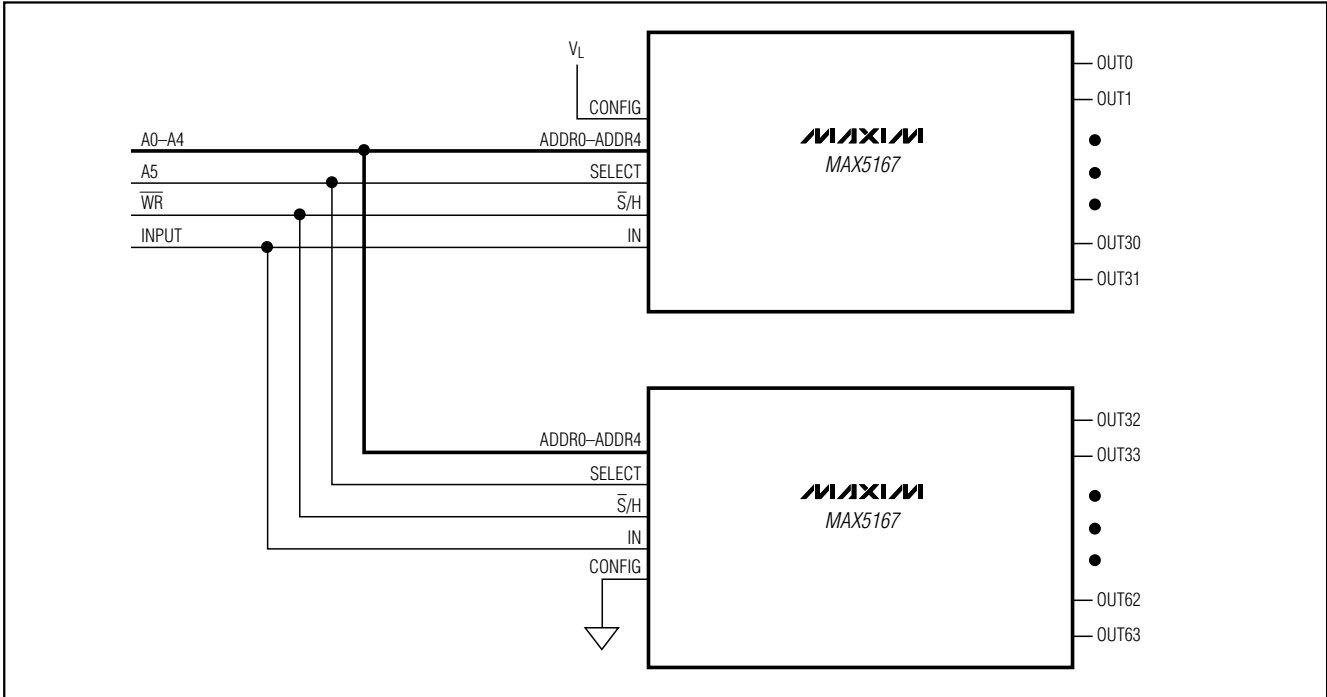


Figure 4. 64 Output Sample-and-Hold Circuit

both of the 32-channel devices. The A5 line toggles the SELECT pins of both devices to select the active one. The device that has CONFIG tied high responds to the lower 32 addresses (000000 through 011111). The device that has CONFIG grounded responds to the upper 32 addresses (100000 through 111111).

Input Drive Requirements

The input of the MAX5167 feeds the inputs of 32 high-impedance buffers. These buffers are what charge the sample/hold capacitor through the multiplexer switch resistance. The bias current of a selected buffer is 10 μ A, and this feeds into the 10pF input capacitance. Figure 5 shows an equivalent input circuit. The bias currents of the other 31 sample and holds are very small in comparison to the bias current of the selected channel.

Powering the MAX5167

The MAX5167 does not require a special power-up sequence to avoid latchup. The device requires three separate supply voltages for operation. However, when one or two of the voltages are not available, DC-DC charge-pump (switched-capacitor) converters provide a simple, efficient solution. The MAX860 provides voltage doubling or inversion, ideal for conversions from +5V to +10V or from +5V to -5V.

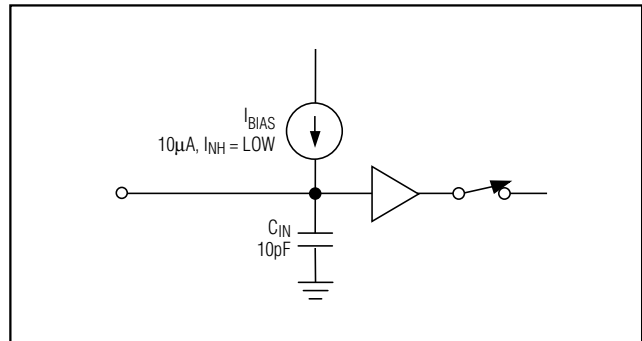


Figure 5. Input Equivalent Circuit

Chip Information

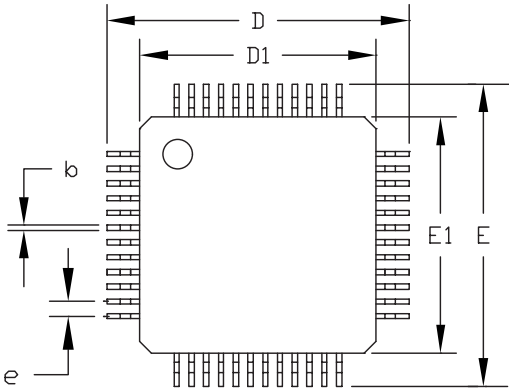
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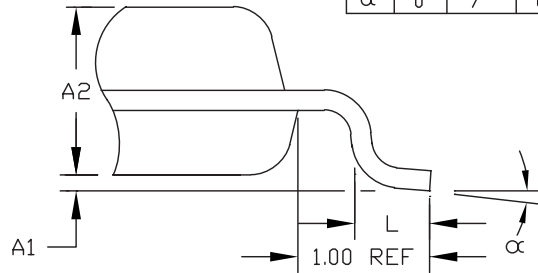
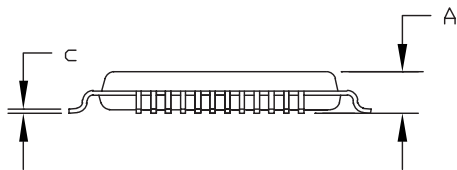
Package Information

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32L/48L, TQFP, EPS



	JEDEC VARIATION			
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A ₁	0.05	0.15	0.05	0.15
A ₂	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D ₁	7.00	BSC.	7.00	BSC.
E	8.90	9.10	8.90	9.10
E ₁	7.00	BSC.	7.00	BSC.
e	0.8	BSC.	0.5	BSC.
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM		
<small>PROPRIETARY INFORMATION</small>		
<small>TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP</small>		
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO. 21-0054</small>	<small>REV D 1/1</small>

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NOTES

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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