LF412AM/883, LF412M/883 and OP-215/883

T-79-15

Dual Precision JFET Input Op Amp

DESCRIPTION

Linear Technology's LF412A/AM/883 and OP-215/883 series of dual JFET input op amps feature several improvements compared to similar types from other manufacturers.

Both devices have lower input bias and offset currents over the entire temperature range, and are available in all standard 8-pin packages.

In addition, Linear's LF412A/883 has lower voltage noise and higher voltage gain. Linear's OP-215 supply currents are nearly halved.

These devices are processed to the requirements of MIL-STD-883 Class B to yield circuits usable in precision military applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LF412AM, OP-215A ..... ±22V
- LF412M, OP-215C ..... ±18V

Internal Power Dissipation 670mW

Differential Input Voltage
- LF412AM, OP-215A ..... ±40V
- LF412M, OP-215C ..... ±30V

Input Voltage (Note C)
- LF412AM, OP-215A ..... ±20V
- LF412M, OP-215C ..... ±16V

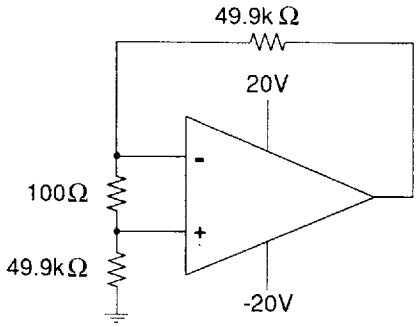
Output Short Circuit Duration ..... Indefinite

Operating Temperature Range ..... -55°C to 125°C

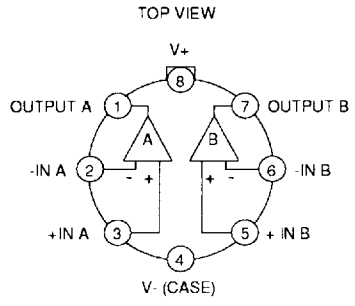
Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

BURN-IN CIRCUIT

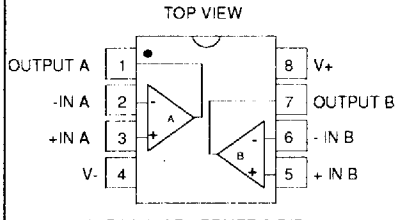


PACKAGE/ORDER INFORMATION



H PACKAGE METAL CAN

ORDER PART NO.
LF412AMH/883 LF412MH/883 OP-215AH/883 OP-215CH/883
PART MARKING†
LF412AMH/883C LF412MH/883C OP-215AH/883C OP-215CH/883C



J8 PACKAGE HERMETIC DIP

ORDER PART NO.
LF412AMJ8/883 LF412MJ8/883 OP-215AJ8/883 OP-215CJ8/883
PART MARKING†
LF412AMJ8/883C LF412MJ8/883C OP-215AJ8/883C OP-215CJ8/883C

† The suffix letter "C" of the part mark indicates compliance per MIL-STD-883, para 1.7.1.1.

TABLE 1: ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	OP-215A MIN	OP-215A TYP	OP-215A MAX	LF412AM MIN	LF412AM TYP	LF412AM MAX	LF412M, OP-215C MIN	LF412M, OP-215C TYP	LF412M, OP-215C MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage				0.2	1.0		0.3	1.0		0.5	3.0	1	mV
I_{OS}	Input Offset Current	$T_J = 25°C$	A		6	50		6	50		10	100	1	pA
		Warmed-Up	A		10	100		10	100		15	200	1	pA
I_B	Input Bias Current	$T_J = 25°C$	A		±10	±100		±10	±100		±15	±200	1	pA
		Warmed-Up	A		±15	±300		±15	±300		±20	±400	1	pA
R_{IN}	Input Resistance				10^{12}			10^{12}			10^{12}			Ω
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		150	400		100	300		50	250		4	V/mV
V_O	Output Voltage Swing	$R_L = 10k\Omega$		±12	±13		±12	±13		±12	±13		4	V
		$R_L = 2k\Omega$		±11	±12.7		±11	±12.7		±11	±12.7		4	V
I_S	Supply Current				3.8	6.0		3.8	6.0		3.8	6.8	1	mA
SR	Slew Rate			10	15		10	15		8	13		7	V/µs
GBW	Gain Bandwidth Product		B	3.5	5.7		3.5	5.7		3.0	5.5			MHz
	Settling Time	to 0.01%			2.3			2.3			2.4			µs
		to 0.10%			1.1			1.1			1.2			µs
	Input Voltage Range		B	±11	+14.5		±11	+19.5		±11	+14.5			V
			B		-11.5			-16.5			-11.5			V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$					80	100					1	dB
		$V_{CM} = \pm 11V$		78	100					72	100		1	dB
		$V_{CM} = \pm 10.5V$		86	100					82	100		1	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$					80	100					1	dB
		$V_S = \pm 10V$ to $\pm 18V$		86	100					80	100		1	dB
e_n	Input Noise Voltage Density	$f_o = 100Hz$			20			20			20			nV/√Hz
		$f_o = 1000Hz$			15			15			15			nV/√Hz
i_n	Input Noise Current Density	$f_o = 100Hz$			0.01			0.01			0.01			pA/√Hz
		$f_o = 1000Hz$			0.01			0.01			0.01			pA/√Hz
	Channel Separation	f = 1Hz to 20kHz			120			120			120			dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55° \leq T_A \leq 125°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	OP-215A MIN	OP-215A TYP	OP-215A MAX	LF412AM MIN	LF412AM TYP	LF412AM MAX	LF412M, OP-215C MIN	LF412M, OP-215C TYP	LF412M, OP-215C MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage				0.5	2.0		0.7	2.0		1.0	5.0	2,3	mV
	Average Input Offset Voltage Drift		B		3	10		4	10		5	20	2,3	µv/°C
I_{OS}	Input Offset Current	$T_J = 125°C$	A		0.8	8		0.8	8		1.0	12	2	nA
		$T_A = 125°C$, Warmed-Up	B		1.2	14		1.2	14		1.5	22	2	nA
I_B	Input Bias Current	$T_J = 125°C$	A		±1.5	±10		±1.5	±10		±1.8	±15	2	nA
		$T_A = 125°C$, Warmed-Up	B		±2.2	±18		±2.2	±18		±2.7	±28	2	nA
	Input Voltage Range	OP-215	B	±10.3	+14.5					±10.3	+14.5			V
			B		-11.5						-11.5			V
		LF412	B				±16	+19.5		±11	+14.5			V
			B					-16.5			-11.5			V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$					80	100					2,3	dB
		$V_{CM} = \pm 11V$								70	100		2,3	dB
		$V_{CM} = \pm 10.3V$		82	100					80	100		2,3	dB
I_S	Supply Current				4.2	6.8		4.0	5.6		4.2	6.8	2,3	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$					80	100					2,3	dB
		$V_S = \pm 10V$ to $\pm 16V$		80	100					78	100		2,3	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		30	150		30	150		25	150		5,6	V/mV
		$V_S = \pm 15V$												
V_O	Output Voltage Swing	$R_L \geq 10k\Omega$		±12	±13		±12	±13		±12	±13		5,6	V

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Note A: Input bias and offset currents are specified for two different conditions. The T_J specification is with the junction at ambient temperature; the warmed-up specification is with the device operating in a warmed-up condition at the ambient temperture specified.

Note B: This parameter is guaranteed by design, characterization, or correlation to other tests.

Note C: Maximum negative input voltage is equal to the negative supply voltage.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6,7
Group A Test Requirments (Method 5005)	1,2,3,4,5,6,7
Group C and D End Point Electrical Parameters (Method 5005)	1

* PDA applies to subgroup 1. See PDA test notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.