Wireless Li-Ion Charger with 1.2V Step-Down DC/DC Converter

FEATURES

- **Wireless Li-Ion Battery Charger Plus High Efficiency Multi-Mode Charge Pump DC/DC**
- **Programmable Charge Current from 1mA to 50mA Via an External Resistor**
- **Wideband Rx Frequency: DC to >10MHz**
- Integrated Rectifier with Overvoltage Limit
- Charge Voltage: 4.2V
- Low Battery Disconnect: 3.0V
- NTC Pin for Temperature Qualified Charging
- DC/DC Regulated Output: 1.2V
- DC/DC Output Current: Up to 60mA
- 50kHz/75kHz Switching, No Audible Noise
- Pushbutton and/or Digital on/off Control for DC/DC
- Thermally Enhanced 12-Lead 2mm × 2mm LQFN Package

APPLICATIONS

- Hearing Aids
- Low Power Li-Ion Powered Devices
- Wireless Headsets
- IoT Wearables

DESCRIPTION

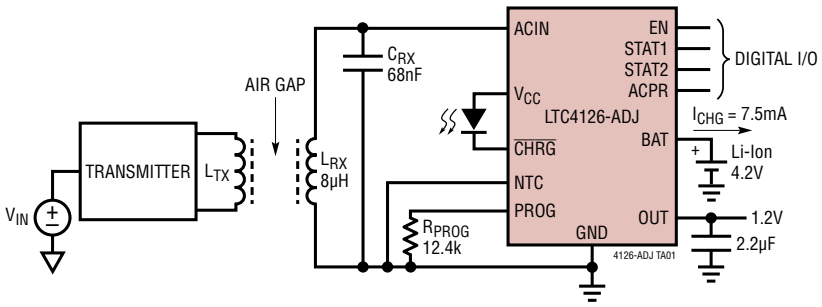
The LTC®4126-ADJ is a low-power wireless single-cell Li-Ion battery charger with an integrated step-down DC/DC regulator. The step-down regulator is a low-noise multi-mode charge pump which is powered from the battery and provides a regulated 1.2V at the output. The switching frequency is set to either 50kHz or 75kHz depending on the mode to keep any switching noise out of the audible range.

The constant-current constant-voltage Li-Ion battery charger has automatic recharge, automatic termination by safety timer, and battery temperature monitoring via an NTC pin. Charge current is programmable from 1mA to 50mA via an external resistor. Undervoltage protection disconnects the battery from all loads when the battery voltage is below 3.0V.

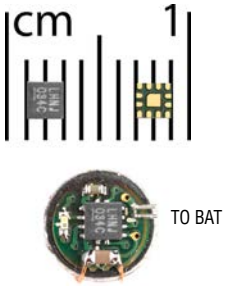
The small package and minimal external component count make the LTC4126-ADJ and its variants suitable for hearing aid applications and other low power portable devices. See the chart below.

PARAMETER		LTC4126-ADJ	LTC4126-10	LTC4126
Charge Current		Programmable	10mA	7.5mA
Charge Timer		6 Hours	3 Hours	6 Hours
Charge Voltage		4.2V	4.1V/4.2V	4.2V/4.35V
EN Pin Polarity		Active High	Active Low	Active High
EN Pin Pull-Up		N/A	1MΩ	N/A
NTC Upper Threshold		76.5% of V_{CC}	62% of V_{CC}	76.5% of V_{CC}
V_{LOBAT3}		3.2V	3.5V	3.2V
DC/DC Mode 3	Threshold	1.1V	1.05V	1.1V
	Timing	110ms	1.7s	110ms

TYPICAL APPLICATION



Top and Bottom View of the IC with Complete Application Circuit



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Input Supply Voltages
- V_{CC} ..... –0.3V to 6V
- ACIN ..... –10V to 6V
- ACIN – V_{CC} Differential ..... –16V to 0.3V

Input/Output Currents
- I_{ACIN} 200mA
- I_{OUT} ..... –60mA

BAT ..... –0.3V to 6V

$\overline{PBEN}$, NTC, EN, PROG ..... –0.3V to [Max (V_{CC}, BAT) + 0.3V]

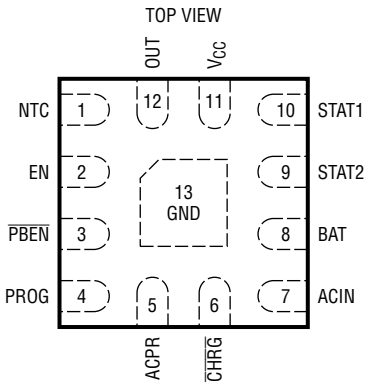
$\overline{CHRG}$ ..... –0.3V to 6V

Operating Junction Temperature Range ... –20°C to 85°C

Storage Temperature Range ..... –40°C to 125°C

Maximum Reflow (Package Body) Temperature ..... 260°C

PIN CONFIGURATION



LQFN PACKAGE
12-LEAD (2mm × 2mm × 0.74mm)
T_{JMAX} = 85°C, θ_{JA} = 92°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

TAPE AND REEL PART NUMBER	PART MARKING*	FINISH CODE	PAD FINISH	PACKAGE** TYPE	MSL RATING	TEMPERATURE RANGE
LTC4126EV-ADJ#TRPBF	LHNJ	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–20°C to 85°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is identified by a label on the shipping container.

Parts ending with PBF are RoHS and WEEE compliant. **The LTC4126-ADJ package dimension is 2mm × 2mm × 0.74mm compared to a standard QFN package dimension of 2mm × 2mm × 0.75mm.

This product is only available in tape and reel or in mini-reel.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{ACIN} = V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Input Voltage Range		●	2.7		5.5	V
V_{BAT}	Battery Voltage Range	Charging		2.7		4.25	V
		Not Charging, DC/DC On		3.1		4.25	V
I_{VCC}	V_{CC} Quiescent Current	Charging Done, DC/DC Off, V_{NTC} > V_{DIS}			50	80	µA
		Charging Done, DC/DC Off, V_{NTC} < V_{DIS}			42	70	µA
I_{BATQ}	BAT Quiescent Current	Charging Done, DC/DC Off, V_{BAT} = 4.25V			4	8	µA
		V_{ACIN} = V_{CC} = 0, DC/DC On, I_{OUT} = 0			37	75	µA
		V_{ACIN} = V_{CC} = 0, DC/DC Off			5	10	µA
		V_{ACIN} = V_{CC} = 0, Battery Disconnected (V_{BAT} < $V_{DISCONNECT}$)			0	0.1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{ACIN} = V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Rectification							
$V_{CC(HIGH)}$	V_{CC} High Voltage Limit	V_{CC} Rising		5.25	5.5	5.75	V
$V_{CC(LOW)}$	V_{CC} Low Voltage Limit	V_{CC} Falling		4.75	5	5.25	V
	ACIN to V_{CC} Voltage Drop	7.5mA from ACIN to V_{CC}			0.6		V
Battery Charger							
V_{CHG}	Battery Charge Voltage		●	4.158	4.200	4.242	V
I_{CHG}	Battery Charge Current	R_{PROG} = 0Ω	 ●	47 40	50 50	53 60	mA mA
		R_{PROG} = 107kΩ	●	0.76	1.01	1.26	mA
		R_{PROG} = 0Ω to 107kΩ, As a Percentage of Typical Value	●	75	100	125	%
ΔV_{UVLO}	V_{CC}-to-V_{BAT} Differential Undervoltage Lockout Threshold (Indicated at ACPR Pin)	V_{CC} Falling V_{CC} Rising		9 55	27 80	45 105	mV mV
ΔV_{UVCL}	V_{CC}-to-V_{BAT} Differential Undervoltage Current Limit Threshold Voltage	I_{BAT} = 0.9 • I_{CHG} I_{BAT} = 0.1 • I_{CHG}			200 120		mV mV
I_{DUVCL}	Charge Current Threshold for DUVCL Fault Indication	(V_{CC} – V_{BAT}) Falling (V_{CC} – V_{BAT}) Rising			40 60		% %
V_{RECHRG}	Recharge Battery Threshold Voltage	As a Percentage of V_{CHG}		96.5	97.5	98.5	%
$t_{TERMINATE}$	Safety Timer Termination Period	Timer Starts at the Beginning of the Charge Cycle, V_{CC} > (V_{BAT} + 100mV)		5.1	6	6.9	hours
f_{SLOW}	Slow Blink Frequency				1.14		Hz
f_{FAST}	Fast Blink Frequency				4.58		Hz
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Voltage		75.0	76.5	78	%V_{CC}
		Hysteresis			1.5		%V_{CC}
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Voltage		33.4	34.9	36.4	%V_{CC}
		Hysteresis			1.5		%V_{CC}
V_{DIS}	NTC Disable Threshold Voltage				150	250	mV
I_{NTC}	NTC Leakage Current	V_{NTC} = 2.5V		–100		100	nA
		V_{NTC} = 0V			–150		nA
Step-Down DC/DC Regulator							
V_{OUT}	DC/DC Regulator Output Voltage	V_{BAT} > V_{LOBAT1} or $V_{DISCONNECT}$ < V_{BAT} < V_{LOBAT2}, I_{OUT} = 0	●	1.16	1.2	1.24	V
		V_{LOBAT2} < V_{BAT} < V_{LOBAT1}, I_{OUT} = 0			V_{BAT}/3		V
V_{LOBAT1}	Low Battery Alert 1 Threshold	V_{BAT} Falling	●	3.52	3.6	3.68	V
		Hysteresis			100		mV
V_{LOBAT2}	Low Battery Alert 2 Threshold	V_{BAT} Falling	●	3.22	3.3	3.38	V
		Hysteresis			100		mV
V_{LOBAT3}	Low Battery Alert 3 Threshold	V_{BAT} Falling	●	3.12	3.2	3.28	V
		Hysteresis			100		mV
$V_{DISCONNECT}$	Low Battery Disconnect Threshold Voltage	V_{BAT} Falling	●	2.93	3	3.07	V
f_{SW}	DC/DC Switching Frequency	3:1 Mode (V_{BAT} > V_{LOBAT2}) 2:1 Mode (V_{BAT} < V_{LOBAT2})	● ●	40 60	50 75	60 90	kHz kHz
R_{OL}	Effective Open-Loop Output Resistance (Note 4)	V_{BAT} = 3.5V, I_{OUT} = 3mA			4.6	6.5	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{ACIN} = V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LIM}	OUT Current Limit	V_{OUT} = 0V			80		mA
Pushbutton Pin ($\overline{PBEN}$)							
V_{IL}	Logic Low Input Voltage		●			0.4	V
V_{IH}	Logic High Input Voltage		●	1.1			V
R_{PU}	Pull-up Resistance to BAT	$V_{\overline{PBEN}} < V_{IL}$			4		MΩ
I_{IH}	Logic High Input Leakage	$V_{\overline{PBEN}} = V_{BAT}$			0	0.1	µA
t_{DBL}	Debounce Time Low			348	425	503	ms
t_{DBH}	Debounce Time High			23	43	63	ms
EN Pin							
V_{IL}	Logic Low Input Voltage		●			0.4	V
V_{IH}	Logic High Input Voltage		●	1.1			V
I_{IL}	Logic Low Input Leakage				0	1	µA
I_{IH}	Logic High Input Leakage				0	1	µA
Logic Output Pins (STAT1, STAT2, ACPR)							
V_{OL}	Logic Low Output Voltage	100µA into Pin				0.2	V
V_{OH}	Logic High Output Voltage	25µA out of Pin		V_{OUT} – 0.2			V
Open-Drain Output ($\overline{CHRG}$)							
	Pin Leakage Current	$V_{\overline{CHRG}}$ = 5V			0	0.5	µA
	Pin Pull-Down Current	$V_{\overline{CHRG}}$ = 400mV		200	300	450	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3: The LTC4126EV-ADJ is tested under conditions such that $T_J \approx T_A$. The LTC4126EV-ADJ is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –20°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

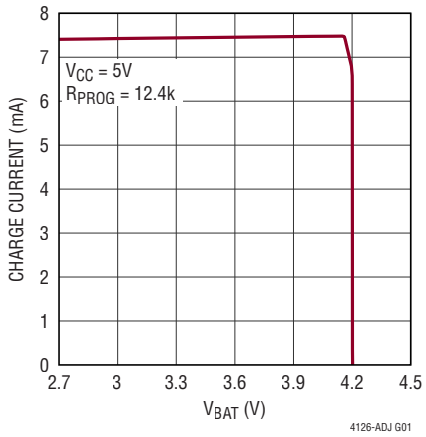
where the package thermal impedance θ_{JA} = 92°C/W).
Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Note 4: See DC/DC Converter in Operation section.

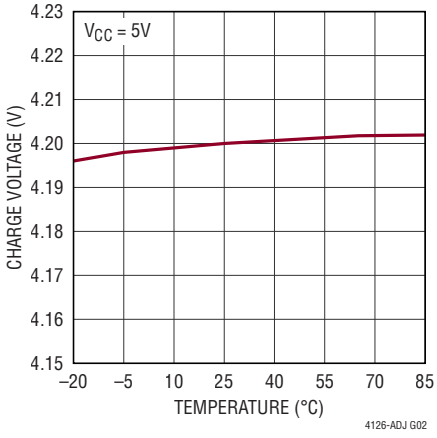
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

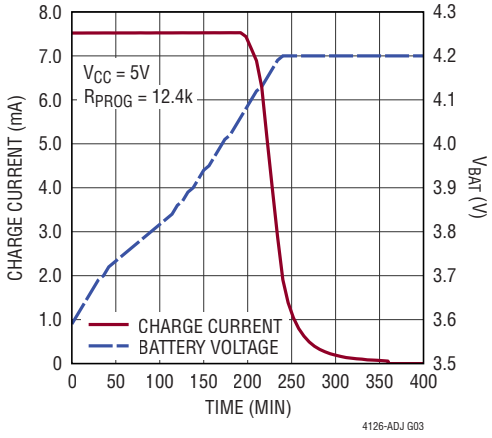
Charge Current vs Battery Voltage



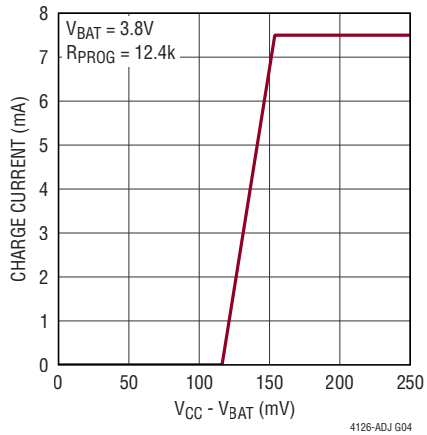
Charge Voltage vs Temperature



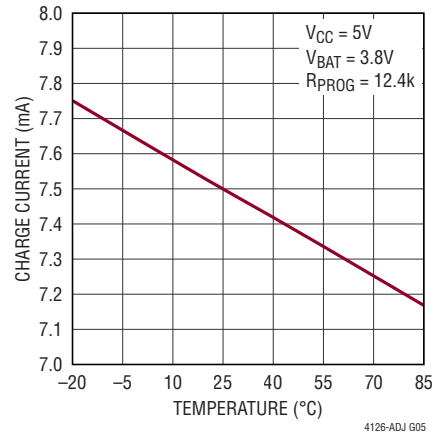
Li-Ion Battery Charge Profile



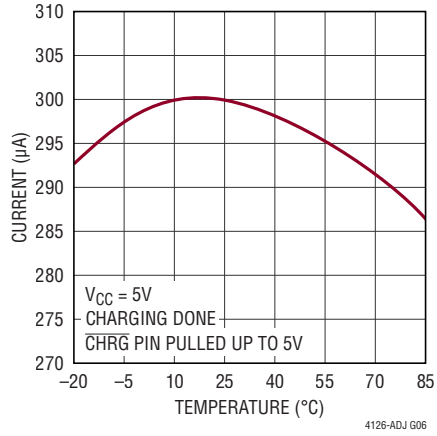
Charge Current vs V_{CC}-to-V_{BAT} Differential Voltage



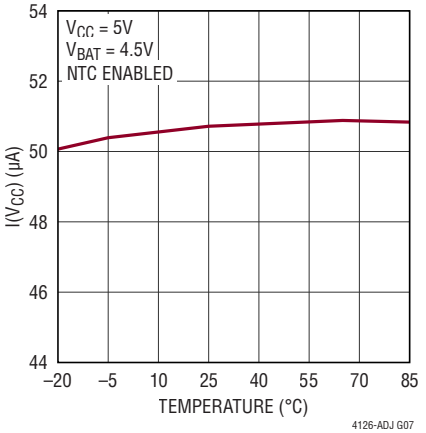
Charge Current vs Temperature



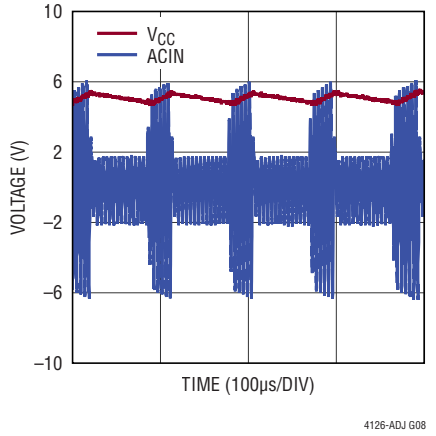
$\overline{CHRG}$ Pin Current vs Temperature



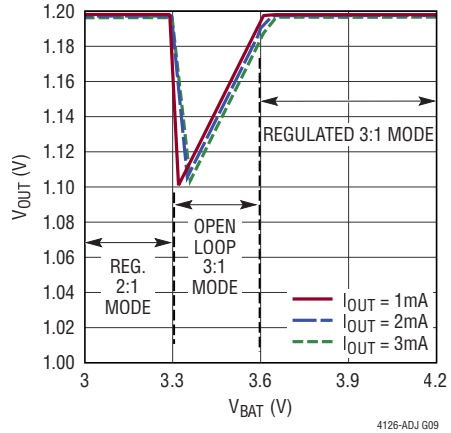
V_{CC} Quiescent Current vs Temperature



ACIN and V_{CC} Waveforms when Shunt Active

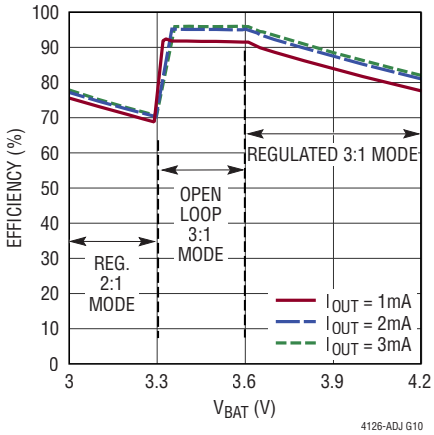


DC/DC Output Voltage vs Battery Voltage

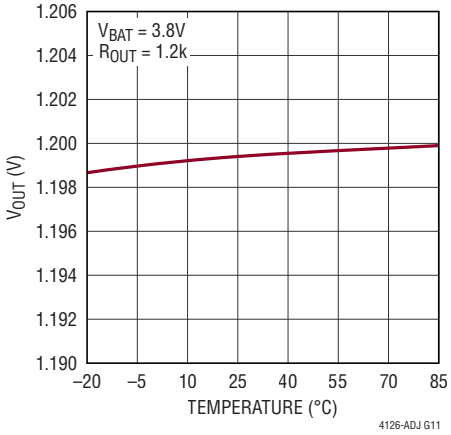


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

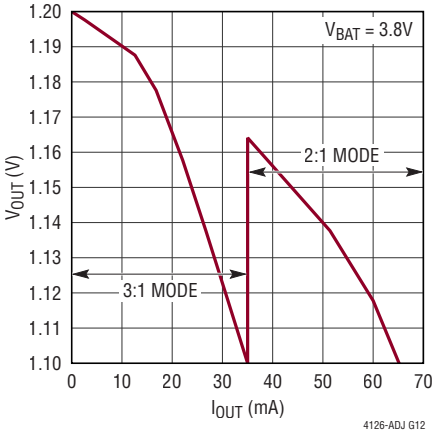
DC/DC Efficiency vs Battery Voltage



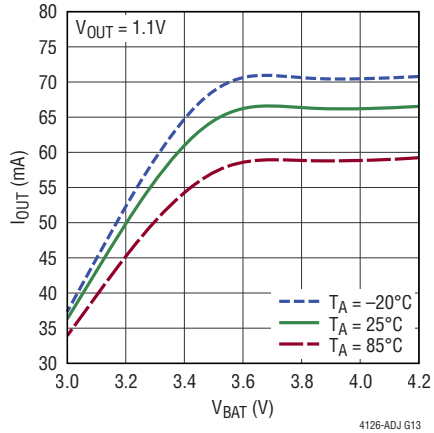
DC/DC Output Voltage vs Temperature



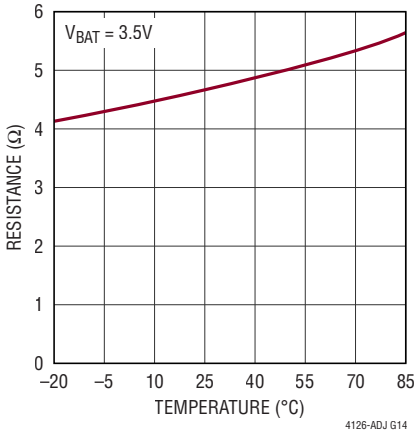
DC/DC Output Voltage vs Load Current



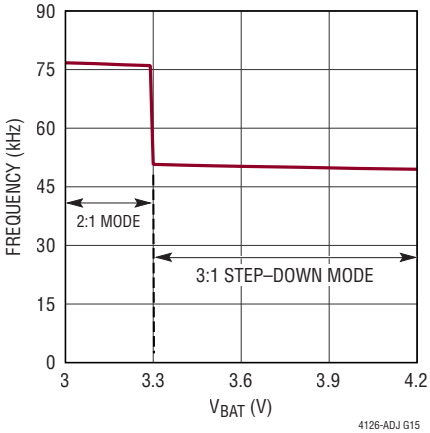
Maximum DC/DC Output Current vs Battery Voltage



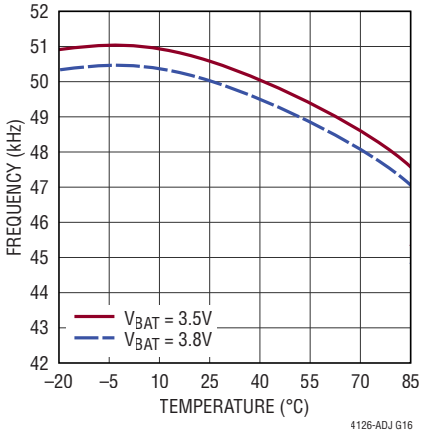
DC/DC Effective Open-Loop Output Resistance vs Temperature



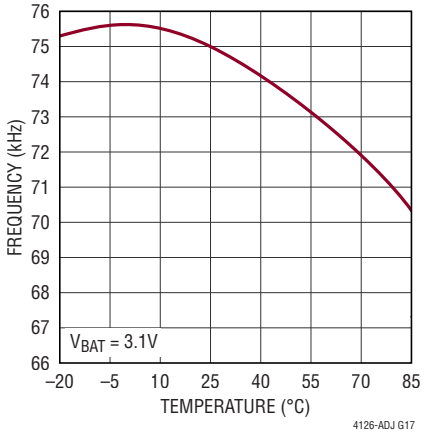
DC/DC Switching Frequency vs Battery Voltage



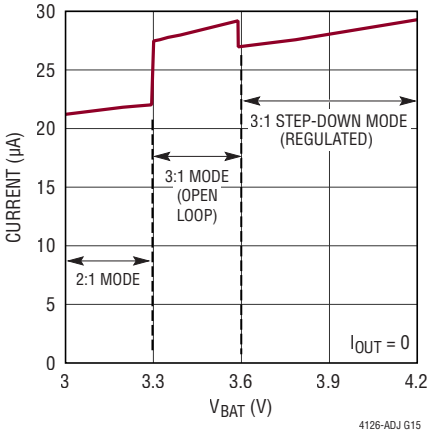
DC/DC Switching Frequency in 3:1 Mode vs Temperature



DC/DC Switching Frequency in 2:1 Mode vs Temperature



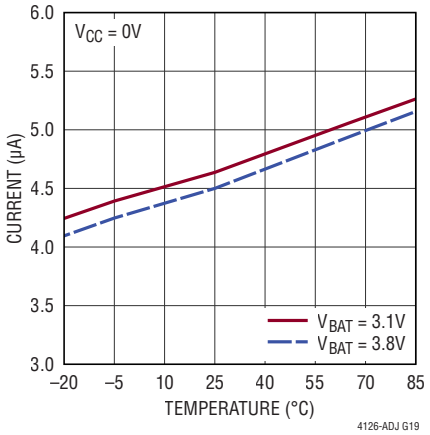
BAT No-Load Quiescent Current (DC/DC On) vs Battery Voltage



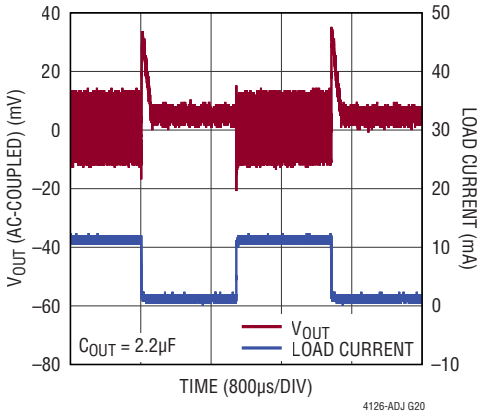
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

BAT Quiescent Current (DC/DC Off) vs Temperature



DC/DC Output Transient Response to Load Step



PIN FUNCTIONS

NTC (Pin 1): Thermistor Input. Connect a thermistor from NTC to GND, and a bias resistor from V_{CC} to NTC. The voltage level on this pin determines if the battery temperature is safe for charging. The charge current and charge timer are suspended if the thermistor indicates a temperature that is unsafe for charging. Once the temperature returns to the safe region, charging resumes. Ground the NTC pin if temperature qualified charging is not needed.

EN (Pin 2): Digital Logic Input Pin to Enable the DC/DC Converter. A minimum voltage of 1.1V enables the regulator provided that the LTC4126-ADJ is not in battery disconnect mode (see Battery Disconnect/Ship Mode under Operation section). A low voltage (0.4V max) disables the regulator and allows the pushbutton to control it. If only pushbutton control is desired, tie this pin to GND. Tie this pin to BAT if the DC/DC needs to remain enabled all the time. Do not leave this pin unconnected.

$\overline{\text{PBEN}}$ (Pin 3): Pushbutton Toggle Input Pin to enable/disable the DC/DC converter. Enabling of the regulator can only occur if the LTC4126-ADJ is not in battery disconnect mode (see Battery Disconnect/Ship Mode under Operation section). A weak internal pull-up forces $\overline{\text{PBEN}}$ high when not driven. A normally open pushbutton is connected from $\overline{\text{PBEN}}$ to GND to force a low state on this pin when the button is pushed. However, the pushbutton is ignored if the EN input is high. If the pushbutton function is not needed, leave this pin unconnected.

PROG (Pin 4): Charge Current Program Pin. A 1% resistor, R_{PROG}, connected from PROG to GND programs the charge current as such:

$$R_{PROG} = \frac{100 \bullet 1.1V}{I_{CHG}} - 2.2k\Omega$$

with I_{CHG} being the desired battery charge current. The minimum and maximum resistances allowed for R_{PROG} are 0Ω and 107kΩ, respectively. Do not leave this pin unconnected.

ACPR (Pin 5): Digital CMOS Logic Output Pin to indicate if there is enough input power available to charge the battery. This pin goes high when the V_{CC}-to-BAT differential voltage rises above 80mV (typical) and goes low when the differential voltage drops below 27mV (typical). The low level of this pin is referenced to GND and the high level is referenced to the OUT pin voltage. Consequently, this indicator is not available if the DC/DC is disabled.

PIN FUNCTIONS

$\overline{\text{CHRG}}$ (Pin 6): Open-Drain Charge Status Output Pin. This pin can be pulled up through a resistor and/or an LED to indicate the status of the battery charger. This pin has four possible states: slow blink to indicate charging, fast blink to indicate a fault, pulled down to indicate charging done, and high impedance to indicate no input power. To conserve power, the pull-down current is limited to 300µA.

ACIN (Pin 7): AC Input Voltage Pin. Connect the external LC tank, which includes the receive coil, to this pin. Connect this pin to GND when not used.

BAT (Pin 8): Battery Connection Pin. Connect a single-cell Li-Ion battery to this pin. Whenever enough input power (AC or DC) is available, the battery will be charged via this pin. Additionally, the DC/DC Converter is powered from the battery via this pin. To minimize the effect of switching noise from the DC/DC converter on charger performance, this pin should be decoupled with a 1µF capacitor to GND if the DC/DC converter is enabled while charging.

STAT2 (Pin 9), STAT1 (Pin 10): Digital CMOS Logic Status Output Pins. The low level of these pins is referenced to GND and the high level is referenced to V_{OUT}. Consequently, these indicators are not available if the DC/DC is disabled. These two pins together with ACPR indicate the various charging states and fault conditions. However, when no input power is available and the DC/DC converter is enabled, these pins instead indicate the voltage level of the battery.

V_{CC} (Pin 11): DC Input Voltage Pin. An internal diode is connected from the ACIN pin (anode) to this pin (cathode). When an AC voltage is present at the ACIN pin, the voltage on this pin is the rectified AC voltage. When the ACIN pin is not used (or shorted to GND), connect this pin to a DC voltage source to provide power to the LTC4126-ADJ and charge the battery.

OUT (Pin 12): DC/DC Converter Output Pin. This pin provides 1.2V to power hearing aid ASICs. A low ESR ceramic capacitor of at least 2.2µF should be placed close to this pin to stabilize the converter.

GND (Exposed Pad Pin 13): Ground Pin. The exposed pad on the backside of the package must be soldered to the PCB ground for a low-resistance electrical connection as well as for optimum thermal performance.

BLOCK DIAGRAM

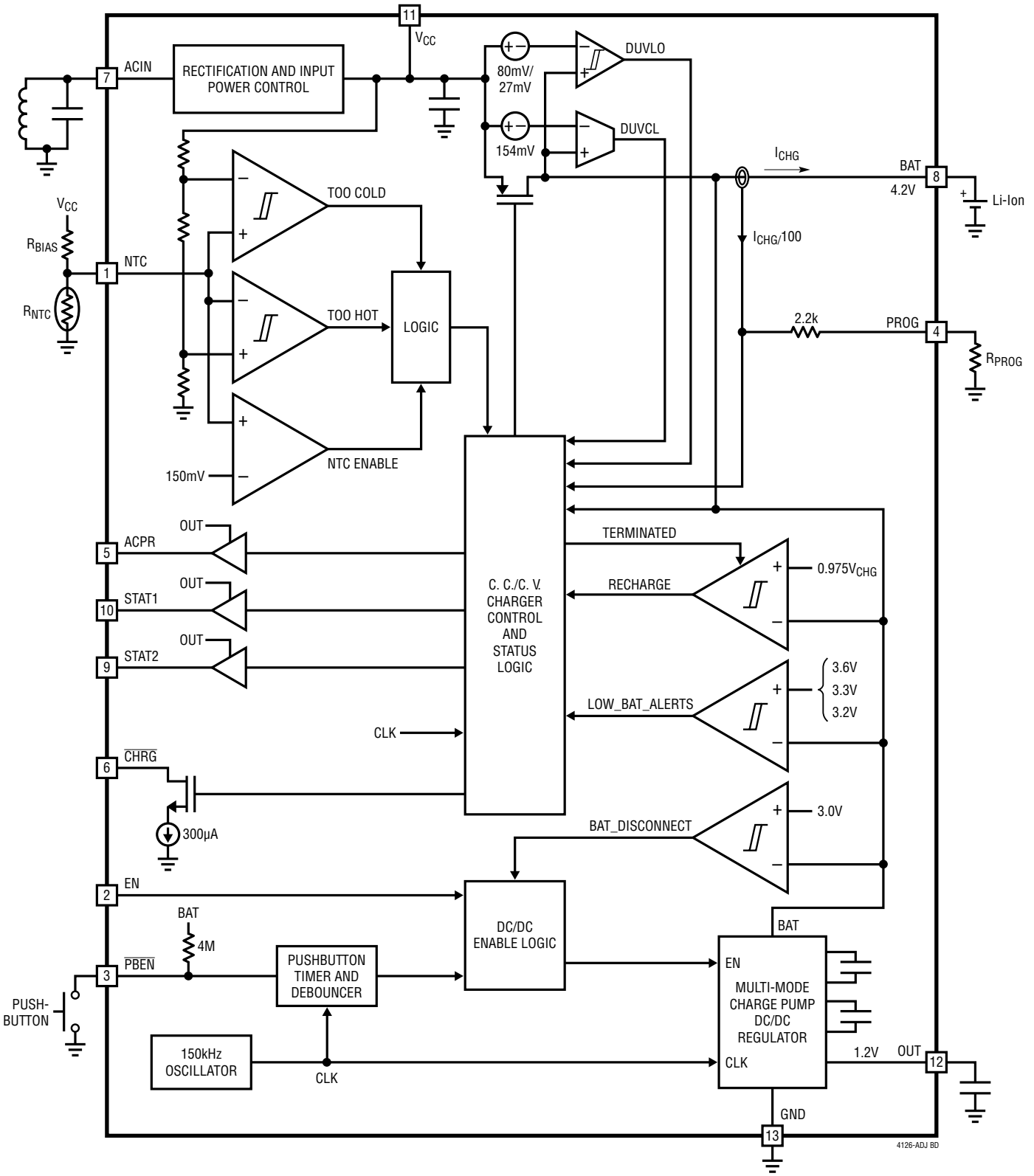


Figure 1. LTC4126-ADJ Block Diagram

OPERATION

The LTC4126-ADJ is a low power battery charger with an integrated step-down DC/DC converter designed to wirelessly charge single-cell Li-Ion batteries and provide a 1.2V output suitable for powering a hearing-aid ASIC. The part has three principal circuit components: an AC power controller, a full-featured linear battery charger, and a step-down DC/DC converter.

AC POWER CONTROLLER

A complete wireless power transfer system consists of transmit circuitry with a transmit coil and receive circuitry with a receive coil. The LTC4126-ADJ resides on the receiver side, where an external parallel resonant LC tank connected to the ACIN pin allows the part to receive power wirelessly from an alternating magnetic field generated by the transmit coil. The Rectification and Input Power Control circuitry (Figure 1) rectifies the AC voltage at the ACIN pin and regulates that rectified voltage at the V_{CC} pin to less than $V_{CC(HIGH)}$ (typically 5.5V).

Operation without Wireless Power

The LTC4126-ADJ can be alternately powered by connecting a DC voltage source to the V_{CC} pin directly instead of receiving power wirelessly through the ACIN pin. Ground the ACIN pin if a voltage supply is connected to V_{CC}.

BATTERY CHARGER

The LTC4126-ADJ includes a full-featured constant-current (CC)/constant-voltage (CV) linear battery charger with automatic recharge, automatic termination by safety timer, bad battery detection, and out-of-temperature-range charge pausing. Charge current is programmable from 1mA to 50mA via an external resistor at the PROG pin, and the final charge voltage is 4.2V.

The value of the resistor at the PROG pin can be calculated as such:

$$R_{PROG} = \frac{100 \bullet 1.1V}{I_{CHG}} - 2.2k\Omega$$

with I_{CHG} being the desired battery charge current. The minimum and maximum resistances allowed for R_{PROG} are 0Ω and 107kΩ, respectively. Examples of R_{PROG} and I_{CHG} are listed in Table 1.

Table 1. I_{CHG} vs R_{PROG}

R_{PROG}(kΩ)	I_{CHG}(mA)
0	50
8.87	10
52.3	2
107	1

As soon as the voltage at the V_{CC} pin rises 80mV (typical) above the BAT pin voltage, the charger attempts to charge the battery and a new charge cycle is initiated. A 6-hour charge termination timer starts at the beginning of this new charge cycle. When the V_{CC}-to-BAT differential voltage rises above 154mV (typical), the charger enters constant-current (CC) mode and charges the battery at the full programmed current. When the BAT pin approaches the final charge voltage, the charger enters constant-voltage (CV) mode and the charge current begins to drop. The charge current continues to drop while the BAT pin voltage is maintained at the proper charge voltage. This state of CC/CV charging is indicated by a slow blinking LED (typically 1.14Hz) at the $\overline{CHRG}$ pin.

After the 6-hour charge termination timer expires, charging stops completely. Once the charge cycle terminates, the LED at the $\overline{CHRG}$ pin stops blinking and assumes a pull-down state. To start a new charge cycle, remove the power source at ACIN or V_{CC} and reapply it.

Automatic Recharge

After charging has terminated, the charger draws only 3.7µA (typical) from the battery. If it remains in this state long enough, the battery will eventually discharge. To ensure that the battery is always topped off, a new charge cycle automatically begins when the battery voltage falls below V_{RECHRG} (typically 97.5% of the charge voltage). In the event that the battery voltage falls below V_{RECHRG} while the safety timer is still running, the timer will not reset. This prevents the timer from restarting every time the battery voltage dips below V_{RECHRG} during a charging cycle.

OPERATION

Bad Battery Fault

If the battery fails to reach a voltage above V_{RECHRG} by the end of a full charge cycle of 6 hours, the battery is deemed faulty and the LED at the $\overline{CHRG}$ pin indicates this bad battery fault condition by blinking fast (typically 4.58Hz).

Differential Undervoltage Lockout (DUVLO)

A differential undervoltage lockout circuit monitors the differential voltage between V_{CC} and BAT and disables the charger if the V_{CC} voltage falls to within 27mV (typical ΔV_{UVLO}) of the BAT voltage. This condition is indicated by a low on the ACPR pin. Charging does not resume until this difference increases to 80mV at which time the ACPR pin transitions back high. The DC/DC must be enabled for proper ACPR indication.

Differential Undervoltage Current Limit (DUVCL)

The LTC4126-ADJ charger also includes differential undervoltage current limiting (DUVCL) which gradually reduces the charge current from the full programmed current towards zero as the V_{CC}-to-BAT differential voltage drops from approximately 154mV to 116mV. See the curve in the Typical Performance Characteristics section. When the charge current drops below 40% of the full programmed value, the LED at the $\overline{CHRG}$ pin blinks fast (typically 4.58Hz) to indicate the DUVCL fault. In the reverse direction, when the charge current rises above 60% of the full programmed value, the LED at the $\overline{CHRG}$ pin resumes slow blinking to indicate normal operation. Due to the finite hysteresis of the DUVCL comparator, it is possible under a very narrow region of coupling conditions for the LTC4126-ADJ to alternate between slow blinking and fast blinking. This behavior should be construed as operation at near (but not 100%) full charge current.

The DUVCL feature is particularly useful in situations where the wireless power available is limited. Without DUVCL, if the magnetic coupling between the receive coil and the transmit coil is low, DUVLO could be tripped if the charger tried to provide the full charge current. DUVLO forces the charge current to drop to zero instantly, allowing the supply voltage to rise above the DUVLO threshold and switch on the charger again. In the absence of DUVCL, this oscillatory behavior would result in intermittent charging. The DUVCL circuitry prevents this undesirable behavior by gradually increasing or decreasing the charge current as input power becomes more or less available.

Temperature Qualified Charging

The LTC4126-ADJ monitors the battery temperature during the charging cycle by using a negative temperature coefficient (NTC) thermistor, placed close and thermally coupled to the battery pack. If the battery temperature moves outside a safe charging range, the IC suspends charging and signals a fault condition via $\overline{CHRG}$ (blinks fast at 4.58Hz) and the STAT pins until the temperature returns to the safe charging range. The safe charging range is determined by two comparators (Too Hot and Too Cold) that monitor the voltage at the NTC pin as shown in the Block Diagram. The rising threshold of the Too Cold comparator is set to 76.5% of V_{CC} (V_{COLD}) and the falling threshold of the Too Hot comparator is set to 34.9% of V_{CC} (V_{HOT}), each with a hysteresis of 1.5% of V_{CC} around the trip point to prevent oscillation. If the battery charger pauses due to a temperature fault, the 6-hour termination timer also pauses until the thermistor indicates a return to a safe temperature. Grounding the NTC pin disables all NTC functionality. Most Li-Ion battery manufacturers recommend a temperature range of 0°C to 40°C as a safe charging range.

Charge Status Indication via $\overline{CHRG}$, ACPR, and STAT pins

The status of the battery charger is indicated via the open-drain $\overline{CHRG}$ pin as well as by the logic pins STAT1, STAT2, and ACPR according to Table 2. Indication by the logic pins is available only when the DC/DC is enabled.

Table 2. Charger Status Indication

$\overline{CHRG}$	ACPR	STAT1	STAT2	STATUS
Hi-Impedance	0	X	X	Not Charging, No Power, STAT pins indicate Battery Level (see Table 3)
Pulled LOW	1	0	0	Done Charging
Blink Slow (1.14Hz)	1	0	1	Charging
Blink Fast (4.58Hz)	1	1	0	Temperature Fault/Bad Battery
Blink Fast (4.58Hz)	1	1	1	Differential Undervoltage Current Limit (DUVCL)

OPERATION

The open-drain $\overline{CHRG}$ pin has an internal 300µA (typical) pull-down. An LED can be connected between this pin and V_{CC} to indicate the charging status and any fault condition as indicated in the table above. The ACPR, STAT1, and STAT2 pins are digital CMOS logic outputs that can be interpreted by a microprocessor. The low level of these three pins is referenced to GND and the high level is referenced to the OUT pin voltage (typically 1.2V). Hence the status indication via these three pins is only available if the DC/DC converter is turned on via the EN pin or the pushbutton. Status indication via the $\overline{CHRG}$ pin is always available during charging.

DC/DC CONVERTER

To supply the system load from the battery to the OUT pin, the LTC4126-ADJ contains a proprietary low-noise multi-mode charge pump DC/DC converter which can be switched on by applying a minimum voltage of 1.1V to the EN pin or by pressing the pushbutton. The converter can be active simultaneously with the charger. The switching frequency of the charge pump is set to either 50kHz or 75kHz depending on the mode of operation. This frequency is chosen to keep any switching noise out of the audio band.

Modes of Operation

The charge pump DC/DC converter has 3 modes of operation depending on the battery voltage. For $V_{BAT} > 3.6V$, the charge pump operates in 3:1 step-down mode (Mode 1) and provides a regulated 1.2V output. In Mode 1, the maximum output current that the DC/DC converter can provide is limited by internal current limit circuitry to approximately 65mA.

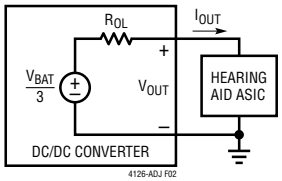


Figure 2. DC/DC Converter Thevenin Equivalent Circuit in Mode 2: 3-to-1 Step-Down

When the battery voltage is between 3.6V and 3.3V, the charge pump still operates in 3:1 step-down mode, but it can no longer maintain 1.2V regulation and provides one-third of the battery voltage at its output (only at no load). This is referred to as Mode 2. The Thevenin equivalent circuit of the converter in Mode 2 is shown in Figure 2, where R_{OL} is the effective open-loop output resistance of the converter. R_{OL} is typically 4.6Ω at room temperature for $V_{BAT} = 3.5V$ and $f_{SW} = 50kHz$. It varies with the battery voltage, the switching frequency of the converter, and the temperature of the die. Figure 2 can be used to determine the output voltage (V_{OUT}) for a specific load current (I_{OUT}) using the following equation:

$$V_{OUT} = \frac{V_{BAT}}{3} - I_{OUT} \bullet R_{OL}$$

When the battery voltage falls below 3.3V, the charge pump switches to 2:1 step-down mode (Mode 3) and again provides a regulated 1.2V output. In Mode 3, the maximum output current that the DC/DC converter can provide decreases with battery voltage but does not fall below approximately 35mA. See the curve in the Typical Performance Characteristics. The variation of the output voltage versus the battery voltage for the various modes of operation is shown in Figure 3.

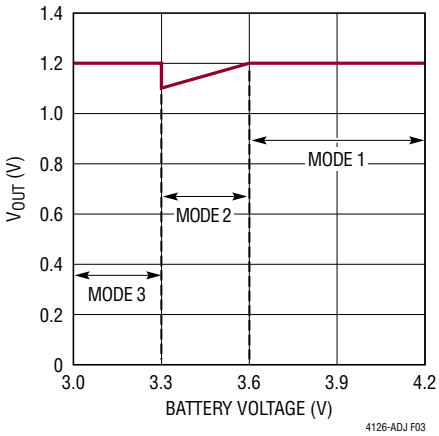


Figure 3. V_{OUT} vs Battery Voltage at $I_{OUT} = 0$

Handling Large Loads

While operating in Mode 1 or Mode 2 (3:1 step-down mode), if a large load at the output causes the output voltage to drop below 1.1V, the converter automatically switches over to Mode 3 (2:1 step-down mode) and attempts to regulate the output at 1.2V. The converter stays in Mode 3 for 110ms (typical) and then returns to the previous mode. If the large load condition persists and V_{OUT} drops below 1.1V again, the converter switches back into Mode 3 for

OPERATION

another 110ms and the cycle continues. The duration of 110ms is chosen to prevent mode switching at a frequency which could fall into the audible range. The switch over to Mode 3 provides more current drive capability at the cost of efficiency and this is why the converter tries to stay in Mode 1 or Mode 2 as much as possible.

Converter Efficiency

The LTC4126-ADJ DC/DC converter efficiency varies throughout the battery voltage range and is very much dependent on the mode it is operating in. The theoretical maximum efficiency in Mode 1 can be expressed as follows:

$$\text{Efficiency, } \eta_{Mode1} = \frac{V_{OUT}}{\left(\frac{V_{BAT}}{3}\right)}$$

If regulation is maintained at the OUT pin at 1.2V, the theoretical maximum efficiency is 85.7% when V_{BAT} = 4.2V and 100% when V_{BAT} = 3.6V as calculated from the above equation.

When the battery voltage is between 3.6V and 3.3V, the converter can no longer maintain a 1.2V regulation at OUT at all loads and is operating in Mode 2. However, the upper limit on the efficiency that the converter can achieve in this mode is determined by switching losses, ohmic losses, and quiescent current loss.

When the battery voltage falls to 3.3V, the converter enters Mode 3 where the theoretical maximum efficiency can be expressed as follows:

$$\text{Efficiency, } \eta_{Mode3} = \frac{V_{OUT}}{\left(\frac{V_{BAT}}{2}\right)}$$

In Mode 3, the theoretical maximum efficiency is 72.7% when V_{BAT} = 3.3V and 80% when V_{BAT} = 3.0V as calculated from the above equation.

Figure 4 shows graphically the variation of the theoretical maximum efficiency of the converter over the range of battery voltages in the three different modes of operation.

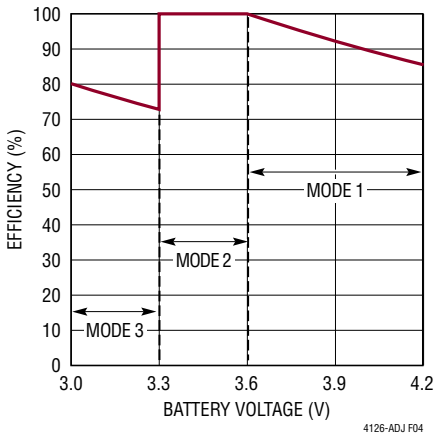


Figure 4. Theoretical Maximum Converter Efficiency vs Battery Voltage

Battery Level Indicator

The LTC4126-ADJ is equipped with a battery voltage monitor which reports various battery voltage levels via the STAT pins when not charging and the converter is enabled. See Table 3. Since the STAT pins indicate either the charger status or the battery levels based on the state of ACPR, there may be a delay of up to 1µs before the STAT pins are valid whenever ACPR changes state.

Table 3. Battery Level Indication

ACPR	STAT1	STAT2	STATUS
0	0	0	V_{BAT} < 3.2V, Low Battery Alert 3
0	0	1	3.2V < V_{BAT} < 3.3V
0	1	0	3.3V < V_{BAT} < 3.6V
0	1	1	V_{BAT} > 3.6V
1	X	X	Power Available, STAT Pins Indicate Charger Status

Battery Disconnect/Ship Mode

When no input power is available and the battery voltage falls to 3.0V (typical), the LTC4126-ADJ shuts down most of its functions to prevent the battery from discharging too deeply, consuming less than 100nA from the battery. Once in battery disconnect mode, normal functioning can only resume when power is applied to the ACIN or V_{CC} pin and the V_{CC} pin voltage rises 80mV (typical) above the BAT pin voltage.

The LTC4126-ADJ is also in battery disconnect mode after initial installation of the battery regardless of its voltage level. This implements the ship mode functionality.

OPERATION

Pushbutton Control

The LTC4126-ADJ is equipped with a pushbutton controller to turn the DC/DC converter on and off if the EN pin is not used (held low). A logic high on the EN pin overrides the pushbutton function and keeps the regulator on. On the falling edge of the EN signal, the DC/DC shuts off and 1µs later, the pushbutton can control the output as long as EN remains low. A push on the pushbutton is considered valid if the $\overline{PBEN}$ pin is held low for at least 425ms (typical). Additionally, the $\overline{PBEN}$ pin needs to return to the high state for at least 43ms (typical) in between successive pushes for a push to be considered valid. An invalid push will not change the state of the converter. A 4MΩ internal resistor pulls up the $\overline{PBEN}$ pin to the BAT voltage. A few different scenarios of valid and invalid pushes are illustrated in Figure 5.

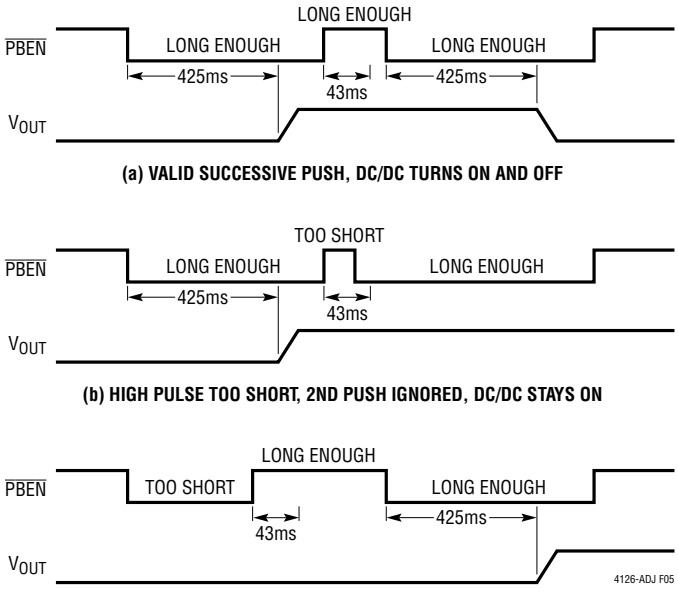


Figure 5. Various Pushbutton Scenarios

APPLICATIONS INFORMATION

WIRELESS POWER TRANSFER

In a wireless power transfer system, power is transmitted using an alternating magnetic field. An AC current in the transmit coil generates a magnetic field. When the receive coil is placed in this field, an AC current is induced in the receive coil. The AC current induced in the receive coil is a function of the applied AC current at the transmitter and the magnetic coupling between the transmit and receive coils. The LTC4126-ADJ internal diode rectifies the AC voltage at the ACIN pin.

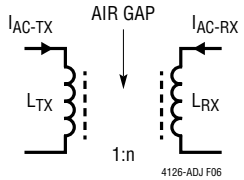


Figure 6. Wireless Power Transfer System

The power transmission range across the air gap as shown in Figure 6 can be improved using resonance by connecting an LC tank to the ACIN pin tuned to the same frequency as the transmit coil AC current frequency.

RECEIVER AND SINGLE TRANSISTOR TRANSMITTER

The single transistor transmitter shown in Figure 7 is an example of a DC/AC converter that can be used to drive AC current into a transmit coil, L_{TX}.

The NMOS, M1, is driven by a 50% duty cycle square wave generated by the LTC6990 oscillator. During the first half of the cycle, M1 is switched on and the current through L_{TX} rises linearly. During the second half of the cycle, M1 is switched off and the current through L_{TX} circulates through the LC tank formed by C_{TX} (= C_{TX1} + C_{TX2}) and L_{TX}. The current through L_{TX} is shown in Figure 8.

If the transmit LC tank frequency is set to 1.29 times the driving frequency, switching losses in M1 are significantly reduced due to zero voltage switching (ZVS). Figure 9 and Figure 10 illustrate the ZVS condition at different $f_{TX-TANK}$ frequencies.

$$f_{TX-TANK} = 1.29 \bullet f_{DRIVE}$$

f_{DRIVE} is set by resistor R_{SET} connected to the LTC6990. $f_{TX-TANK}$ is set by:

$$f_{TX-TANK} = \frac{1}{2 \bullet \pi \sqrt{L_{TX} \bullet C_{TX}}}$$

The peak voltage of the transmit coil, L_{TX}, that appears at the drain of M1 is:

$$V_{TX-PEAK} = 1.038 \bullet \pi \bullet V_{IN}$$

And the peak current through L_{TX} is:

$$I_{TX-PEAK} = \frac{0.36 \bullet V_{IN}}{f_{TX-TANK} \bullet L_{TX}}$$

The RMS current through L_{TX} is:

$$I_{TX-RMS} = 0.66 \bullet I_{TX-PEAK}$$

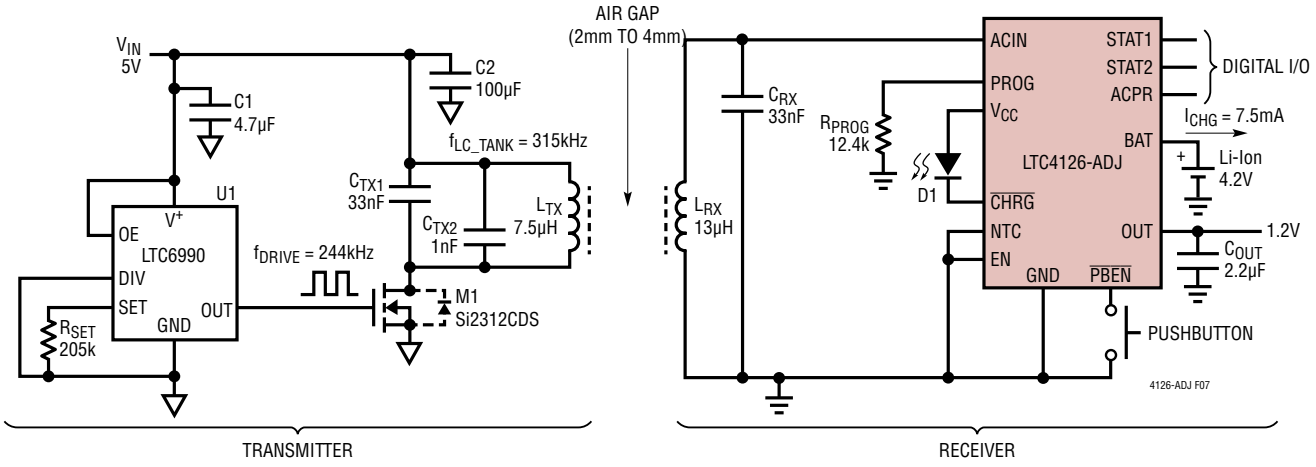


Figure 7. DC/AC Converter, Transmit/Receive Coil, Tuned Resonant LTC4126-ADJ Receiver (See Table 4 and Table 5 for Recommended Components)

APPLICATIONS INFORMATION

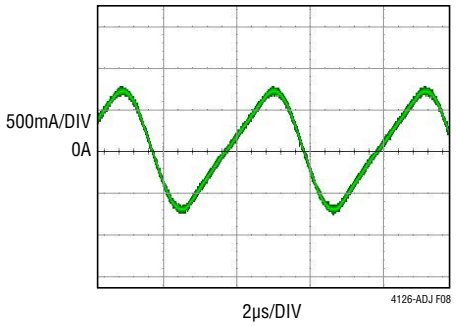


Figure 8. Current Through Transmit Coil

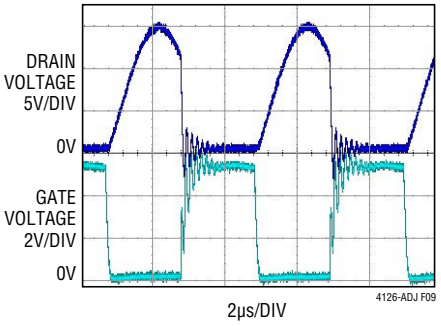


Figure 9. Voltage on the Drain and Gate of NMOS M1 when $f_{TX\_TANK} = f_{DRIVE}$

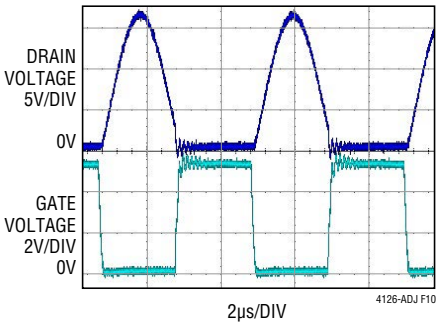


Figure 10. Voltage on the Drain and Gate of NMOS M1 when $f_{TX\_TANK} = 1.29 \bullet f_{DRIVE}$

The LC tank at the receiver, L_{RX} and C_{RX}, is tuned to the same frequency as the driving frequency of the transmit LC tank:

$$f_{RX\text{-}TANK} = f_{DRIVE}$$

where $f_{RX\text{-}TANK}$ is given by,

$$f_{RX-TANK} = \frac{1}{2 \bullet \pi \sqrt{L_{RX} \bullet C_{RX}}}$$

Note that since f_{DRIVE} can be easily adjusted, it is best practice to choose $f_{RX\text{-}TANK}$ using the minimum component count (i.e. C_{RX}) and then adjust f_{DRIVE} to match.

The amount of AC current in the transmit coil can be increased by increasing the supply voltage (V_{IN}). Since the amount of power transmitted is proportional to the AC current in the transmit coil, V_{IN} can be varied to adjust the power delivery to the receive coil.

The overall power transfer efficiency is also dependent on the quality factor (Q) of the components used in the transmitter and receiver circuitry. Select components with low resistance for transmit/receive coils and capacitors.

CHOOSING TRANSMIT POWER LEVEL

As discussed in the previous section, the supply voltage (V_{IN}) can be used to adjust the transmit power of the transmitter shown in Figure 7. Transmit power should be set as low as possible to receive the desired output power under worst-case coupling conditions (e.g. maximum transmit distance with the worst-case misalignment). Although the LTC4126-ADJ is able to shunt excess received power to maintain the V_{CC} voltage in the desired range, it has the adverse effect of raising the die temperature and possibly the battery temperature, and if the battery temperature exceeds the Too Hot temperature threshold set by the thermistor, the charger pauses charging the battery.

Using the rated current of the transmit inductor to set an upper limit, transmit power should be adjusted downward until charge current is negatively impacted under worst-case coupling conditions. Once the transmit power level is determined, the transmit and receive coils should be arranged under best-case coupling conditions with a fully-charged battery or a battery simulator to make sure that the shunting of excess power does not raise the die temperature too much.

In addition to temperature, another parameter that needs to be checked is the maximum negative voltage on the ACIN pin. Following the procedure above, when evaluating the rise in temperature of the LTC4126-ADJ under the best-case coupling conditions, ensure that $V_{CC} - V_{ACIN}$ does not exceed 16V. Figure 11 shows a typical waveform on ACIN showing $V_{CC} - V_{ACIN} < 16V$.

APPLICATIONS INFORMATION

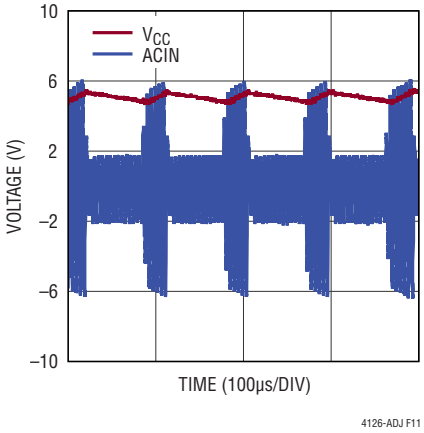


Figure 11. Typical Acceptable Voltage Waveform on the ACIN Pin with $V_{CC} - V_{ACIN} < 16V$.

As an alternative to using the empirical method to determine the maximum negative voltage on the ACIN pin, the following formula can be used in conjunction with Figure 12, which shows a parallel resonant configuration on the receiver:

$$|V_{RX}| = \frac{\omega k \sqrt{L_{TX} L_{RX}}}{\sqrt{\left(1-\omega^2 L_{RX} C_{RX}\right)^2 + \left(\omega \frac{L_{RX}}{R_{L-AC}}\right)}} |I_{TX}|$$

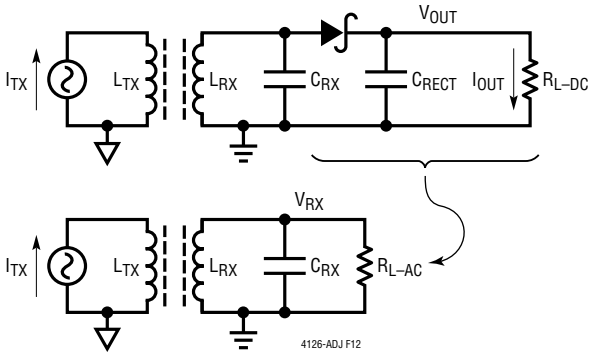


Figure 12. Modeling Parallel Resonant Configuration and Half Wave Rectifier on the Receiver

$|V_{RX}|$ is the amplitude of the voltage on the receiver coil, $|I_{TX}|$ is the amplitude of the current in the transmit coil, k is the coupling factor between the transmit and receive coils, ω is the operating frequency in radians per second, L_{TX} is the self-inductance of the transmit coil, L_{RX} is the self-inductance of the receive coil, C_{RX} is the receiver resonant capacitance and R_{L-AC} is the equivalent AC load resistance.

One simplification is as follows:

$$R_{L-AC} \approx \frac{R_{L-DC}}{2}$$

which assumes that the drop across the Schottky diode is much smaller than the amplitude $|V_{RX}|$. Additionally, R_{L-DC} can be approximated as the ratio of the output voltage (V_{OUT}) to the output current (I_{OUT}):

$$R_{L-DC} = \frac{V_{OUT}}{I_{OUT}}$$

The amplitude of the current in the transmit coil $|I_{TX}|$ can be either measured directly or its initial (no receiver) value can be calculated based on the transmitter circuit. This initial value is a conservative estimate since the amplitude of the transmitter coil current will drop as soon as the receiver, with a load, is coupled to it.

The coupling factor (k) between the two coils could be obtained by running a finite element simulation inputting the coil dimensions and physical configurations. An easier method to obtain this coupling number, is to use the series-aiding and series-cancelling measurement method for two loosely coupled coils as shown in Figure 13.

And:

$$L_{AIDING} = L_{AB}$$

$$L_{CANCELLING} = L_{CD}$$

$$k = \frac{L_{AIDING} - L_{CANCELLING}}{4\sqrt{L_{TX} L_{RX}}}$$

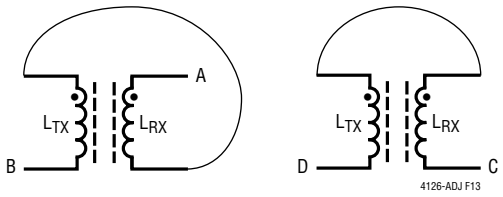


Figure 13. Series-Aiding and Series-Cancelling Method Configurations Used for Measuring the Coupling Factor k

APPLICATIONS INFORMATION

SINGLE TRANSISTOR TRANSMITTER AND LTC4126-ADJ RECEIVER-DESIGN EXAMPLE

The example in Figure 7 illustrates the design of the resonant coupled single transistor transmitter and LTC4126-ADJ charger. The steps needed to complete the design are reviewed as follows.

1. Determine the receiver resonant frequency and set component values for the receiver LC tank:

   It is best practice to select a resonant frequency that yields a low component count. In this example, 244kHz is selected as the receiver resonant frequency. At 244kHz, the tank capacitance (C_{RX}) required with the selected receive coil (13µH) is 33nF. Since 33nF is a standard value for capacitors, the tank capacitance requires only one component. The tank capacitance calculation is shown below.

   $$C_{RX} = \frac{1}{4 \bullet \pi^2 \bullet f^2_{RX-TANK} \bullet L_{RX}} = 32.7nF \simeq 33nF$$

   Select a 33nF capacitor with a minimum voltage rating of 25V and 5% (or better) tolerance for C_{RX}. A higher voltage rating usually corresponds to a higher quality factor which is preferable. However, the higher the voltage rating, the larger the package size usually is.

2. Set the driving frequency (f_{DRIVE}) for the single transistor transmitter:

   f_{DRIVE} is set to the same value as the receiver resonant frequency:

   $$R_{SET} = \frac{1MHz}{N_{DIV}} \bullet \frac{50k\Omega}{244kHz} = 205k\Omega$$

   where N_{DIV} = 1 as the DIV pin of the LTC6990 is grounded. Select a 205kΩ (standard value) resistor with 1% tolerance. For more information regarding the oscillator, consult the LTC6990 data sheet.

3. Set the LC tank component values for the single transistor transmitter: If f_{DRIVE} is 244kHz, the transmit LC tank frequency ($f_{TX-TANK}$) is:

   $f_{TX-TANK}$ = 1.29 • 244kHz = 315kHz

   The transmit coil (L_{TX}) used in the example is 7.5µH. The value of transmit tank capacitance (C_{TX}) can be calculated:

   $$C_{TX} = \frac{1}{4 \bullet \pi^2 \bullet f^2_{TX-TANK} \bullet L_{TX}} = 34nF$$

   Since 34nF is not a standard capacitor value, use a 33nF capacitor in parallel with a 1nF capacitor to obtain a value within 1% of the calculated C_{TX}. The recommended rating for C_{TX} capacitors is 50V with 5% (or better) tolerance.

4. Verify that the AC current through the transmit coil is well within its rating. In this example, the supply voltage to the single transistor transmitter is 5V. The peak AC current through the transmit (L_{TX}) coil can be calculated as:

   $$I_{TX-PEAK} = \frac{0.36 \bullet V_{IN}}{f_{TX-TANK} \bullet L_{TX}} = \frac{0.36 \bullet 5V}{315kHz \bullet 7.5\mu H} = 0.76A$$

   and the RMS current as:

   I_{TX-RMS} = 0.66 • 0.76A = 0.5A

   The rated current for the transmit coil is 1.55A (see the Wurth 760308103206 data sheet for more information). So the I_{TX-RMS} calculated is well below the rated current.

5. Also verify that the transmit power level chosen does not result in excessive heating of the LTC4126-ADJ.

COMPONENT SELECTION FOR TRANSMITTER AND RECEIVER

To ensure optimum performance from the LTC4126-ADJ, use the components listed in Table 4 and Table 5 for the receiver and transmitter, respectively, as shown in Figure 7. Select receive and transmit coils with good quality factors to improve the overall power transmission efficiency. Use a ferrite core to improve the magnetic coupling between the transmit and receive coils and to shield the rest of the transmit and receive circuitry from the AC magnetic field. Capacitors with low ESR and low thermal coefficients such as C0G ceramics should be used in the transmit and receive LC tanks.

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Table 4. Recommended Components for the Receiver Shown in Figure 7

ITEM	PART DESCRIPTION	MANUFACTURER/PART NUMBER
L_{RX}	Receive Coil, 13µH, 10mm	Wurth 760308101208
C_{RX}	Capacitor, C0G, 33nF, ±5%, 50V, 0805 or	TDK C2012C0G1H333J125AA
	Capacitor, C0G, 33nF, ±5%, 50V, 1206	Murata GCM3195C1H333JA16D
C_{OUT}	Capacitor, X5R, 2.2uF, ±10%, 6.3V, 0402	Murata GRM155R60J225KE95D
D1	LED, 620nm, Red, 0603, SMD	Rohm Semiconductor SML-311UTT86

Table 5. Recommended Components for the Transmitter Shown in Figure 7

ITEM	PART DESCRIPTION	MANUFACTURER/PART NUMBER
L_{TX}	Transmit Coil, 7.5µH, 28mm × 15mm	Wurth 760308103206
C_{TX1}	Capacitor, C0G, 33nF, ±5%, 50V, 0805	TDK C2012C0G1H333J125AA
C_{TX2}	Capacitor, C0G, 1nF, ±5%, 50V, 0603	TDK C1608C0G1H102J080AA
M1	MOSFET, N-CH 20V, 6A, SOT-23-3	Vishay Si2312CDS-T1-GE3
R_{SET}	Resistor, 205kΩ, ±1%, 1/16W, 0402	Vishay CRCW0402205KFKED
U1	IC, Voltage Controlled Silicon Oscillator, 2mm × 3mm DFN	Analog Devices LTC6990IDCB
C1	Capacitor, X5R, 4.7µF, ±20%, 6.3V, 0402	TDK C1005X5R0J475M
C2	Capacitor, X5R, 100µF, ±20%, 6.3V, 1206	Murata GRM31CR60J107ME39L

COMPONENT SELECTION FOR $\overline{CHRG}$ STATUS INDICATOR

The LED connected at the $\overline{CHRG}$ pin is powered by a 300µA (typical) pull-down current source. Select a high efficiency LED with a low forward voltage drop. Some recommended LEDs are shown in Table 6.

Table 6. Recommended LEDs

MANUFACTURER/ PART NUMBER	PART DESCRIPTION
Rohm Semiconductor, SML-311UTT86	LED, 620nm, RED, 0603, SMD
Lite-On Inc., LTST-C193KRKT-5A	LED, RED, 0603, SMT

Temperature Qualified Charging

To use the battery temperature qualified charging feature, connect an NTC thermistor, R_{NTC}, between the NTC pin and GND, and a bias resistor, R_{BIAS}, from the V_{CC} pin to the NTC pin (Figure 14). Since the Too Hot comparator threshold in the LTC4126-ADJ is internally set to 34.9% of V_{CC}, the resistance of the thermistor at the hot threshold, R_{HOT}, can be computed using the following equation:

$$\frac{R_{HOT}}{R_{HOT} + R_{BIAS}} = 0.349$$

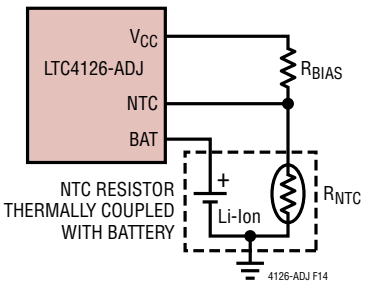

Figure 14. NTC Thermistor Connection

This can be simplified as:

$$\frac{R_{HOT}}{R_{BIAS}} = 0.536$$

If R_{BIAS} is chosen to have a value equal to the value of the chosen NTC thermistor at 25°C (R_{25}), then R_{HOT}/R_{25} = 0.536. Thermistor manufacturers usually publish resistance/temperature conversion tables for their thermistors and list the ratio of the resistance, R_T, of the thermistor at any given temperature, T, to its resistance, R_{25}, at 25°C. For the Vishay thermistor NTCS0402E3104*HT with β25/85 = 3950k, the ratio R_T/R_{25} = 0.536 corresponds to approximately 40°C.

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Similarly, since the Too Cold comparator threshold in the LTC4126-ADJ is internally set to 76.5% of V_{CC}, the resistance of the thermistor at the cold threshold, R_{COLD}, can be computed using the following equation:

$$\frac{R_{COLD}}{R_{COLD}+R_{BIAS}} = 0.765$$

This can be simplified as:

$$\frac{R_{COLD}}{R_{BIAS}} = 3.25$$

Again, if R_{BIAS} is chosen to have a value equal to the value of the chosen NTC thermistor at 25°C (R_{25}), then R_{COLD}/R_{25} = 3.25. For the same Vishay thermistor with β25/85 = 3950k, the ratio R_T/R_{25} = 3.25 corresponds to approximately 0°C.

The hot/cold temperature thresholds can be increased or decreased by choosing an R_{BIAS} value which is not the same as R_{25}. For example, if a hot temperature threshold of 50°C is desired, consult the resistance/temperature conversion table of the thermistor to find the ratio R_{50}/R_{25}. For the same Vishay thermistor used above, this ratio is 0.3631. Since R_{HOT}/R_{BIAS} = 0.536, R_{BIAS} can be calculated as follows:

$$R_{BIAS} = \frac{R_{HOT}}{0.536} = \frac{0.3631 \bullet R_{25}}{0.536} = 0.677 \bullet R_{25}$$

This means: choose an R_{BIAS} value which is 67.7% of the value of the thermistor at 25°C to set the hot temperature threshold to 50°C. However, this will automatically shift the cold temperature threshold upward too. The cold temperature threshold can be recalculated by computing the R_{COLD}/R_{25} ratio as follows:

$$\frac{R_{COLD}}{R_{25}} = \frac{R_{COLD}}{R_{BIAS}} \bullet \frac{R_{BIAS}}{R_{25}} = 3.25 \bullet 0.677 = 2.202$$

From the conversion table, this ratio corresponds to about 8°C. Note that changing the value of R_{BIAS} to be smaller than R_{25} moves both the hot and cold thresholds higher. Similarly, R_{BIAS} with a value greater than R_{25} will move both the hot and cold thresholds lower. Also note that with only one degree of freedom (i.e. adjusting the value of R_{BIAS}), the user can only set either the cold or hot threshold but not both.

It is possible to adjust the hot and cold threshold independently by introducing another resistor as a second degree of freedom (Figure 15). The resistor R_D in effect reduces the sensitivity of the resistance between the NTC pin and ground. Therefore, intuitively this resistor will move the hot threshold to a hotter temperature and the cold threshold to a colder temperature. The value of R_{BIAS} and R_D can now be set according to the following formula:

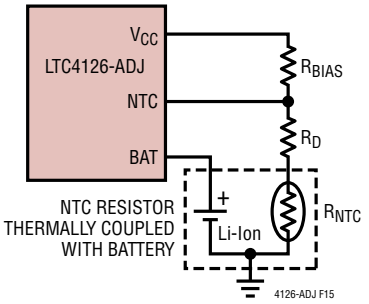

Figure 15. NTC Thermistor Connection with Desensitizing Resistor R_D

$$R_{BIAS} = \frac{(R_{COLD} - R_{HOT})}{2.714}$$

$$R_D = 0.197 \bullet R_{COLD} - 1.197 \bullet R_{HOT}$$

Note that this method can only be used to push the hot and cold temperature thresholds apart from each other. When using the formulas above, if the user finds that a negative value is needed for R_D, the two temperature thresholds selected are too close to each other and a higher sensitivity thermistor is needed. For example, this method can be

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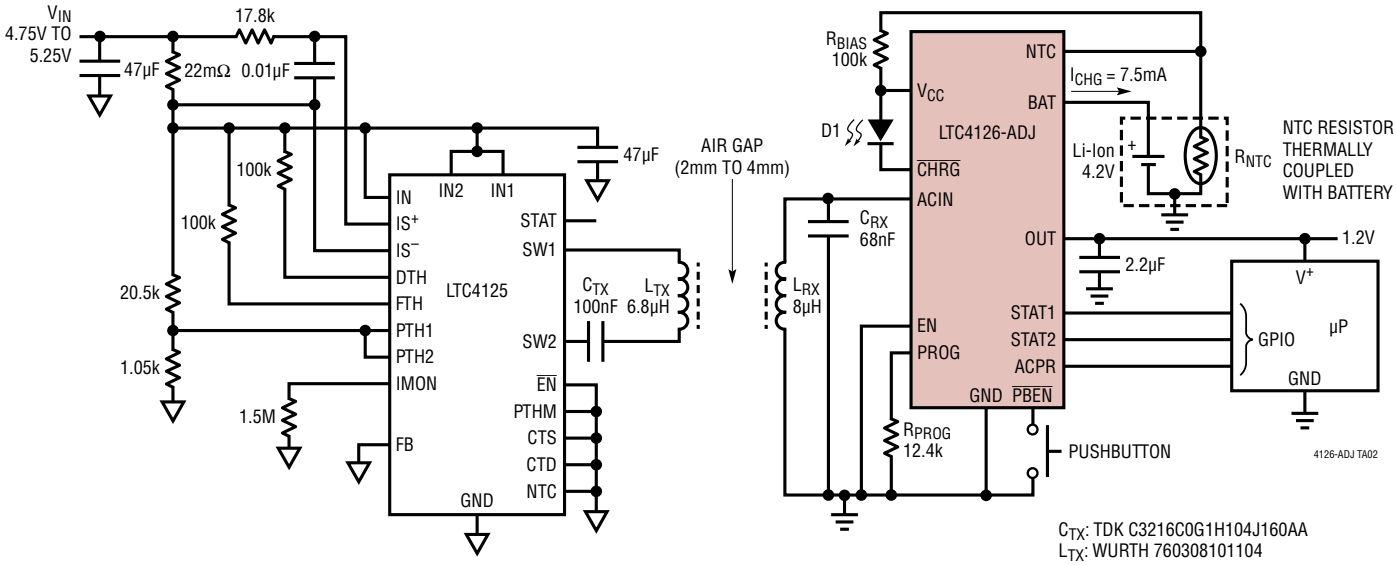
used to set the hot and cold thresholds independently to 60°C and –5°C. Using the same Vishay thermistor with β25/85 = 3950k whose nominal value at 25°C is 100k, the formula results in R_{BIAS} = 147k and R_D = 52.3k for the closest 1% resistor values.

PC BOARD LAYOUT CONSIDERATIONS

Since the exposed pad of the LTC4126-ADJ package is the only ground pin and serves as the return path for both the charger and the DC/DC converter, it must be soldered to the PC board ground for a good electrical connection. Although the LTC4126-ADJ is a low power IC, the shunt circuitry in the AC power control block can cause a fair amount of on-chip power dissipation if the available AC power is excessive. If the heat is not dissipated properly on the PC board, the temperature of the die and subsequently, the temperature of the battery may rise above the hot temperature threshold set by the NTC thermistor causing the charger to pause charging. For optimum thermal performance, there should be a group of vias directly under the exposed pad on the backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (Layer 2).

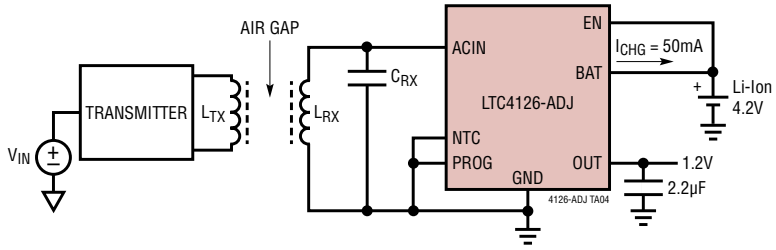
TYPICAL APPLICATIONS

Full-Featured Application Circuit

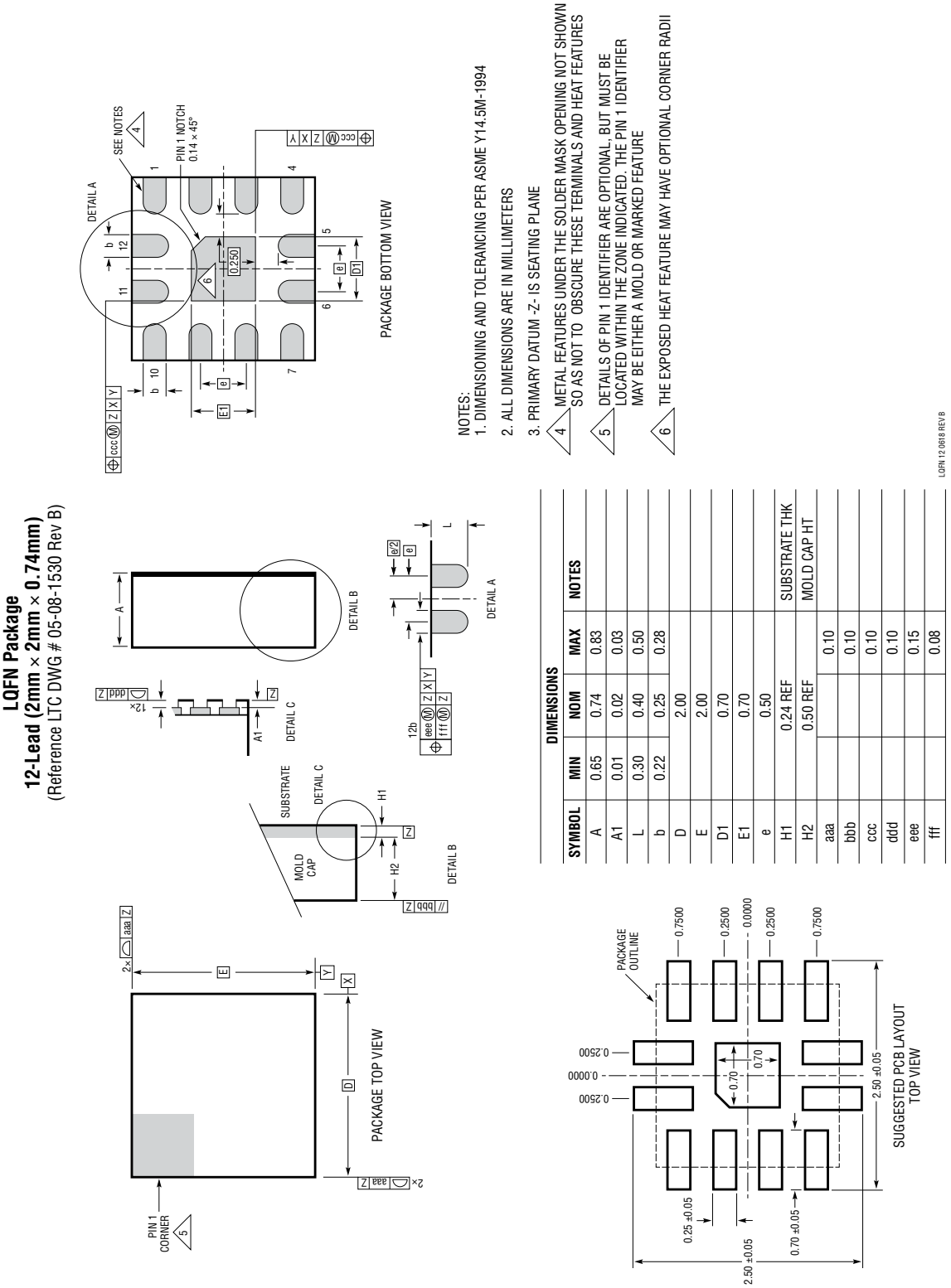


C_{TX}: TDK C3216C0G1H104J160AA
L_{TX}: WURTH 760308101104
R_{NTC}: VISHAY NTCS0402E3104JHT
D1: ROHM SEMICONDUCTOR SML-311UTT86
C_{RX}: AVX 0603YC683JAT2A
L_{RX}: SUNLORD MQQRC060630S8R0

Minimum Component Count Application Circuit

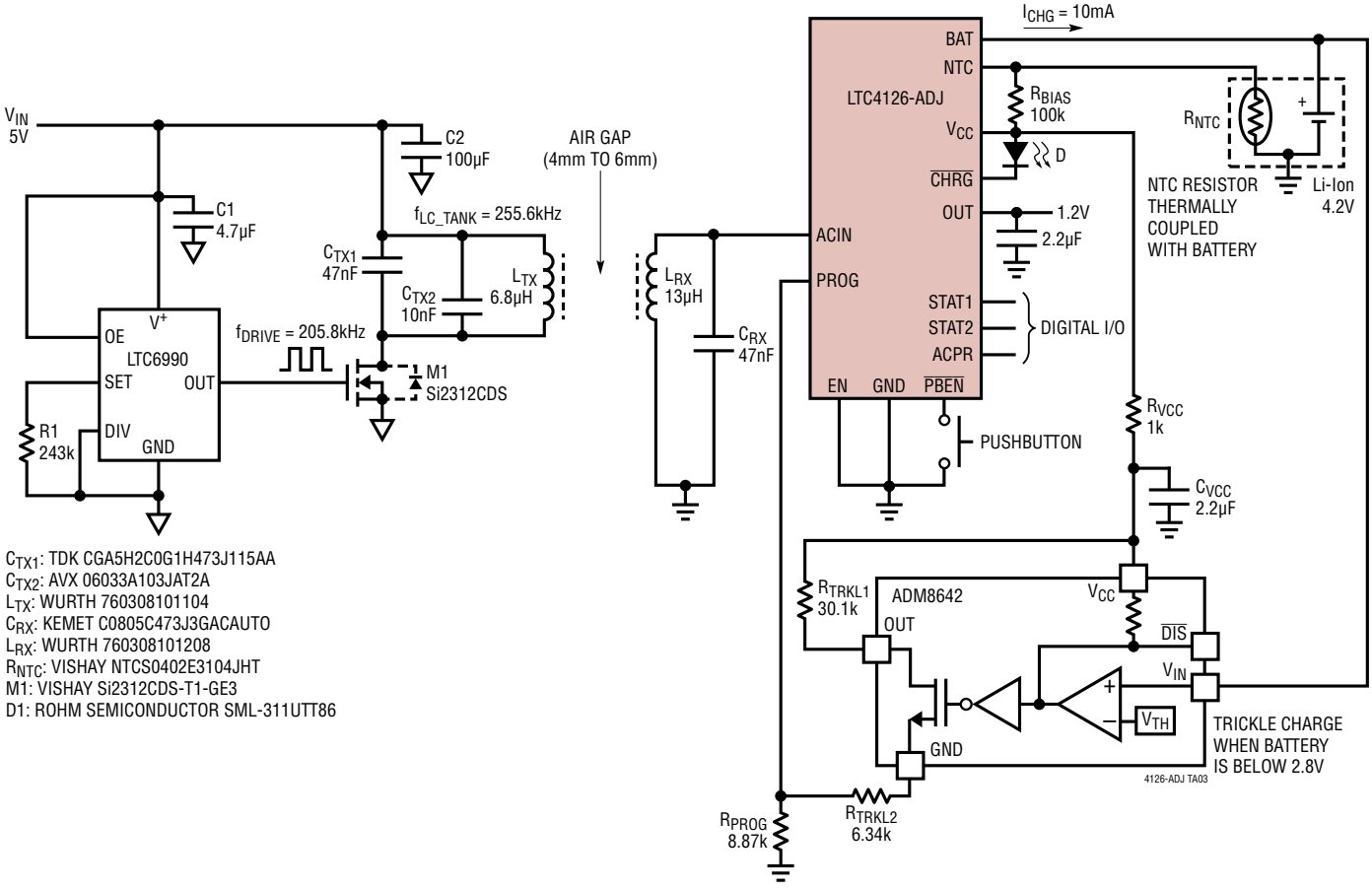


PACKAGE DESCRIPTION



TYPICAL APPLICATION

Wireless 10mA Li-Ion Battery Charger (4.2V) Tuned at 204kHz with Pushbutton Enabling and C/10 Trickle Charging Function



C_{TX1}: TDK CGA5H2C0G1H473J115AA
C_{TX2}: AVX 06033A103JAT2A
L_{TX}: WURTH 760308101104
C_{RX}: KEMET C0805C473J3GACAUTO
L_{RX}: WURTH 760308101208
R_{NTC}: VISHAY NTCS0402E3104JHT
M1: VISHAY Si2312CDS-T1-GE3
D1: ROHM SEMICONDUCTOR SML-311UTT86

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4120	400mA Wireless Power Receiver Buck Battery Charger	Wireless 1 to 2 Cell Li-Ion Charger, 400mA Charge Current, Dynamic Harmonization Control, Wide Input Range: 12.5V to 40V, 16-Lead 3mm × 3mm QFN Package
LTC4123	Low Power Wireless Charger for Hearing Aids	Wireless Single NiMH Charger, Integrated Rectifier with Overvoltage Limit, 25mA Charge Current, Zn-Air Detect, Temperature Compensated Charge Voltage, 6-Lead 2mm × 2mm DFN Package
LTC4124	100mA Wireless Li-Ion Charger with Low Battery Disconnect	Wireless Single Li-Ion Charger with PowerPath™, Pin-Selectable Charge Current: 10mA/25mA/50mA/100mA, Pin-Selectable Charge Voltage: 4.0V/4.1V/4.2V/4.35V, 12-Lead 2mm × 2mm QFN Package
LTC4125	5W Auto Resonant Wireless Power Transmitter	Monolithic Auto Resonant Full Bridge Driver, Transmit Power Automatically Adjusts to Receiver Load, Foreign Object Detection, Wide Operating Switching Frequency Range: 50kHz to 250kHz, Input Voltage Range 3V to 5.5V, 20-Lead 4mm × 5mm QFN Package
LTC4126/ LTC4126-10	7.5mA/10mA Wireless Li-Ion Charger with 1.2V Step-Down DC/DC Converter	Wireless Single Li-Ion Charger, Integrated Rectifier with Overvoltage Limit, 7.5mA/10mA Charge Current, Pin Selectable Float Voltages (LTC4126: 4.2V, 4.35V/LTC4126-10: 4.1V, 4.2V), 12-Lead 2mm × 2mm QFN Package
LTC6990	TimerBlox: Voltage Controlled Silicon Oscillator	Fixed-Frequency or Voltage-Controlled Operation, Frequency Range of 488Hz to 2MHz, Low-Profile SOT-23 and 2mm × 3mm DFN Packages
LTC6992	TimerBlox: Voltage Controlled Pulse-Width Modulator (PWM)	Pulse Width Modulation by 0V to 1V Analog Input, Frequency Range of 3.81Hz to 1MHz, Low-Profile SOT-23 and 2mm × 3mm DFN Packages