## FEATURES

Operates with 3.3 V supply
EIA RS-422 and RS-485 compliant over full CM range
$19 \mathrm{k} \Omega$ input impedance
Up to 50 transceivers on bus
20 Mbps data rate
Short circuit protection
Specified over full temperature range
Thermal shutdown
Interoperable with 5 V logic
$840 \mu$ A supply current
2 nA shutdown current
Also available in TSSOP package
Meets IEC1000-4-4 (>1 kV)
8 ns skew
Upgrade for MAX 3491, SN75ALS180

## APPLICATIONS

## Telecommunications

DTE-DCE interface
Packet switching
Local area networks
Data concentration
Data multiplexers
Integrated services digital network (ISDN)

## AppleTalk

Industrial controls

## GENERAL DESCRIPTION

The ADM3491 is a low power, differential line transceiver designed to operate using a single 3.3 V power supply. Low power consumption, coupled with a shutdown mode, makes it ideal for power-sensitive applications. It is suitable for communication on multipoint bus transmission lines.

## FUNCTIONAL BLOCK DIAGRAM



Figure 1.
The ADM3491 is intended for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. It contains a differential line driver and a differential line receiver, making it suitable for full-duplex data transfer.

The input impedance is $19 \mathrm{k} \Omega$, allowing up to 50 transceivers to be connected on the bus. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state, if a significant temperature increase is detected in the internal driver circuitry during fault conditions.

The receiver contains a fail-safe feature that results in a logic high output state, if the inputs are unconnected (floating).

The ADM3491 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology.

The ADM3491 is fully specified over the industrial temperature range and is available in DIP and SOIC packages, as well as the space-saving TSSOP package.

## Rev. A

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## ADM3491

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## SPECIFICATIONS

$\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$. All specifications $\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted.
Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRIVER |  |  |  |  |  |
| Differential Output Voltage, Vod | 2.0 |  |  | V | $\mathrm{RL}=100 \Omega$, Figure 4, $\mathrm{V}_{\text {cc }}>3.1 \mathrm{~V}$ |
|  | 1.5 |  |  | V | $\mathrm{RL}=54 \Omega$, Figure 4 |
|  | 1.5 |  |  | V | $\mathrm{RL}=60 \Omega$, Figure 5, $-7 \mathrm{~V}<\mathrm{V}_{\text {TST }}<+12 \mathrm{~V}$ |
| $\Delta\left\|V_{\text {ool }}\right\|$ for Complementary Output States |  |  | 0.2 | V | $\mathrm{R}=54 \Omega$ or $100 \Omega$, Figure 4 |
| Common-Mode Output Voltage, Voc |  |  | 3 | V | $\mathrm{R}=54 \Omega$ or $100 \Omega$, Figure 4 |
| $\Delta \mid$ Voc for Complementary Output States |  |  | 0.2 | V | $\mathrm{R}=54 \Omega$ or $100 \Omega$, Figure 4 |
| CMOS Input Logic Threshold Low, $\mathrm{V}_{\text {INL }}$ |  |  | 0.8 | V |  |
| CMOS Input Logic Threshold High, Vinh | 2.0 |  |  | V |  |
| Logic Input Current (DE, DI, $\overline{\mathrm{RE}}$ ) |  |  | $\pm 1.0$ | $\mu \mathrm{A}$ |  |
| Output Leakage (Y, Z) Current |  |  | $\pm 3$ | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{o}}=-7 \mathrm{~V}$ or $+12 \mathrm{~V}, \mathrm{~V}_{\text {cc }}=0 \mathrm{~V}$ or 3.6 V |
| Output Short-Circuit Current |  |  | $\pm 250$ | mA | $\mathrm{V}_{0}=-7 \mathrm{~V}$ or +12 V |
| RECEIVER |  |  |  |  |  |
| Differential Input Threshold Voltage, $\mathrm{V}_{\text {TH }}$ | -0.2 |  | +0.2 | V | $-7 \mathrm{~V}<\mathrm{V}_{\text {cm }}<+12 \mathrm{~V}$ |
| Input Voltage Hysteresis, $\Delta \mathrm{V}_{\text {TH }}$ |  | 50 |  | mV | $\mathrm{V}_{\mathrm{cm}}=0 \mathrm{~V}$ |
| Input Resistance | 12 | 19 |  | $\mathrm{k} \Omega$ | $-7 \mathrm{~V}<\mathrm{V}_{\text {cm }}<+12 \mathrm{~V}$ |
| Input Current (A, B) |  |  | 1 | mA | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}$ |
|  |  |  | -0.8 | mA | $\mathrm{V}_{\mathrm{IN}}=-7 \mathrm{~V}$ |
| Logic Enable Input Current ( $\overline{\mathrm{RE}})$ |  |  | $\pm 1$ | $\mu \mathrm{A}$ |  |
| Output Voltage Low, Vol |  |  | 0.4 | V | $\mathrm{l}_{\text {lut }}=2.5 \mathrm{~mA}$ |
| Output Voltage High, V OH | V cc -0.4 V |  |  | V | lout $=-1.5 \mathrm{~mA}$ |
| Short-Circuit Output Current |  |  | $\pm 60$ | mA | $\mathrm{V}_{\text {OUt }}=\mathrm{GND}$ or $\mathrm{V}_{\text {cc }}$ |
| Three-State Output Leakage Current |  |  | $\pm 1.0$ | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {CC }}=3.6 \mathrm{~V}, 0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<\mathrm{V}_{\text {cC }}$ |
| POWER SUPPLY CURRENT |  |  |  |  |  |
| Icc |  |  |  |  | Outputs unloaded |
|  |  | 0.84 | 1.5 | mA | $D E=V_{C C}, \overline{\mathrm{RE}}=0 \mathrm{~V}$ |
|  |  | 0.84 | 1.5 | mA | $\mathrm{DE}=0 \mathrm{~V}, \overline{\mathrm{RE}}=0 \mathrm{~V}$ |
| Supply Current in Shutdown |  | 0.002 | 1 | $\mu \mathrm{A}$ | $\mathrm{DE}=0 \mathrm{~V}, \overline{\mathrm{RE}}=\mathrm{V}_{\mathrm{cc}}$ |

## ADM3491

## TIMING SPECIFICATIONS

$\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Table 2.

| Parameter | Min | Typ | Max | Unit | Test Conditions/ Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRIVER |  |  |  |  |  |
| Differential Output Delay, TDD | 1 |  | 35 | ns | $\mathrm{R}_{\mathrm{L}}=60 \Omega, \mathrm{C}_{L 1}=\mathrm{C}_{L 2}=15 \mathrm{pF}$, Figure 8 |
| Differential Output Transition Time | 1 | 8 | 15 | ns | $\mathrm{R}_{\mathrm{L}}=60 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 8 |
| Propagation Delay Input to Output, $\mathrm{T}_{\text {PLH }}$, TPHL | 7 | 22 | 35 | ns | $\mathrm{R}_{\mathrm{L}}=27 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 9 |
| Driver Output to Output, $\mathrm{T}_{\text {skew }}$ |  |  | 8 | ns | $\mathrm{R}_{\mathrm{L}}=54 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 9 |
| ENABLE/DISABLE |  |  |  |  |  |
| Driver Enable to Output Valid |  | 45 | 90 | ns | $\mathrm{RL}_{\mathrm{L}}=110 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Figure 6 |
| Driver Disable Timing |  | 40 | 80 | ns | $\mathrm{R}_{\mathrm{L}}=110 \Omega, C_{L}=50 \mathrm{pF}$, Figure 6 |
| Driver Enable from Shutdown |  | 650 | 110 | ns | $\mathrm{R}_{\mathrm{L}}=110 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, Figure 6 |
| RECEIVER |  |  |  |  |  |
| Time to Shutdown | 80 | 190 | 300 | ns |  |
|  | 25 | 65 | 90 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, Figure 11 |
| Skew, $\mathrm{TPLH}^{-} \mathrm{T}_{\text {PHL }}$ |  |  | 10 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, Figure 11 |
| Receiver Enable, $\mathrm{T}_{\text {EN }}$ |  | 25 | 50 | ns | $C_{L}=15 \mathrm{pF}$, Figure 7 |
| Receiver Disable, Tden |  | 25 | 45 | ns | $C_{L}=15 \mathrm{pF}$, Figure 7 |
| Receiver Enable from Shutdown |  |  | 500 | ns | $C_{L}=15 \mathrm{pF}$, Figure 7 |

$\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$.
Table 3.

| Parameter | Min | Typ | Max | Unit | Test Conditions/ Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRIVER |  |  |  |  |  |
| Differential Output Delay, $\mathrm{T}_{\text {DD }}$ | 1 |  | 70 | ns | $\mathrm{R}_{\mathrm{L}}=60 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 8 |
| Differential Output Transition Time | 2 | 8 | 15 | ns | $\mathrm{R}_{\mathrm{L}}=60 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 8 |
| Propagation Delay Input to Output, $\mathrm{T}_{\text {PLH, }}, \mathrm{T}_{\text {PHL }}$ | 7 | 22 | 70 | ns | $\mathrm{R}_{\mathrm{L}}=27 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 9 |
| Driver Output to Output, $\mathrm{T}_{\text {skew }}$ |  |  | 10 | ns | $\mathrm{RL}_{\mathrm{L}}=54 \Omega, \mathrm{C}_{\mathrm{L} 1}=\mathrm{C}_{\mathrm{L} 2}=15 \mathrm{pF}$, Figure 9 |
| ENABLE/DISABLE |  |  |  |  |  |
| Driver Enable to Output Valid |  | 45 | 110 | ns | $R_{L}=110 \Omega, C_{L}=50 \mathrm{pF}$, Figure 6 |
| Driver Disable Timing |  | 40 | 110 | ns | $\mathrm{R}_{L}=110 \Omega, C_{L}=50 \mathrm{pF}$, Figure 6 |
| Driver Enable from Shutdown |  | 650 | 110 | ns | $\mathrm{R}_{\mathrm{L}}=110 \Omega, C_{L}=15 \mathrm{pF}$, Figure 6 |
| RECEIVER |  |  |  |  |  |
| Time to Shutdown | 50 | 190 | 500 | ns |  |
| Propagation Delay Input to Output, $\mathrm{T}_{\text {PLH, }}, \mathrm{T}_{\text {PHL }}$ | 25 | 65 | 115 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, Figure 11 |
| Skew, TPLH - T PHL |  |  | 20 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, Figure 11 |
| Receiver Enable, Ten |  | 25 | 50 | ns | $C_{L}=15 \mathrm{pF}$, Figure 7 |
| Receiver Disable, TDEN |  | 25 | 50 | ns | $C_{L}=15 \mathrm{pF}$, Figure 7 |
| Receiver Enable from Shutdown |  |  | 600 | ns | $C_{L}=15 \mathrm{pF}$, Figure 7 |

## ABSOLUTE MAXIMUM RATINGS

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.

Table 4.

| Parameter | Min |
| :---: | :---: |
| $V_{\text {cc }}$ | 7 V |
| Inputs |  |
| Driver Input (DI) | -0.3 V to $\mathrm{V}_{\text {cc }}+0.3 \mathrm{~V}$ |
| Control Inputs ( $\mathrm{DE}, \overline{\mathrm{RE} \text { ) }}$ | -0.3 V to $\mathrm{V}_{\text {cc }}+0.3 \mathrm{~V}$ |
| Receiver Inputs (A, B) | -7.5 V to +12.5 V |
| Outputs |  |
| Driver Outputs | -7.5 V to +12.5 V |
| Receiver Output | -0.5 V to $\mathrm{V}_{\mathrm{cc}}+0.5 \mathrm{~V}$ |
| 14-Lead DIP, Power Dissipation | 800 mW |
| $\theta_{\text {JA, }}$, Thermal Impedance | $140^{\circ} \mathrm{C} / \mathrm{W}$ |
| 14-Lead SOIC, Power Dissipation | 650 mW |
| $\theta_{\mathrm{JA}}$, Thermal Impedance | $115^{\circ} \mathrm{C} / \mathrm{W}$ |
| 16-Lead TSSOP, Power Dissipation | 500 mW |
| $\theta_{\mathrm{JA}}$, Thermal Impedance | $158^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range Industrial (A Version) | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 s ) | $300^{\circ} \mathrm{C}$ |
| Vapor Phase (60 s) | $215^{\circ} \mathrm{C}$ |
| Infrared (15 s) | $220^{\circ} \mathrm{C}$ |
| ESD Rating | >2 kV |
| EFT Rating (IEC1000-4-4) | $>1 \mathrm{kV}$ |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance

WARNING!
WARNING:

## ADM3491

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 2. DIP/SOIC Pin Configuration


Figure 3. TSSOP Pin Configuration

Table 5. Pin Function Descriptions

| Pin Number |  | Mnemonic | Description |
| :---: | :---: | :---: | :---: |
| DIP/ SOIC | TSSOP |  |  |
| 1,8 | 2, 7, 9, 10, 13, 16 | NC | No Connect. |
| 2 | 3 | RO | Receiver Output. High when A > B by 200 mV ; low when A < B by 200 mV . |
| 3 | 4 | $\overline{\mathrm{RE}}$ | Receiver Output Enable. When $\overline{\mathrm{RE}}$ is low, the receiver output RO is enabled. When $\overline{\mathrm{RE}}$ is high, the output is high impedance. If $\overline{\mathrm{RE}}$ is high and DE is low, the ADM3491 enters a shutdown state. |
| 4 | 5 | DE | Driver Output Enable. A high level enables the driver differential outputs, Y and Z. A low level places the part in a high impedance state. |
| 5 | 6 | DI | Driver Input. When the driver is enabled, a logic low on DI forces $Y$ low and $Z$ high; a logic high on DI forces Y high and Z low. |
| 6,7 | 8 | GND | Ground Connection, 0 V . |
| 9 | 11 | Y | Noninverting Driver Output Y. |
| 10 | 12 | Z | Inverting Driver Output Z. |
| 11 | 14 | B | Inverting Receiver Input B. |
| 12 | 15 | A | Noninverting Receiver Input A. |
| 13, 14 | 1 | $\mathrm{V}_{\text {cc }}$ | Power Supply, $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$. |

## TEST CIRCUITS



Figure 4. Driver Voltage Measurement Test Circuit


Figure 5. Driver Enable/Disable Test Circuit


Figure 6. Driver Differential Output Delay Test Circuit


Figure 7. Driver/Receiver Propagation Delay Test Circuit


Figure 8. Driver Voltage Measurement Test Circuit 2


Figure 9. Receiver Enable/Disable Test Circuit


Figure 10. Driver Propagation Delay Test Circuit


Figure 11. Receiver Propagation Delay Test Circuit

## ADM3491

## SWITCHING CHARACTERISTICS



Figure 12. Driver Propagation Delay, Rise/Fall Timing


Figure 13. Receiver Propagation Delay


Figure 14. Driver Enable/Disable Timing


Figure 15. Receiver Enable/Disable Timing

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 16. Receiver Output Low Voltage vs. Output Current


Figure 17. Receiver Output Low Voltage vs. Temperature


Figure 18. Driver Differential Output Voltage vs. Output Current


Figure 19. Receiver Output High Voltage vs. Output Current


Figure 20. Receiver Output High Voltage vs. Temperature


Figure 21. Driver Differential Output Voltage vs. Temperature

## ADM3491



Figure 22. Supply Current vs. Temperature


Figure 23. Driving 100 ft . Cable L-H Transition


Figure 24. Driving 100 ft. Cable H-L Transition


Figure 25. Shutdown Current vs. Temperature

## APPLICATIONS INFORMATION

## DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals, which appear as common-mode voltages on the line.

The two main standards approved by the Electronics Industries Association (EIA) specify the electrical characteristics of transceivers used in differential data transmission:

- RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft . A single driver can drive a transmission line with up to 10 receivers.
- RS-485 standard was defined to cater to true multipoint communications. This standard meets or exceeds all the requirements of RS-422, but also allows multiple drivers and receivers to be connected to a single bus. An extended common-mode range of -7 V to +12 V is defined.

The most significant differentiator of the RS-485 standard is that the drivers can be disabled, thereby allowing more than one to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Table 6. Comparison of RS-422 and RS-485 Interface Standards

| Specification | RS-422 | RS-485 |
| :--- | :--- | :--- |
| Transmission Type | Differential | Differential |
| Maximum Cable Length | 4000 ft. | 4000 ft. |
| Minimum Driver Output Voltage | $\pm 2 \mathrm{~V}$ | $\pm 1.5 \mathrm{~V}$ |
| Driver Load Impedance | $100 \Omega$ | $54 \Omega$ |
| Receiver Input Resistance | $4 \mathrm{k} \Omega \mathrm{min}$ | $12 \mathrm{k} \Omega \mathrm{min}$ |
| Receiver Input Sensitivity | $\pm 200 \mathrm{mV}$ | $\pm 200 \mathrm{mV}$ |
| Receiver Input Voltage Range | -7 V to +7 V | -7 V to +12 V |

## CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM3491 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 26. Only one driver can transmit at a particular time, but multiple receivers can be enabled simultaneously.

As with any transmission line, it is important that reflections be minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

## RECEIVER OPEN-CIRCUIT FAIL-SAFE FEATURE

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.


Figure 26. ADM3491 Full-Duplex Data Link

Table 7. Transmitting Truth Table

| Transmitting |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| Inputs |  | Outputs |  |  |
| $\overline{\mathbf{R E}}$ | $\mathbf{D E}$ | DI | $\mathbf{Z}$ | Y |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| 0 | 0 | X | Hi-Z | Hi-Z |
| 1 | 0 | X | $\mathrm{Hi}-\mathrm{Z}$ | $\mathrm{Hi}-\mathrm{Z}$ |

Table 8. Receiving Truth Table

| Receiving |  |  |  |
| :--- | :--- | :--- | :--- |
| Inputs |  |  | Outputs |
| $\overline{\mathbf{R E}}$ | $\mathbf{D E}$ | $\mathbf{A - B}$ | RO |
| 0 | X | $>+0.2 \mathrm{~V}$ | 0 |
| 0 | X | $<-0.2 \mathrm{~V}$ | 0 |
| 0 | X | Inputs O/C | 1 |
| 1 | X | X | $\mathrm{Hi}-\mathrm{Z}$ |

## OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 27. 14-Lead Plastic DIP
( $\mathrm{N}-14$ )
Dimensions shown in inches and (millimeters)


COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 28. 14-Lead Narrow Body Small Outline (SOIC)
(R-14)
Dimensions shown in inches and (millimeters)


Figure 29. 16-Lead Thin Shrink Small Outline (TSSOP) (RU-16)
Dimensions shown in inches and (millimeters)

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Options |
| :--- | :--- | :--- | :--- |
| ADM3491AN | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Plastic DIP | $\mathrm{N}-14$ |
| ADM3491AR | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Narrow Body Small Outline (SOIC) | R-14 |
| ADM3491AR-REEL | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Narrow Body Small Outline (SOIC) | R-14 |
| ADM3491AR-REEL7 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Narrow Body Small Outline (SOIC) | R-14 |
| ADM3491ARZ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Narrow Body Small Outline (SOIC) | R-14 |
| ADM3491ARZ-REEL ${ }^{1}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Narrow Body Small Outline (SOIC) | R-14 |
| ADM3491ARZ-REEL7 ${ }^{1}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 14-Lead Narrow Body Small Outline (SOIC) | R-14 |
| ADM3491ARU | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16-Lead Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADM3491ARU-REEL | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16-Lead Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADM3491ARU-REEL7 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16-Lead Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADM3491ARUZ $^{1}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16-Lead Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADM3491ARUZ-REEL $^{1}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16-Lead Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADM3491ARUZ-REEL7 ${ }^{1}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16-Lead Thin Shrink Small Outline (TSSOP) | RU-16 |

${ }^{1} \mathrm{Z}=\mathrm{Pb}$-free part.

## ADM3491

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## ADM3491

## NOTES

