1.1 Scope.

This specification covers the detail requirements of CMOS monolithic analog multiplexers ADG526A and ADG527A with 16 channels and dual 8 channels, respectively. These multiplexers also feature high switching speeds, low R_{ON} and on-chip latches to facilitate microprocessor interfacing. Break-Before-Make switching is guaranteed.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	ADG526AT(X)/883B
−2	ADG527AT(X)/883B

NOTE
[1]To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Terminal LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C)

V+ to V− ..... 44 V
V+ to GND ..... 25 V
V− to GND ..... −25 V
Analog Inputs
  Voltage at S, D ..... V− to V+
  Continuous Current, S or D ..... 30 mA
  Pulsed Current S or D
    1 ms Duration, 10% Duty Cycle ..... 70 mA
Digital Inputs
  Voltages at IN ..... V− −4 V to V+ +4 V or 20 mA, Whichever Occurs First
Power Dissipation (Package)
  Up to +75°C ..... 470 mW/°C
  Derates above +75°C by ..... 6 mW°C
Operating Temperature ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature (T_J) ..... +175°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-28 and E-28A
θ_{JA} = 120°C/W for Q-28 and E-28A

ADG526A/ADG527A—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Test Condition[1]/Comments	Units
Switch ON Resistance	R_{DS}	−1, 2	400	300	400	V_D = +10 V; V_S = −10 V; I_{DS} = 1 mA; Test Circuit 1	Ω max
		−1, 2	600	450	600	V+ = +10.8 V; V− = −10.8 V; Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	−1, 2	50	1	50	V+ = +16.5 V; V− = −16.5 V; Test Circuit 2	±nA max
Drain OFF Leakage Current	I_D (OFF)	−1	200	1	200	V_D = V_S = ±10 V; V+ = +16.5 V; V− = −16.5 V; Test Circuit 3	±nA max
		−2	100	1	100		
Channel ON Leakage Current	I_D (ON)	−1	200	1	200	V_D = V_S = ±10 V; V+ = +16.5 V; V− = −16.5 V; Test Circuit 4	±nA max
		−2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	−2	25		25	V1 = ±10 V; V2 = ±10 V; Test Circuit 5	nA max
Digital Input High Voltage	V_{INH}	−1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	−1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	−1, 2	1	1	1	V+ = +16.5 V; V− = −16.5 V; V_{IN} = +16.5 V	±μA max
Low Level Input Current	I_{INL}	−1, 2	1	1	1	V+ = +16.5 V; V− = −16.5 V; V_{IN} = 0 V	±μA max
Supply Current	$+I_{CC}$	−1, 2	1.5	1	1.5	V+ = +16.5 V; V− = −16.5 V; V_{INH} = 2.4 V; V_{INL} = 0.8 V	mA max
	$-I_{CC}$	−1, 2	0.2	0.1	0.2		
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	−1, 2	400			V1 = ±10 V; V2 = ±10 V; Test Circuit 6	ns max
Subgroup 9, 10, 11 t_{ON} (ENABLE, $\overline{WRITE}$)	t_{ON} (EN, $\overline{WR}$)	−1, 2	400			Test Circuit 7a, 7b, 7c	ns max
t_{OFF} (ENABLE, $\overline{RESET}$)	t_{OFF} (EN, $\overline{RS}$)	−1, 2	400				
Subgroup 12 Off Isolation	V_{ISO}	−1, 2	50			R_L = 1 kΩ; C_L = 12 pF; V_{IN} = 20 V pk–pk, f = 100 kHz; T_A = +25°C; Test Circuit 8	dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	−1, 2	60			V_S = 20 V pk–pk; R_L = 1 kΩ; C_L = 12 pF; T_A = +25°C; Test Circuit 9	dB min
Subgroup 14 Charge Injection	Q_{INJ}	−1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	−1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	−1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	−1	100				pF max
		−2	50				

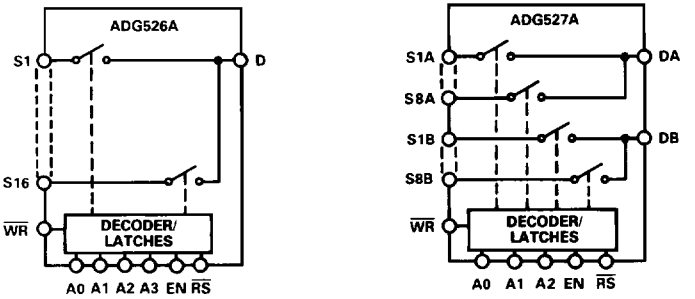
NOTE: DUAL SUPPLY OPERATION – ±15 V
[1]Unless otherwise noted V+ = +15 V; V− = −15 V.

Table 2.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Test Condition[1]/Comments	Units
Switch ON Resistance	R_{DS}	−1, 2	1000	700	1000	V_D = +10 V; V_S = 0 V; I_{DS} = 0.5 mA V+ = +10.8 V; V− = 0 V; Test Circuit 1	Ω max
Source OFF Leakage Current	I_S (OFF)	−1, 2	50	1	50	V+ = +16.5 V; V− = 0 V; Test Circuit 2	±nA max
Drain OFF Leakage Current	I_D (OFF)	−1	200	1	200	V+ = +16.5 V; V− = 0 V; V1 = +10 V/0 V; V2 = 0 V/+10 V; Test Circuit 3	±nA max
		−2	100	1	100		
Channel ON Leakage Current	I_D (ON)	−1	200	1	200	V+ = +16.5 V; V− = 0 V; V1 = +10 V/0 V; V2 = 0 V/+10 V; Test Circuit 4	±nA max
		−2	100	1	100		
Differential OFF Output Leakage	I_{DIFF}	−2	25		25	V+ = +16.5 V; V− = 0 V; V1 = +10 V/0 V; V2 = 0 V/+10 V; Test Circuit 5	±nA max
Digital Input High Voltage	V_{INH}	−1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	−1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	−1, 2	1	1	1	V+ = +16.5 V; V− = 0 V; V_{IN} = +16.5 V	±μA max
Low Level Input Current	I_{INL}	−1, 2	1	1	1	V+ = +16.5 V; V− = 0 V; V_{IN} = 0 V	±μA max
Supply Current	$+I_{CC}$	−1, 2	1.5	1.5	1.5	V+ = +16.5 V; V− = 0 V; V_{INH} = 2.4 V; V_{INL} = 0.8 V	mA max
Subgroup 9, 10, 11 $t_{TRANSITION}$	t_{TRANS}	−1, 2	600			V1 = 10 V/0 V; V2 = 0 V/10 V; Test Circuit 6	ns max
Subgroup 9, 10, 11 t_{ON} (ENABLE, $\overline{WRITE}$)	t_{ON} (EN, $\overline{WR}$)	−1, 2	600			Test Circuit 7a, 7b, 7c	ns max
t_{OFF} (ENABLE, $\overline{RESET}$)	t_{OFF} (EN, $\overline{RS}$)	−1, 2	600				
Subgroup 12 Off Isolation	V_{ISO}	−1, 2	50				dB min
Subgroup 13 Crosstalk between Channels	V_{CT}	−1, 2	60				dB min
Subgroup 14 Charge Injection	Q_{INJ}	−1, 2	50			Test Circuit 10	pC max
Digital Input Capacitance	C_{IN}	−1, 2	20				pF max
Source Capacitance, OFF	C_S (OFF)	−1, 2	20				pF max
Drain Capacitance, OFF	C_D (OFF)	−1	100				pF max
		−2	50				

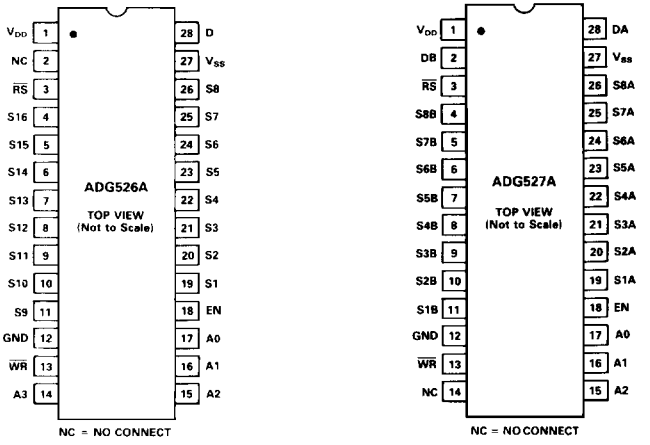
NOTE: SINGLE SUPPLY OPERATION – +15 V
[1]Unless otherwise noted V+ = +15 V; V− = 0 V.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

DIP



LCC

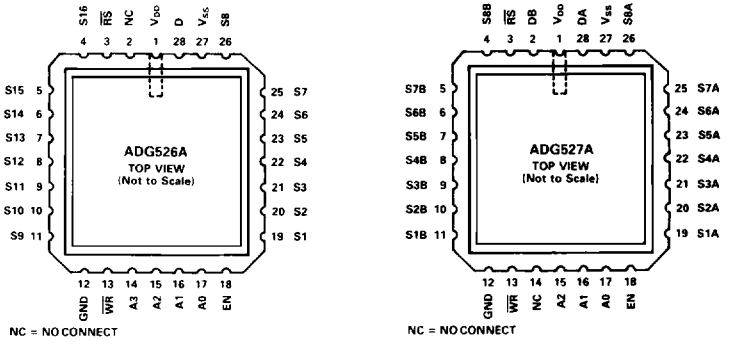


Table 3.

MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10**, 11**
Group C End Point Electrical Parameters, Method 5005	1

NOTES
*Indicates PDA applies to Subgroup 1.
**Subgroups 10 & 11, if not tested, shall be guaranteed to the limits in the data sheet.

Table 4. ADG526A Truth Table

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X		1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

X = Don't Care

Table 5. ADG527A Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X		1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

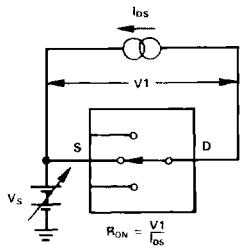
X = Don't Care

3.2.4 Microcircuit Technology Group.

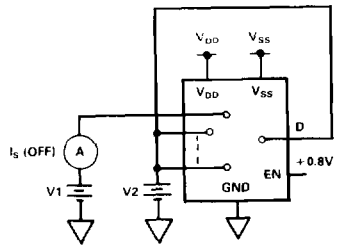
This microcircuit is covered by technology group (82).

4.2.1 Life Test/Burn-In Circuit.

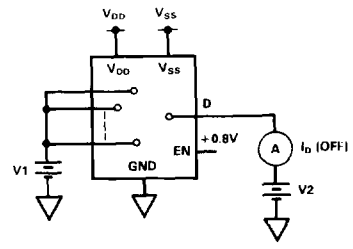
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B). Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.



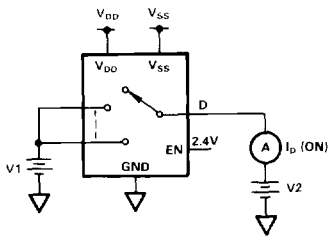
Test Circuit 1
R_{ON}



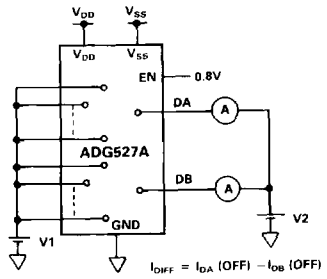
Test Circuit 2
I_S (OFF)



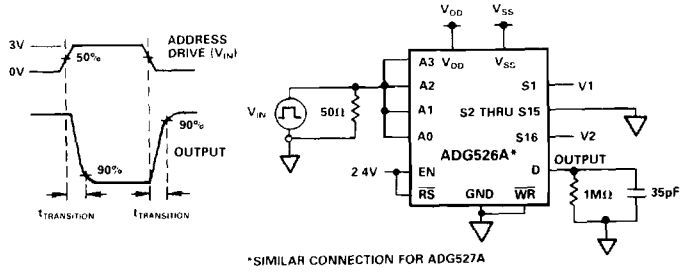
Test Circuit 3
I_D (OFF)



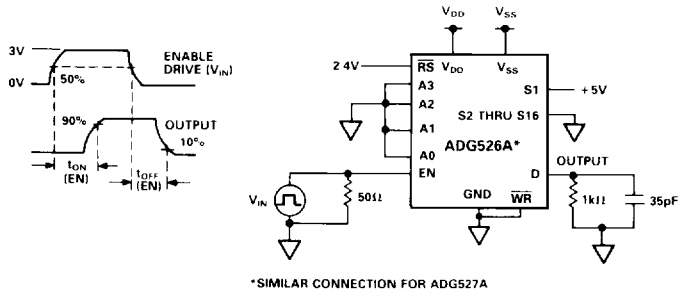
Test Circuit 4
I_D (ON)



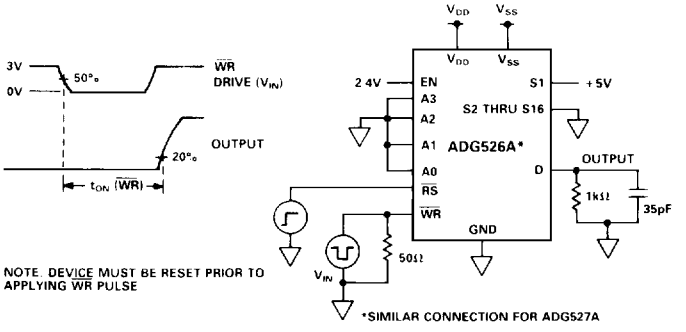
Test Circuit 5
I_{DIFF}



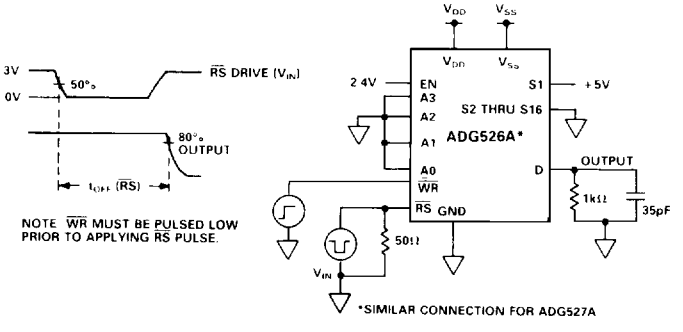
Test Circuit 6
Switching Time of Multiplexer, $t_{TRANSITION}$



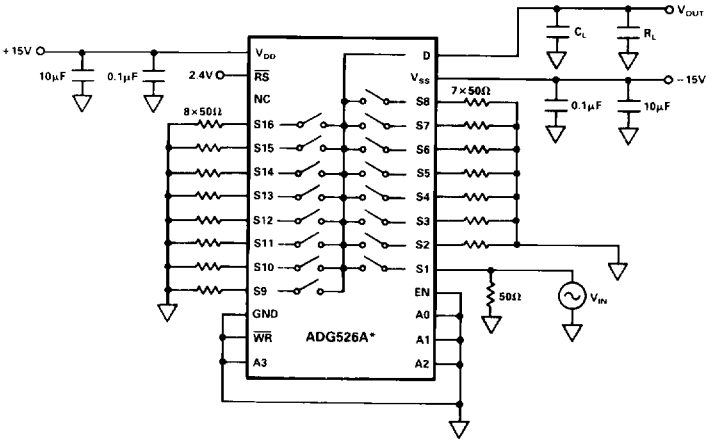
Test Circuit 7a
Enable Delay, t_{ON} (EN), t_{OFF} (EN)



Test Circuit 7b
Write Turn-On Time, t_{ON} (WR)



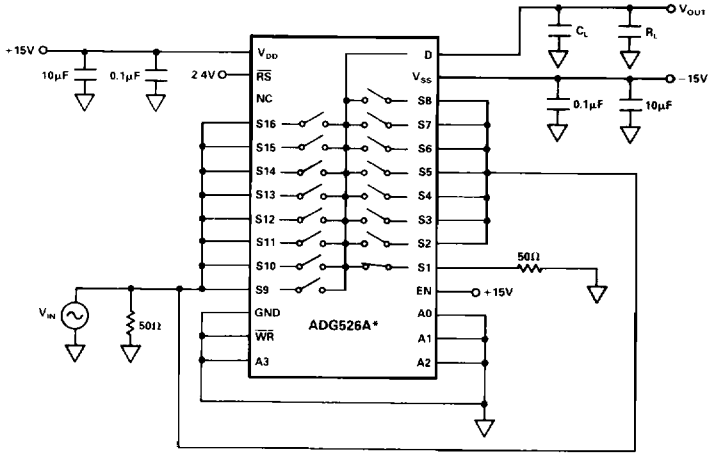
Test Circuit 7c
Reset Turn-Off Time, t_{OFF} (RS)



*SIMILAR TYPE OF CIRCUIT APPLIES FOR ADG527A.

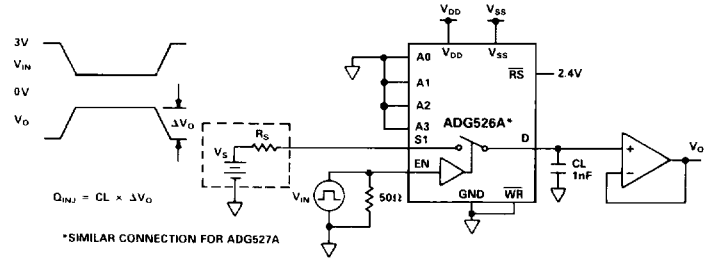
NC = NO CONNECT

Test Circuit 8
OFF Isolation



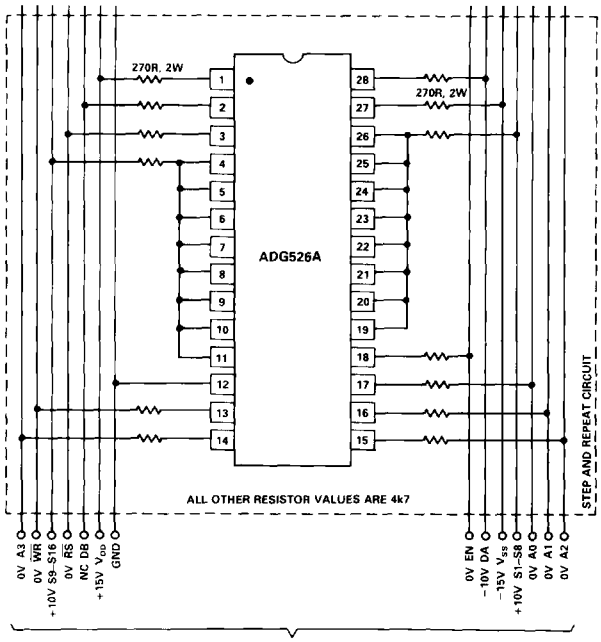
*SIMILAR CIRCUIT APPLIES FOR ADG527A

Test Circuit 9
Crosstalk Between Channels



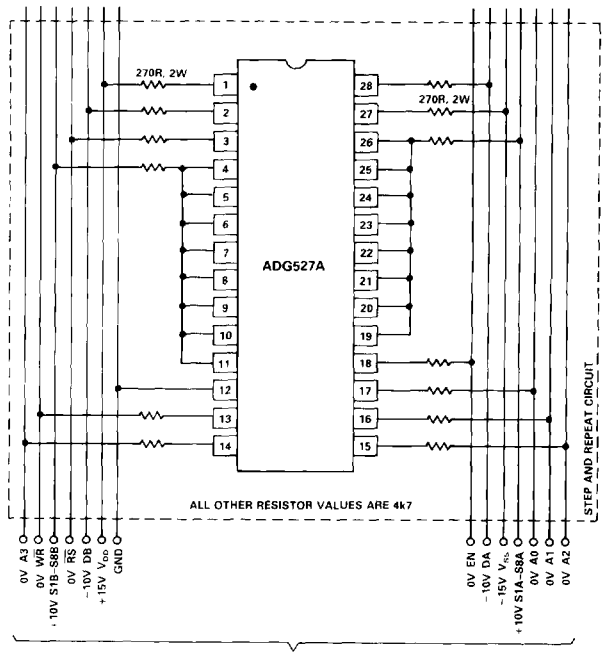
*SIMILAR CONNECTION FOR ADG527A

Test Circuit 10
Charge Injection



NOTES
A0, A1, A2, A3, $\overline{WR}$, $\overline{RS}$, AND EN EACH HAVE ONE OFF 100k RESISTOR TO GND AT BOARD EDGE
THE POWER UP SEQUENCE IS AS FOLLOWS: APPLY GND; A0, A1, A2, A3, $\overline{WR}$, $\overline{RS}$ EN; V_{DD}, V_{SS}; DA; S1–S16.
NC = NO CONNECT

ADG526A Edge Connections



NOTES
A0, A1, A2, A3, $\overline{WR}$, $\overline{RS}$, AND EN EACH HAVE ONE OFF 100k RESISTOR TO GND AT BOARD EDGE
THE POWER UP SEQUENCE IS AS FOLLOWS: APPLY GND; A0, A1, A2, EN, $\overline{WR}$, $\overline{RS}$; V_{DD}, V_{SS}; S1A–S8A, S1B–S8B.

ADG527A Edge Connections