



Low-Voltage, Quad, SPST CMOS Analog Switches

MAX4610/MAX4611/MAX4612

General Description

The MAX4610/MAX4611/MAX4612 are quad, low-voltage, single-pole/single-throw (SPST) analog switches. On-resistance (100Ω, max) is matched between switches to 4Ω, max and is flat (4Ω, max) over the specified signal range. Each switch handles V+ to GND analog signal levels. Maximum off-leakage current is only 1nA at T_A = +25°C and 2nA at T_A = +85°C.

The MAX4610 has four normally open (NO) switches, and the MAX4611 has four normally closed (NC) switches. The MAX4612 has two NO switches and two NC switches. These CMOS switches operate from a single +2V to +12V supply. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

Applications

- Battery-Operated Equipment
- Audio/Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Sample-and-Hold Circuits
- Communication Circuits

Features

- ◆ Offered in Automotive Temperature Range (-40°C to +125°C)
- ◆ Guaranteed On-Resistance
100Ω max (5V Supply)
46Ω max (12V Supply)
- ◆ Guaranteed Match Between Channels (4Ω, max)
- ◆ Guaranteed Flatness Over Signal Range (18Ω, max)
- ◆ Off-Leakage Current Over Temperature
< 2nA at T_A = +85°C
- ◆ > 2kV ESD Protection per Method 3015.7
- ◆ Rail-to-Rail Signal Handling
- ◆ TTL/CMOS-Logic Compatible

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4610CUD	0°C to +70°C	14 TSSOP	U14-1
MAX4610CSD	0°C to +70°C	14 Narrow SO	S14-2
MAX4610CPD	0°C to +70°C	14 Plastic DIP	P14-6
MAX4610C/D	0°C to +70°C	Dice*	—
MAX4610EGE	-40°C to +85°C	16 QFN-EP**	G1644-1
MAX4610EUD	-40°C to +85°C	14 TSSOP	U14-1
MAX4610ESD	-40°C to +85°C	14 Narrow SO	S14-2
MAX4610EPD	-40°C to +85°C	14 Plastic DIP	P14-6
MAX4610ASD	-40°C to +125°C	14 Narrow SO	S14-2

Ordering Information continued at end of data sheet.

*Contact factory for dice specifications.

**EP = Exposed pad.

Pin Configurations/Truth Tables

TOP VIEW

TSSOP/SO/DIP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

QFN

MAX4611/MAX4612 Pin Configurations/Truth Tables appear at end of data sheet.

**EP = EXPOSED PAD
CONNECT EP TO V+

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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V+	-0.3V to +13V
IN_, COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current (any terminal) (pulsed at 1ms, 10% duty cycle)	20mA
Peak Current (any terminal) (pulsed at 1ms, 10% duty cycle)	40mA
ESD per Method 3015.7	> 2kV

Continuous Power Dissipation (T_A = +70°C)

14-Pin TSSOP (derate 6.3mW/°C above +70°C)	500mW
14-Pin Narrow SO (derate 8.00mW/°C above +70°C) ..	640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..	800mW
16-Pin QFN (derate 18.5mW/°C above +70°C)	1481mW

Operating Temperature Ranges

MAX461_C_	0°C to +70°C
MAX461_E_	-40°C to +85°C
MAX461_A_	-40°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO_, NC_, COM_, or IN_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH						
Analog Signal Range (Note 3)	V _{COM_} , V _{NO_} , V _{NC_}		0		V+	V
On-Resistance	R _{ON}	V+ = 4.5V, I _{COM_} = 1mA, V _{NO_} = V _{NC_} = 3V	T _A = +25°C	70	100	Ω
			T _A = T _{MIN} to T _{MAX}		150	
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V+ = 4.5V, I _{COM_} = 1mA, V _{NO_} = V _{NC_} = 3V	T _A = +25°C	1.0	4	Ω
			T _A = T _{MIN} to T _{MAX}		8	
On-Resistance Flatness (Note 5)	R _{FLAT(ON)}	V+ = 4.5V; I _{COM_} = 1mA; V _{NO_} = V _{NC_} = 3V, 2V, 1V	T _A = +25°C	12	18	Ω
			T _A = T _{MIN} to T _{MAX}		25	
NO_ or NC_ Off-Leakage Current (Note 6)	I _{NO(OFF)}	V+ = 5.5V; V _{COM_} = 1V, 4.5V; V _{NO_} = 4.5V, 1V	T _A = +25°C	-0.1	+0.1	nA
			T _A = -40°C to +85°C	-2	+2	
			T _A = -40°C to +125°C	-30	+30	
COM_ Off-Leakage Current (Note 6)	I _{COM(OFF)}	V+ = 5.5V; V _{COM_} = 1V, 4.5V; V _{NO_} = V _{NC_} = 4.5V, 1V	T _A = +25°C	-0.1	+0.1	nA
			T _A = -40°C to +85°C	-2	+2	
			T _A = -40°C to +125°C	-30	+30	
COM_ On-Leakage Current (Note 6)	I _{COM(ON)}	V+ = 5.5V; V _{COM_} = 1V, 4.5V; V _{NO_} = V _{NC_} = 1V, 4.5V, or floating	T _A = +25°C	-0.2	+0.2	nA
			T _A = -40°C to +85°C	-4	+4	
			T _A = -40°C to +125°C	-30	+30	

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MAX4610/MAX4611/MAX4612

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT						
Input Current with Input-Voltage High	I _{IN_H}	V _{IN_} = 2.4V, all others = 0.8V	-0.1	±0.001	+0.1	μA
Input Current with Input-Voltage Low	I _{IN_L}	V _{IN_} = 0.8V, all others = 2.4V	-0.1	±0.001	+0.1	μA
Input High Voltage	V _{IN_H}		2.4	1.5		V
Input Low Voltage	V _{IN_L}			1.4	0.8	V
DYNAMIC (Note 3)						
Turn-On Time	t _{ON}	V _{COM_} = 3V, Figure 2	T _A = +25°C	35	60	ns
			T _A = T _{MIN} to T _{MAX}			
Turn-Off Time	t _{OFF}	V _{COM_} = 3V, Figure 2	T _A = +25°C	15	20	ns
			T _A = T _{MIN} to T _{MAX}			
On-Channel Bandwidth	BW	Signal = 0dBm, Figure 4, 50Ω in and out	T _A = +25°C	300		MHz
Charge Injection	V _{CTE}	C _L = 1.0nF, V _{GEN} = 0, R _{GEN} = 0, Figure 3	T _A = +25°C	1	5	pC
Off-Isolation (Note 7)	V _{ISO}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 4	T _A = +25°C	-60		dB
Crosstalk (Note 8)	V _{CT}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 5	T _A = +25°C	-80		dB
NO_ or NC_ Capacitance	C _(OFF)	f = 1MHz, Figure 6	T _A = +25°C	16		pF
COM_ Off-Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 6	T _A = +25°C	16		pF
COM_ On-Capacitance	C _{COM(ON)}	f = 1MHz, Figure 6	T _A = +25°C	23		pF
Total Harmonic Distortion	THD	600Ω IN and OUT, 20Hz to 20kHz, 2V _{P-P}	T _A = +25°C	0.009		%
SUPPLY						
Power-Supply Range			2		12	V
Supply Current	I ₊	V _{IN} = 0 or V ₊ , all switches on or off	-1	±0.001	+1	μA

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ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V, V_{IN_H} = 2.4V, V_{IN_L} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
On-Resistance	R _{ON}	V+ = 2.7V, I _{COM_} = 1mA, V _{NO_} = V _{NC_} = 1V	T _A = +25°C	175		360	Ω
			T _A = T _{MIN} to T _{MAX}			450	
On-Resistance Match Between Channels (Note 4)	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 1mA, V _{NO_} = V _{NC_} = 1V	T _A = +25°C	2		5	Ω
			T _A = T _{MIN} to T _{MAX}			10	
NO __ or NC __ Off-Leakage Current (Notes 3, 6)	I _{NO(OFF)}	V+ = 3.6V, V _{COM_} = 0.5V, 3V; V _{NO_} = V _{NC_} = 3V, 0.5V	T _A = +25°C	-0.1		+0.1	nA
			T _A = -40°C to +85°C	-2		+2	
			T _A = -40°C to +125°C	-30		+30	
COM __ Off-Leakage Current (Notes 3, 6)	I _{COM(OFF)}	V+ = 3.6V, V _{COM_} = 0.5V, 3V; V _{NO_} = V _{NC_} = 3V, 0.5V	T _A = +25°C	-0.1		+0.1	nA
			T _A = -40°C to +85°C	-2		+2	
			T _A = -40°C to +125°C	-30		+30	
COM __ On-Leakage Current (Notes 3, 6)	I _{COM(ON)}	V+ = 3.6V, V _{COM_} = 0.5V, 3V; V _{NO_} = V _{NC_} = 0.5V, 3V, or floating	T _A = +25°C	-0.2		+0.2	nA
			T _A = -40°C to +85°C	-4		+4	
			T _A = -40°C to +125°C	-30		+30	
LOGIC INPUTS							
Input High Voltage	V _{IN_H}			2.4	1.0		V
Input Low Voltage	V _{IN_L}				1.0	0.5	V
DYNAMIC (Note 3)							
Turn-On Time	t _{ON}	V _{COM_} = 1.5V, Figure 2	T _A = +25°C	50		90	ns
			T _A = -40°C to +85°C			120	
			T _A = -40°C to +125°C			140	
Turn-Off Time	t _{OFF}	V _{COM_} = 1.5V, Figure 2	T _A = +25°C	30		45	ns
			T _A = T _{MIN} to T _{MAX}			60	

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MAX4610/MAX4611/MAX4612

ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = +12V, V_{IN_H} = 4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
On-Resistance	R _{ON}	V+ = 12V, I _{COM} = 2mA, V _{NO_} = V _{NC_} = 10V	T _A = +25°C	30	45		Ω
			T _A = T _{MIN} to T _{MAX}			60	
LOGIC INPUTS							
Input High Voltage	V _{IN_H}			4.0	2.8		V
Input Low Voltage	V _{IN_L}				2.5	0.8	V
SUPPLY							
Positive Supply Current	I+	V _{IN_} = 0 or V+, all switches on or off		-1	±0.001	+1	μA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON}(\text{max}) - R_{ON}(\text{min})$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 6: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at +25°C.

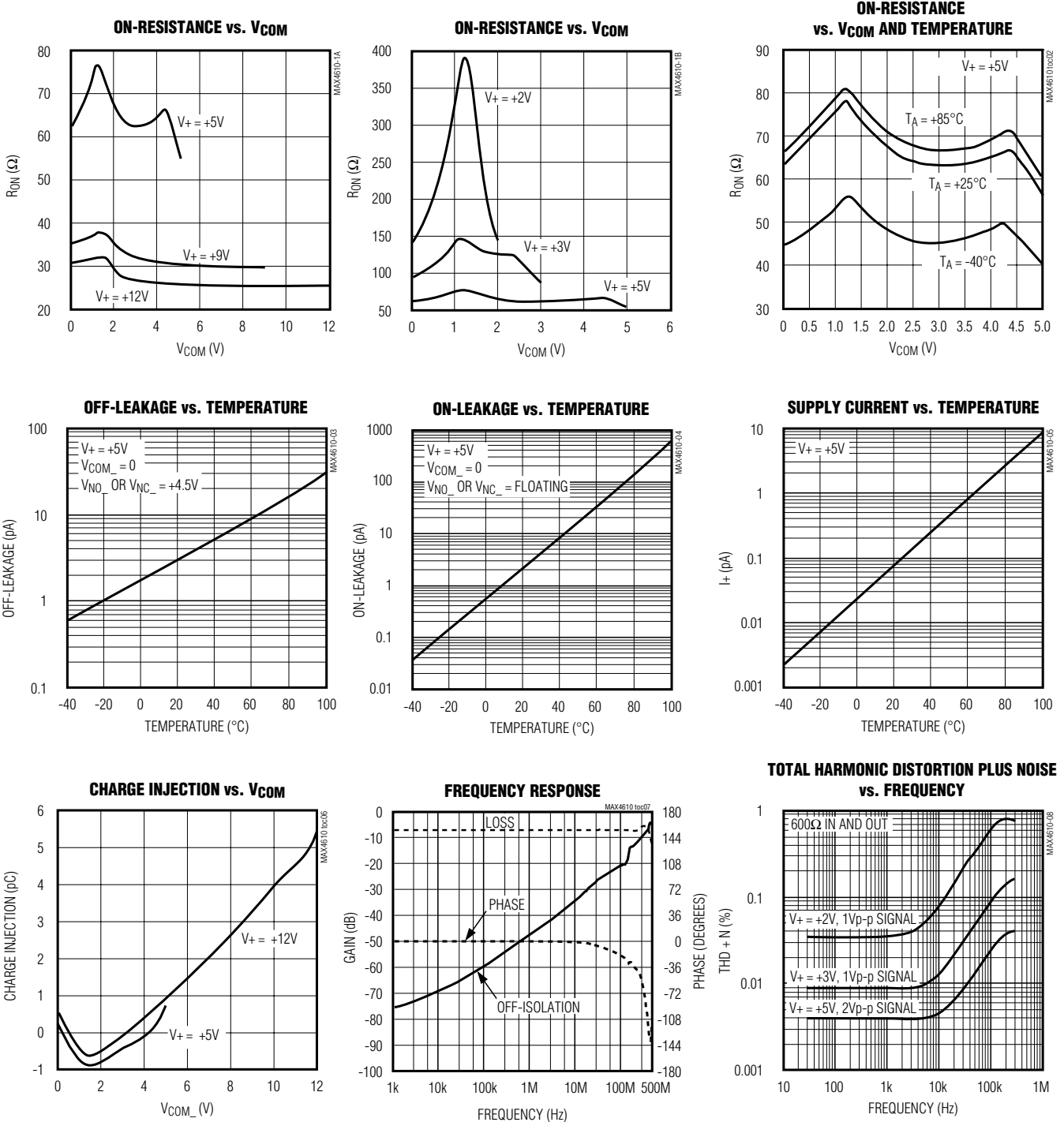
Note 7: Off-Isolation = $20 \log_{10} (V_{COM_} / V_{NO_})$, V_{COM_} = output, V_{NO_} = input to off switch.

Note 8: Between any two switches.

Low-Voltage, Quad, SPST CMOS Analog Switches

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Pin Description

PIN						NAME	FUNCTION
MAX4610		MAX4611		MAX4612			
TSSOP/SO/ DIP	QFN	TSSOP/SO/DIP	QFN	TSSOP/SO/DIP	QFN		
1, 3, 8, 11	1, 3, 8, 11	—	—	—	—	NO1–NO4	Analog Switch Normally Open Terminals
—	—	1, 3, 8, 11	1, 3, 8, 11	—	—	NC1–NC4	Analog Switch Normally Closed Terminals
—	—	—	—	1, 8	1, 8	NO1, NO3	Analog Switch Normally Open Terminals
—	—	—	—	3, 11	3, 11	NC2, NC4	Analog Switch Normally Closed Terminals
2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	COM1–COM4	Analog Switch Common Terminals
13, 5, 6, 12	14, 5, 6, 13	13, 5, 6, 12	14, 5, 6, 13	13, 5, 6, 12	14, 5, 6, 13	IN1–IN4	Logic-Control Digital Input
7	7	7	7	7	7	GND	Ground. Connect to digital ground.
—	12, 15	—	12, 15	—	12, 15	N.C.	No Connection. Not internally connected.
14	16	14	16	14	16	V+	Positive Analog and Digital-Supply Voltage Input. Internally connected to substrate.
—	EP	—	EP	—	EP	EP	Exposed Pad. Connect to V+.

MAX4610/MAX4611/MAX4612

Applications Information

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog or logic signals are not current limited. If this sequencing is not possible, and if the analog or logic inputs are not current limited to 20mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 13V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be

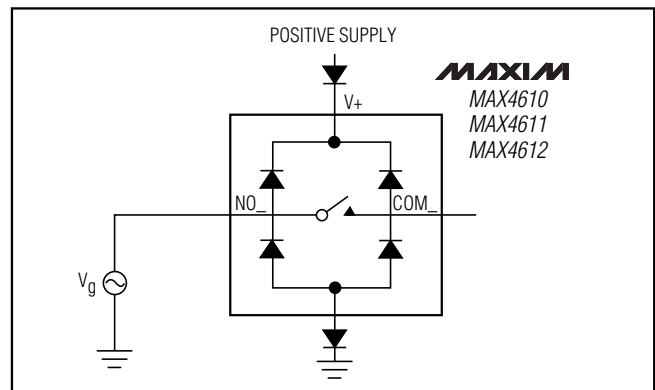


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

significant when low supply voltages (+5V or less) are used. With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

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Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Operating Considerations for High-Voltage Supply

The MAX4610/MAX4611/MAX4612 are pin-compatible with the industry-standard 74HC4066 and the MAX4066, and are optimized for +5V single-supply operation. The MAX4610 family is capable of +12V

single-supply operation with some precautions. The absolute maximum rating for V+ is +13.2V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1µF capacitor to ground as close to the IC as possible.

Caution: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or 12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4610/MAX4611/MAX4612. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Test Circuits/Timing Diagrams

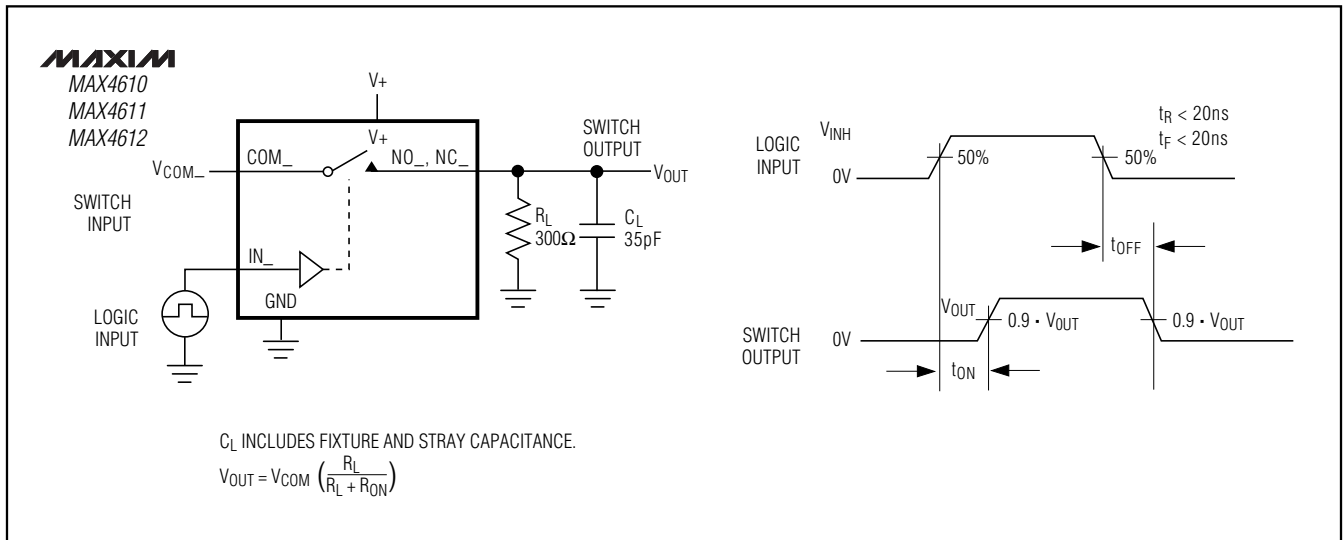


Figure 2. Switching Time

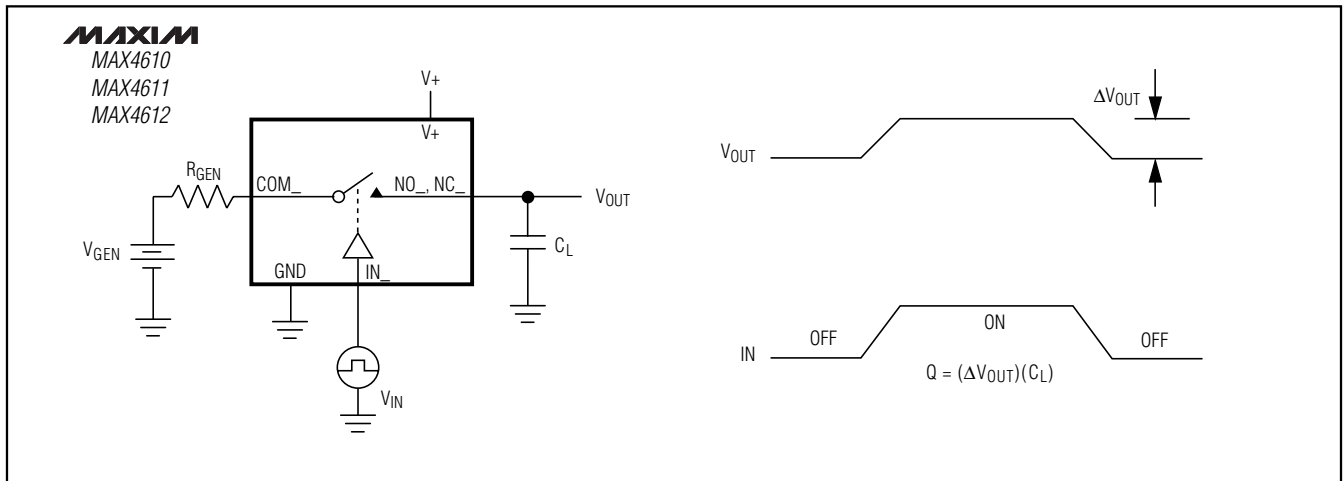


Figure 3. Charge Injection

Low-Voltage, Quad, SPST CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)

MAX4610/MAX4611/MAX4612

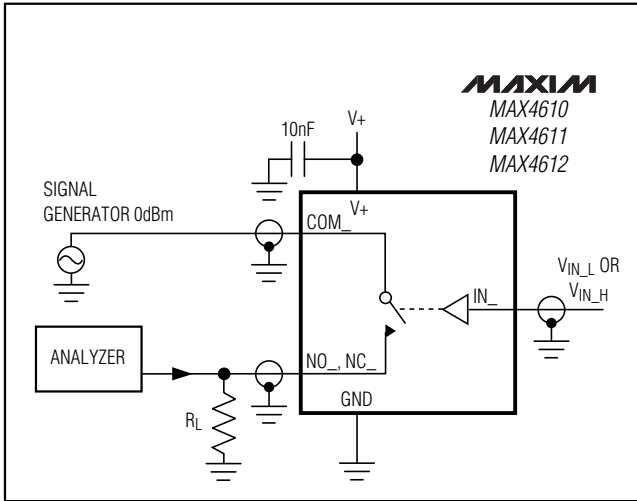


Figure 4. Off-Isolation/On-Channel Bandwidth

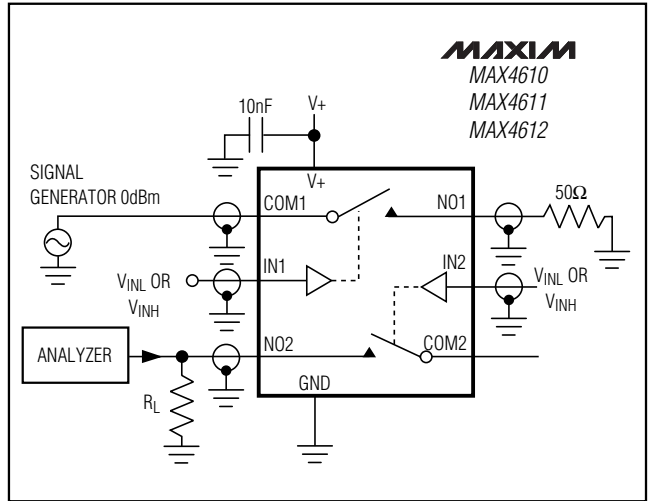


Figure 5. Crosstalk

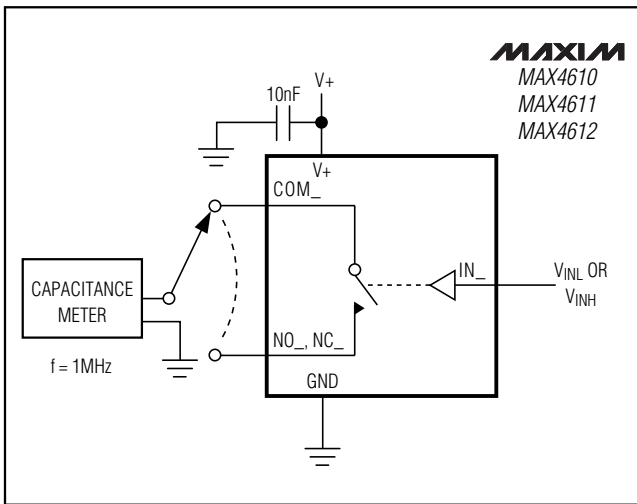


Figure 6. Channel Off/On-Capacitance

Ordering Information (continued)

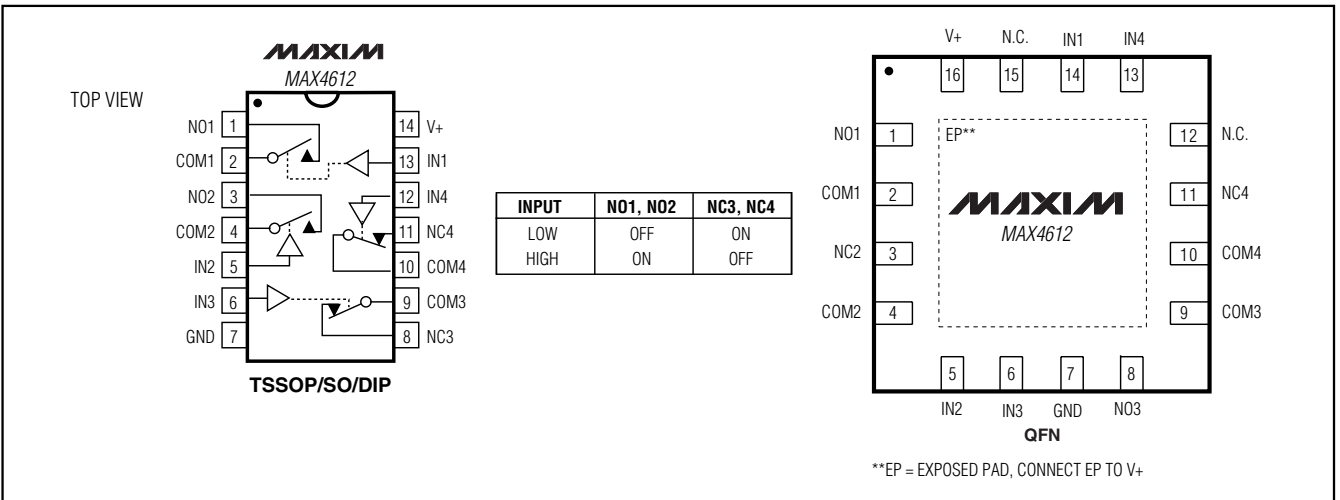
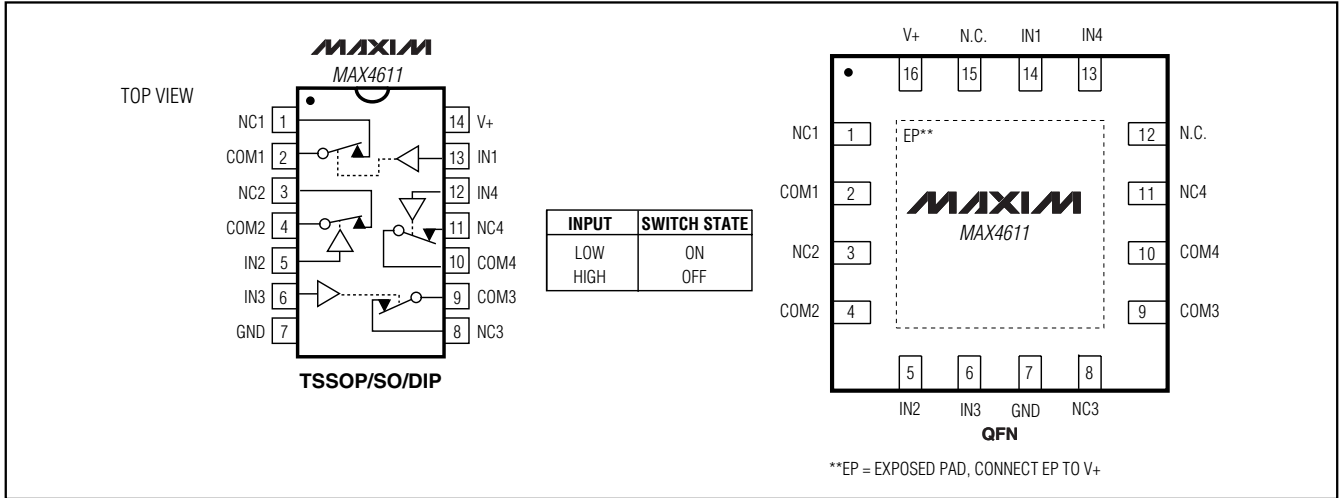
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4611 CUD	0°C to +70°C	14 TSSOP	U14-1
MAX4611CSD	0°C to +70°C	14 Narrow SO	S14-2
MAX4611CPD	0°C to +70°C	14 Plastic DIP	P14-6
MAX4611C/D	0°C to +70°C	Dice*	—
MAX4611EGE	-40°C to +85°C	16 QFN-EP**	G1644-1
MAX4611EUD	-40°C to +85°C	14 TSSOP	U14-1
MAX4611ESD	-40°C to +85°C	14 Narrow SO	S14-2
MAX4611EPD	-40°C to +85°C	14 Plastic DIP	P14-6
MAX4611AUD	-40°C to +85°C	14 TSSOP	U14-1
MAX4611ASD	-40°C to +85°C	14 Narrow SO	S14-2
MAX4612 CUD	0°C to +70°C	14 TSSOP	U14-1
MAX4612 CSD	0°C to +70°C	14 Narrow SO	S14-2
MAX4612CPD	0°C to +70°C	14 Plastic DIP	P14-6
MAX4612C/D	0°C to +70°C	Dice*	—
MAX4612EUD	-40°C to +85°C	14 TSSOP	U14-1
MAX4612ESD	-40°C to +85°C	14 Narrow SO	S14-2
MAX4612EGE	-40°C to +85°C	16 QFN-EP**	G1644-1
MAX4612EPD	-40°C to +85°C	14 Plastic DIP	P14-6
MAX4612AUD	-40°C to +125°C	14 TSSOP	U14-1
MAX4612ASD	-40°C to +125°C	14 Narrow SO	S14-2

*Contact factory for dice specifications.

**EP = Exposed pad.

Low-Voltage, Quad, SPST CMOS Analog Switches

Pin Configurations/Truth Tables (continued)



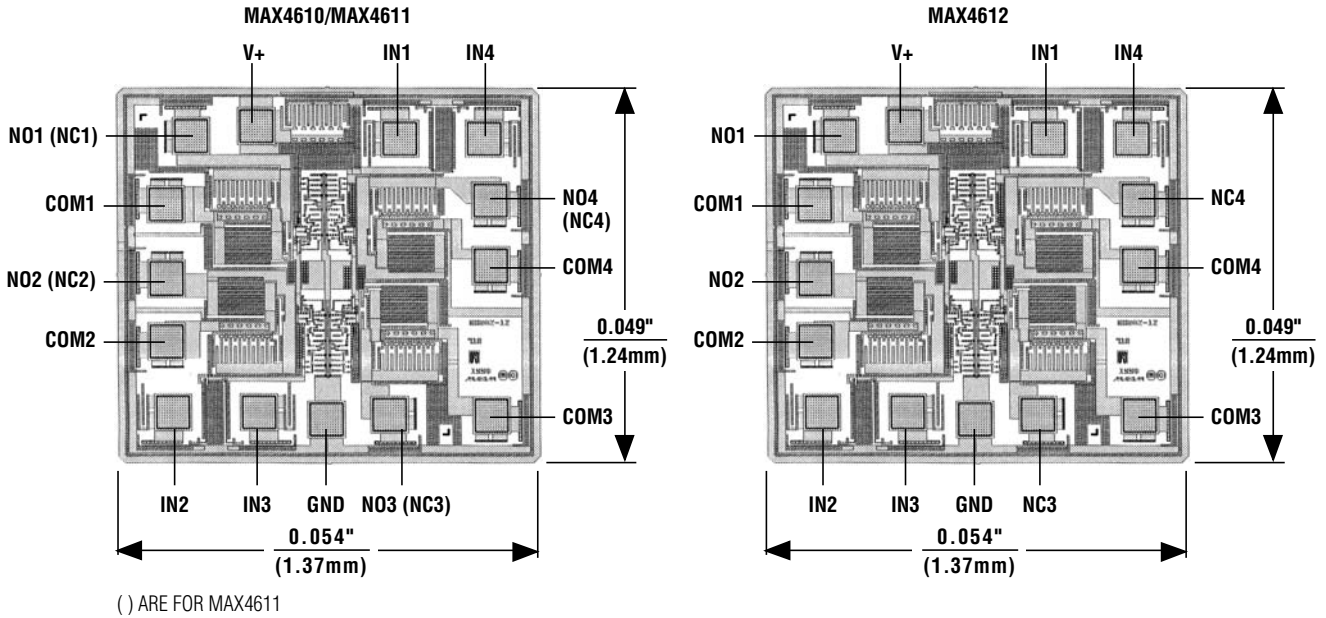
Revision History

Pages changed at Rev 4: 1-5, 7, 9, 10, 13.

Low-Voltage, Quad, SPST CMOS Analog Switches

Chip Topographies

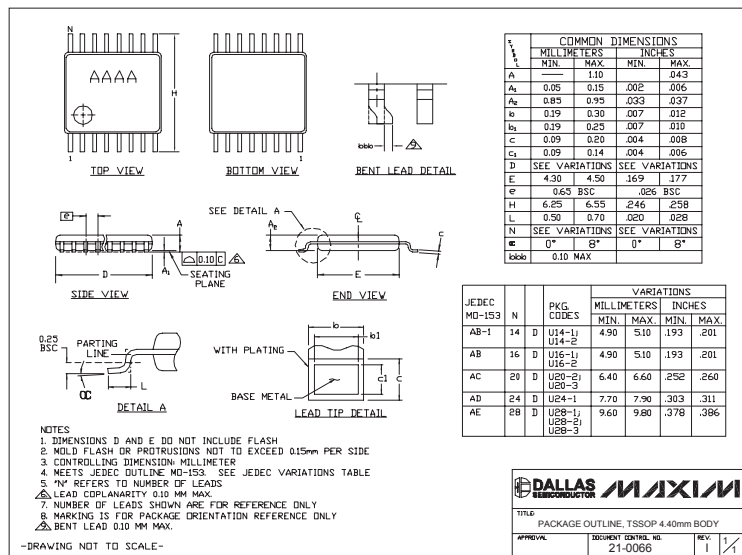
MAX4610/MAX4611/MAX4612



TRANSISTOR COUNT: 132
SUBSTRATE CONNECTED TO V+

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Low-Voltage, Quad, SPST CMOS Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

SOIC N LEPS

TOP VIEW

FRONT VIEW

SIDE VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC 1.27 BSC			
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:

- D&E DO NOT INCLUDE MOLD FLASH.
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
- LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
- CONTROLLING DIMENSION: MILLIMETERS.
- MEETS JEDEC MS012.
- N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV	1/1
	21-0041	B	

PDIP N LEPS

TOP VIEW

FRONT VIEW

SIDE VIEW

INCHES		MILLIMETERS		N	MS000	
MIN	MAX	MIN	MAX			
A	0.180	---	4.572	8	AB	
A1	0.015	---	0.38	14	AC	
A2	0.125	0.175	3.18	4.45	16	AA
A3	0.055	0.080	1.40	2.03	18	AD
B	0.015	0.022	0.381	0.56	20	AE
B1	0.045	0.065	1.14	1.65	24	AF
C	0.008	0.014	0.2	0.355	28	*5
D1	0.005	0.080	0.13	2.03		
E	0.300	0.325	7.62	8.26		
E1	0.240	0.310	6.10	7.87		
e	0.100 BSC		2.54 BSC			
eA	0.300 BSC		7.62 BSC			
eB	0.400 BSC		10.16 BSC			
L	0.115	0.150	2.921	3.81		

NOTES:
 1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
 5. SIMILAR TO JEDEC MO-058AB
 6. N = NUMBER OF PINS

MAXIM

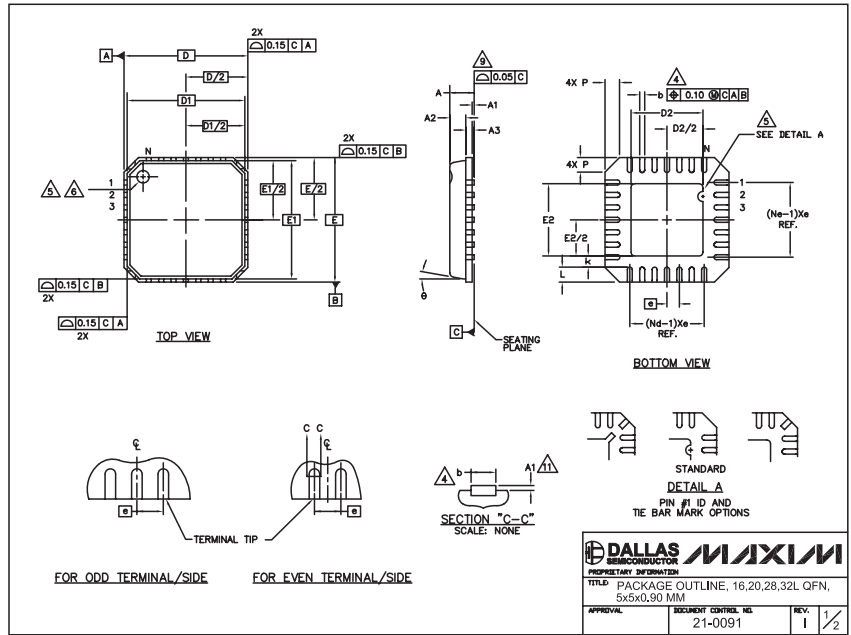
PACKAGE FAMILY OUTLINE: PDIP .300" 1/1 21-0043 D

Low-Voltage, Quad, SPST CMOS Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4610/MAX4611/MAX4612



PKG	COMMON DIMENSIONS											
	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
ø	0"			12"			0"			12"		

PKG CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1695-3	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.12 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

DALLAS MAXIM
SEMICONDUCTOR

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN,
5x5x0,90 MM

APPROVAL	DOCUMENT CONTROL, NO. 21-0091	REV. 1 2/2
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Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.



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MAX4610

Part Number Table

Notes:

1. See the [MAX4610 QuickView Data Sheet](#) for further information on this product family or download the [MAX4610 full data sheet](#) (PDF, 952kB).
2. Other options and links for purchasing parts are listed at: <http://www.maxim-ic.com/sales>.
3. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [full data sheet](#) or [Part Naming Conventions](#).
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX4610EEE-T		<input type="checkbox"/>		-40C to +85C	RoHS/Lead-Free: No
MAX4610C/D		<input type="checkbox"/>			RoHS/Lead-Free: No
MAX4610CPD	<input type="checkbox"/>	<input type="checkbox"/>	PDIP;14 pin;.300" Dwg: 21-0043D (PDF) Use pkgcode/variation: P14-6*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4610EPD	<input type="checkbox"/>	<input type="checkbox"/>	PDIP;14 pin;.300" Dwg: 21-0043D (PDF) Use pkgcode/variation: P14-6*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4610CEE+	<input type="checkbox"/>	<input type="checkbox"/>	QSOP;16 pin;.150" Dwg: 21-0055F (PDF) Use pkgcode/variation: E16+4*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610CEE+T		<input type="checkbox"/>		0C to +70C	RoHS/Lead-Free: Yes
MAX4610CEE-T		<input type="checkbox"/>		0C to +70C	RoHS/Lead-Free: No

MAX4610CEE			QSOP;16 pin; .150" Dwg: 21-0055F (PDF) Use pkgcode/variation: E16-4*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4610EEE				-40C to +85C	RoHS/Lead-Free: No
MAX4610CSD+			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14+2*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610CSD+T			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14+2*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610ASD-T				-40C to +125C	RoHS/Lead-Free: No
MAX4610ASD			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14-2*	-40C to +125C	RoHS/Lead-Free: No Materials Analysis
MAX4610CSD			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14-2*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4610CSD-T			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14-2*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4610ESD+T			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14+2*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610ESD			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14-2*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4610ESD-T			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14-2*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4610ESD+			SOIC;14 pin; .150" Dwg: 21-0041B (PDF) Use pkgcode/variation: S14+2*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610AUD			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14-1*	-40C to +125C	RoHS/Lead-Free: No Materials Analysis
MAX4610AUD-T				-40C to +125C	RoHS/Lead-Free: No
MAX4610CUD			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14-1*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4610CUD+T			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14+1*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis

MAX4610CUD+			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14+1*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610CUD-T			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14-1*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4610EUD+			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14+1*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610EUD+T			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14+1*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4610EUD			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4610EUD-T			TSSOP;14 pin;4.4mm Dwg: 21-0066I (PDF) Use pkgcode/variation: U14-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis

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