

MAX32665/MAX32666

Low-Power Arm Cortex-M4 with FPU-Based Microcontroller with Bluetooth 5 for Wearables

General Description

DARWIN is a new breed of low-power microcontrollers built to thrive in the rapidly evolving Internet of Things (IoT). They are smart, with the biggest memories in their class and a massively scalable memory architecture. They run forever, thanks to wearable-grade power technology. They are durable enough to withstand the most advanced cyberattacks. DARWIN microcontrollers are designed to run any application imaginable—in places where you would not dream of sending other microcontrollers.

Generation UB microcontrollers are designed to handle the increasingly complex applications demanded by today's advanced battery-powered devices and wirelessly connected devices, while providing robust hardware security and Bluetooth® 5 Low Energy (Bluetooth LE) radio connectivity.

The MAX32665/MAX32666 UB class microcontrollers are advanced systems-on-chips featuring an Arm® Cortex®-M4 with FPU CPU for efficient computation of complex functions and algorithms with integrated power management. It also includes the newest generation Bluetooth 5 LE radio with support for long range (4x) and high throughput (2Mbps) and ADI's best-in-class hardware security suite trust protection unit (TPU). The devices offer large on-board memory with 1MB flash and 560KB SRAM. Split flash banks of 512KB each support seamless over-the-air upgrades, adding an additional degree of reliability. Memory scalability of data (SRAM) and code (Flash) space is supported by two SPI execute-in-place (SPIX) interfaces.

Multiple high-speed interfaces are supported including HS-USB, secure digital interface (SD, SDIO, MMC, SD-HC, and microSD™), SPI, UART, and I²C serial interfaces, and an audio subsystem supporting PDM, PCM, I²S, and TDM interfaces. An 8-input, 10-bit ADC is available to monitor analog inputs from external sensors and meters. The devices are available in 109-bump WLP (0.35mm pitch) and 121-bump CTBGA (0.65mm pitch).

Applications

- Connected Home
- Industrial Sensors
- Payment/Fitness/Medical Wearables
- Telemedicine
- Gaming Devices
- Hearables

Benefits and Features

- High-Efficiency Microcontroller and Audio DSP for Wearable and Hearable Devices
 - Arm Cortex-M4 with FPU Up to 96MHz
 - Optional Second Arm Cortex-M4 with FPU Optimized for Data Processing
 - Low-Power, 7.3728MHz System Clock Option
 - 1MB Flash, Organized into Dual Banks 2 x 512KB
 - 560KB SRAM; 3 x 16KB Cache
- Bluetooth 5 Low Energy Radio
 - 1Mbps and 2Mbps Data Throughput
 - Long Range (125kbps and 500kbps)
 - Advertising Extension
 - Rx Sensitivity: -95dbm; Tx Power Up to +4.5dbm
 - On-Chip Matching with Single-Ended Antenna Port
- Power Management Maximizes Operating Time for Battery Applications
 - Integrated SIMO SMPS for Coin-Cell Operation
 - Dynamic Voltage Scaling Minimizes Active Core Power Consumption
 - 27.3µA/MHz at 3.3V Executing from Cache
 - Selectable SRAM Retention in Low Power Modes with RTC Enabled
- Multiple Peripherals for System Control
 - Three QSPI Master/Slave with Three Chip Selects Each, Three 4-Wire UARTs, Three I²C Master/Slave, up to 50 GPIO
 - QSPI (SPIXF) with Real-Time Flash Decryption
 - QSPI (SPIXR) RAM Interface Provides SRAM Expansion
 - 8-Input, 10-Bit Delta-Sigma ADC 7.8ksps
 - USB 2.0 HS Engine with Internal Transceiver
 - PDM Interface Supports Two Digital Microphones
 - I²S with TDM, Six 32-Bit Timers, Two High-Speed Timers, 1-Wire® Master, 16 Pulse Trains (PWM)
 - Secure Digital Interface Supports SD3.0/SDIO3.0/eMMC4.51
- Secure Valuable IP/Data with Hardware Security
 - Trust Protection Unit (TPU) with MAA Supports Fast ECDSA and Modular Arithmetic
 - AES/SHA-2/DES/3DES Hardware Accelerator
 - TRNG Seed Generator
- Ensure Software Integrity and Loading
 - Secure Bootloader (SCPBL)
 - Secure Boot

Simplified Block Diagram

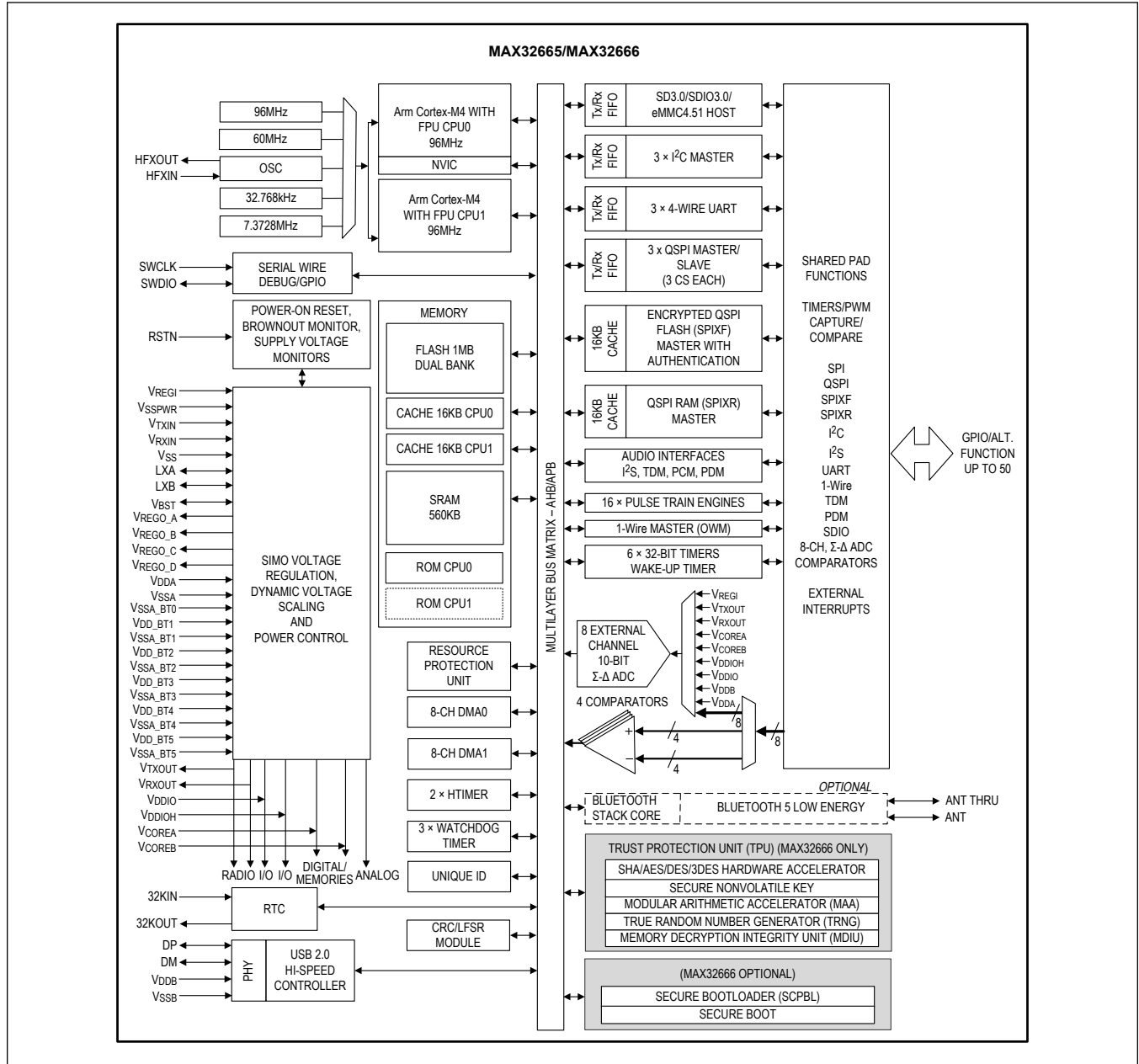


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Absolute Maximum Ratings

V _{COREA}	-0.3V to +1.21V	DM, DP (with respect to V _{SSB})	-0.3V to +3.6V
V _{COREB}	-0.3V to +1.21V	V _{DDIO} Combined Pins (sink)	100mA
V _{DDA}	-0.3V to +1.98V	V _{DDIOH} Combined Pins (sink)	100mA
V _{DDIO}	-0.3V to +1.98V	V _{SSA}	100mA
V _{DDIOH}	-0.3V to +3.6V	V _{SS}	100mA
V _{REGI}	-0.3V to +3.6V	V _{SPPWR}	100mA
V _{TXIN}	-0.3V to +1.9V	V _{SSA_BT[1:5]}	100mA
V _{RXIN}	-0.3V to +1.9V	Output Current (sink) by Any GPIO Pin	25mA
V _{DDA_BT[1:5]}	-0.3V to +1V	Output Current (source) by Any GPIO Pin	-25mA
RSTN, GPIO (V _{DDIO})	-0.3V to V _{DDIO} + 0.5V	Continuous Package Power Dissipation CTBGA (multilayer board) T _A = +70°C (derate 31.0mW/°C above +70°C)	1692mW
GPIO (V _{DDIOH})	-0.3V to V _{DDIOH} + 0.5V	Operating Temperature Range	-40°C to +85°C
32KIN, 32KOUT	-0.3V to V _{DDA} + 0.2V	Storage Temperature Range	-65°C to +125°C
HFXIN, HFXOUT	-0.3V to V _{DDA} + 0.2V	Soldering Temperature	+260°C
AIN[7:0]	-0.3V to +3.6V		
V _{DDB} (with respect to V _{SSB})	-0.3V to +3.6V		

Note: No device pin can exceed 3.63V. All voltages with respect to V_{SS} unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

109 WLP

Package Code	W1093A4+1
Outline Number	21-100301
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ _{JA})	38.05°C/W
Junction to Case (θ _{JC})	N/A

121 CTBGA

Package Code	X12188+6C
Outline Number	21-0680
Land Pattern Number	90-0451
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ _{JA})	32.5°C/W
Junction to Case (θ _{JC})	8.8°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Core Input Supply Voltage A	V _{COREA}		V _{COREA} V _{RST}	1.1	1.21	V

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Core Input Supply Voltage B	V _{COREB}		V _{COREB} V _{RST}	1.1	1.21	V
Input Supply Voltage, Analog	V _{DDA}		1.71	1.8	1.89	V
Input Supply Voltage, TXIN	V _{TXIN}	Bluetooth Transmitter Supply	1.1	1.3	1.9	V
Input Supply Voltage, RXIN	V _{RXIN}	Bluetooth Receiver Supply	1.1	1.3	1.9	V
Input Supply Voltage, Battery	V _{REGI}	If power to the device is cycled, V _{REGI} must exceed V _{REGI_POR(MIN)} within 20ms after V _{DDA} > 1.24V. After that, V _{REGI} can settle to its final value.	2.0	2.7	3.6	V
	V _{REGI_POR}		2.4			
Input Supply Voltage, GPIO	V _{DDIO}		1.71	1.8	1.89	V
Input Supply Voltage, GPIO (High)	V _{DDIOH}		1.71	1.8	3.6	V
Power-Fail Reset Voltage	V _{RST}	Monitors V _{COREA}	0.72	0.77		V
		Monitors V _{COREB}	0.72	0.77		
		Monitors V _{DDA}	1.60	1.65	1.69	
		Monitors V _{ddb}	2.81	2.91		
		Monitors V _{DDIO}	1.60	1.65	1.69	
		Monitors V _{DDIOH}	1.60	1.65	1.69	
		Monitors V _{REGI}	1.94		2.08	
		Monitors V _{TXOUT}		0.773		
		Monitors V _{RXOUT}		0.773		
Power-On Reset Voltage	V _{POR}	Monitors V _{COREA}		0.63		V
V _{REGI} Current, ACTIVE Mode	I _{REGI_ACT}	Total current into V _{REGI} pins, f _{sys_clk} = 96MHz, V _{REGI} = 3.3V, CPU0 in ACTIVE mode, executing While(1) from cache; inputs tied to V _{SS} , V _{DDIO} , or V _{DDIOH} ; outputs source/sink 0mA		3.3		mA
	I _{REGI_SLOPE}	This parameter is the slope of a line which includes the point I _{REGI_ACT} and a nonzero y-intercept. V _{REGI} = 3.3V, f _{sys_clk} is changed only. DVS off. CPU0 in ACTIVE mode, executing While(1) from cache; inputs tied to V _{SS} , V _{DDIO} , or V _{DDIOH} ; outputs source/sink 0mA		27.3		μA/MHz
V _{REGI} Current, SLEEP Mode	I _{REGI_SLP}	Total current into V _{REGI} pins, f _{sys_clk} = 96MHz, V _{REGI} = 3.3V, CPU0 in SLEEP mode; inputs tied to V _{SS} , V _{DDIO} , or V _{DDIOH} ; outputs source/sink 0mA		2.1		mA

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
V _{REGI} Current, BACKUP Mode	I _{REGI_BK}	Total current into V _{REGI} pins, V _{REGI} = 3.3V; inputs tied to V _{SS} , V _{DDIO} , or V _{DDIOH} ; outputs source/sink 0mA	RTC enabled, full memory retention		8.6		μA
			RTC enabled, no memory retention		1.6		
			RTC disabled, no memory retention		1.2		
			RTC disabled, full memory retention		8.4		
			RTC disabled, 32KB memory retention		6.3		
			RTC disabled, 64KB memory retention		6.3		
V _{REGI} Fixed Current, DEEPSLEEP Mode	I _{REGI_FDSL}	Standby state with full retention		10.0		μA	
V _{REGO_X} Output Current	V _{REGO_X_IOUT}	Output current for each of the V _{REGO_X} outputs		5	50	mA	
V _{REGO_X} Output Current Combined	V _{REGO_X_IOUT_TOT}	All four V _{REGO_X} outputs combined		15	100	mA	
V _{REGO_X} Output Voltage Range	V _{REGO_X_RANGE}	V _{REGI} ≥ V _{REGO_X} + 200mV	0.5	1.0	1.85	V	
V _{REGO_X} Efficiency	V _{REGO_X_EFF}	V _{REGI} = 2.7V, V _{REGO_X} = 1.1V, load = 30mA		90		%	
CLOCKS							
System Clock Frequency	f _{SYS_CLK}		8		96,000	kHz	
System Clock Period	t _{SYS_CLK}			1/f _{SYS_CLK}		ns	
High-Speed Oscillator Frequency	f _{HSCLK}	Factory default, user adjustable 50MHz to 96MHz	92.5	96	99.6	MHz	
Low-Power Oscillator Frequency	f _{LPCLK}			60		MHz	
RF Oscillator Frequency	f _{RFCLK}	32MHz crystal, C _L = 12pF, ESR ≤ 50Ω, C ₀ ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm		32		MHz	
HFXIN, HFXOUT Input Capacitance	C _{HFX_PIN}			6		pF	
7MHz Oscillator Frequency	f _{7MCLK}			7.3728		MHz	
RTC Input Frequency	f _{32KIN}	32kHz watch crystal, C _L = 6pF, ESR < 90kΩ, C ₀ ≤ 2pF		32.768		kHz	
RTC Operating Current	I _{RTC_BDSLP}	BACKUP or DEEPSLEEP mode		0.39		μA	
RTC Power-Up Time	t _{RTC_ON}			250		ms	
Nanoring Oscillator Frequency	f _{NANO}			8		kHz	

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			$0.3 \times V_{DDIO}$	V
	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			$0.3 \times V_{DDIOH}$	
Input Low Voltage for RSTN	V_{IL_RSTN}			$0.5 \times V_{COREA}$		V
Input High Voltage for All GPIO	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	$0.7 \times V_{DDIO}$			V
	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	$0.7 \times V_{DDIOH}$			
Input High Voltage for RSTN	V_{IH_RSTN}			$0.5 \times V_{COREA}$		V
Output Low Voltage for All GPIO	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, $V_{DDIO} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 00$, $I_{OL} = 1mA$		0.2	0.4	V
		V_{DDIO} selected as I/O supply, $V_{DDIO} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 01$, $I_{OL} = 2mA$		0.2	0.4	
		V_{DDIO} selected as I/O supply, $V_{DDIO} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 10$, $I_{OL} = 4mA$		0.2	0.4	
		V_{DDIO} selected as I/O supply, $V_{DDIO} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 11$, $I_{OL} = 8mA$		0.2	0.4	
	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, $V_{DDIOH} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 00$, $I_{OL} = 1mA$		0.2	0.4	
		V_{DDIOH} selected as I/O supply, $V_{DDIOH} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 01$, $I_{OL} = 2mA$		0.2	0.4	
		V_{DDIOH} selected as I/O supply, $V_{DDIOH} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 10$, $I_{OL} = 4mA$		0.2	0.4	
		V_{DDIOH} selected as I/O supply, $V_{DDIOH} = 1.71V$, $GPIO_n_DS_SEL[1:0] = 11$, $I_{OL} = 8mA$		0.2	0.4	
Combined I_{OL} , All GPIO	I_{OL_TOTAL}				48	mA

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage for All GPIO	V _{OH_VDDIO}	V _{DDIO} selected as I/O supply, V _{DDIO} = 1.71V, GPIO _n _DS_SEL[1:0] = 00, I _{OL} = -1mA	V _{DDIO} - 0.4			V
		V _{DDIO} selected as I/O supply, V _{DDIO} = 1.71V, GPIO _n _DS_SEL[1:0] = 01, I _{OL} = -2mA	V _{DDIO} - 0.4			
		V _{DDIO} selected as I/O supply, V _{DDIO} = 1.71V, GPIO _n _DS_SEL[1:0] = 10, I _{OL} = -4mA	V _{DDIO} - 0.4			
		V _{DDIO} selected as I/O supply, V _{DDIO} = 1.71V, GPIO _n _DS_SEL[1:0] = 11, I _{OL} = -8mA	V _{DDIO} - 0.4			
	V _{OH_VDDIOH}	V _{DDIOH} selected as I/O supply, V _{DDIOH} = 1.71V, GPIO _n _DS_SEL[1:0] = 00, I _{OL} = -1mA	V _{DDIOH} - 0.4			
		V _{DDIOH} selected as I/O supply, V _{DDIOH} = 1.71V, GPIO _n _DS_SEL[1:0] = 01, I _{OL} = -2mA	V _{DDIOH} - 0.4			
		V _{DDIOH} selected as I/O supply, V _{DDIOH} = 1.71V, GPIO _n _DS_SEL[1:0] = 10, I _{OL} = -4mA	V _{DDIOH} - 0.4			
		V _{DDIOH} selected as I/O supply, V _{DDIOH} = 1.71V, GPIO _n _DS_SEL[1:0] = 11, I _{OL} = -8mA	V _{DDIOH} - 0.4			
Combined I _{OH} , All GPIO	I _{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V _{IHYS}			300		mV
Input Leakage Current Low	I _{IL}	V _{DDIO} = 1.89V, V _{DDIOH} = 3.6V, V _{DDIOH} selected as I/O supply, V _{IN} = 0V, internal pullup disabled	-100		+100	nA
Input Leakage Current High	I _{IH}	V _{DDIO} = 1.89V, V _{DDIOH} = 3.6V, V _{DDIOH} selected as I/O supply, V _{IN} = 3.6V, internal pulldown disabled	-100		+100	nA
	I _{OFF}	V _{DDIO} = 0V, V _{DDIOH} = 0V, V _{DDIO} selected as I/O supply, V _{IN} < 1.89V	-1		+1	μA
	I _{IH3V}	V _{DDIO} = V _{DDIOH} = 1.71V, V _{DDIO} selected as I/O supply, V _{IN} = 3.6V	-2		+2	
Input Pullup Resistor RSTN	R _{PU_R}	P1M = 1		1		MΩ
		P1M = 0		25		kΩ
Input Pullup/Pulldown Resistor for All GPIO	R _{PU1}	Normal resistance		25		kΩ
	R _{PU2}	Highest resistance		1		MΩ
BLUETOOTH RADIO / POWER						
Bluetooth Supply Voltage LNA/Mixer	V _{DDA_BT1}	Internal LDO disabled	0.855	0.9	0.945	V
Bluetooth Supply Voltage Power Amplifier	V _{DDA_BT2}	Internal LDO disabled	0.9		1.2	V

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bluetooth Supply Voltage FRAC_N Divider	V _{DDA_BT3}	Internal LDO disabled	0.855	0.9	0.945	V
Bluetooth Supply Voltage Receiver Baseband	V _{DDA_BT4}	Internal LDO disabled	0.855	0.9	0.945	V
Bluetooth Supply Voltage Voltage-Controlled Oscillator	V _{DDA_BT5}	Internal LDO disabled	0.855	0.9	0.945	V
BLUETOOTH RADIO / FREQUENCY						
Operating Frequency		1MHz channel spacing	2360		2500	MHz
PLL Programming Resolution	PLL_RES			1		MHz
Frequency Deviation at 1Mbps	$\Delta f_{1\text{MHz}}$			± 170		kHz
Frequency Deviation at Bluetooth LE 1Mbps	$\Delta f_{\text{BLE}1\text{MHz}}$			± 250		kHz
Frequency Deviation at 2Mbps	$\Delta f_{2\text{MHz}}$			± 320		kHz
Frequency Deviation at Bluetooth LE 2Mbps	$\Delta f_{\text{BLE}2\text{MHz}}$			± 500		kHz
BLUETOOTH RADIO / CURRENT CONSUMPTION (SIMO enabled, V_{REGI} = 3.3V. Low-power oscillator enabled, f_{SYS_CLK} = 60MHz, Bluetooth LE stack running on dedicated hardware. Measured at the V_{REGI} device pin, V_{REGO_B} = 0.9V. CPU0 in DEEPSLEEP mode.)						
Tx Run Current	I _{TX_+4.5DBM}	P _{RF} = +4.5dBm		6.00		mA
	I _{TX_0DBM}	P _{RF} = 0dBm		4.30		
	I _{TX_-10DBM}	P _{RF} = -10dBm		3.22		
	I _{TX_-12DBM}	P _{RF} = -12dBm		3.05		
	I _{TX_-16DBM}	P _{RF} = -16dBm		2.85		
	I _{TX_-20DBM}	P _{RF} = -20dBm		2.80		
Tx Startup Current	I _{START_TX}			1.40		mA
Rx Run Current	I _{RX_1M}	f _{RX} = 1Mbps		3.20		mA
	I _{RX_2M}	f _{RX} = 2Mbps		3.30		
Rx Startup Current	I _{START_RX}			1.40		mA
BLUETOOTH RADIO / TRANSMITTER						
Maximum Output Power	P _{RF}			+4.5		dBm
RF Power Accuracy	P _{RF_ACC}			± 1		dB
First Adjacent Channel Transmit Power $\pm 2\text{MHz}$	P _{RF1_1}	2Mbps Bluetooth LE		-31.7		dBc
Second Adjacent Channel Transmit Power $\pm 4\text{MHz}$	P _{RF2_1}	2Mbps Bluetooth LE		-49.1		dBc

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BLUETOOTH RADIO / RECEIVER						
Maximum Received Signal Strength at < 0.1% PER	P _{RX_MAX}			0		dBm
Receiver Sensitivity, Ideal Transmitter	P _{SENS_IT}	1Mbps Bluetooth LE		-95		dBm
		2Mbps Bluetooth LE		-92		
Receiver Sensitivity, Dirty Transmitter	P _{SENS_DT}	1Mbps Bluetooth LE		-94		dBm
		2Mbps Bluetooth LE		-91		
Receiver Sensitivity, Long-Range Coded	P _{SENS_LR}	125kbps Bluetooth LE		-103		dBm
		500kbps Bluetooth LE		-101		
C/I Cochannel	C/I _{1MHz}	1Mbps Bluetooth LE		8		dB
	C/I _{2MHz}	2Mbps Bluetooth LE		8		
Adjacent Interference	C/I _{+1_1}	+1MHz offset, 1Mbps Bluetooth LE		-1		dBm
	C/I _{-1_1}	-1MHz offset, 1Mbps Bluetooth LE		-2		
	C/I _{+2_1}	+2MHz offset, 1Mbps Bluetooth LE		-30.7		dB
	C/I _{-2_1}	-2MHz offset, 1Mbps Bluetooth LE		-32.3		
	C/I _{+2_2}	+2MHz offset, 2Mbps Bluetooth LE		-1.7		
	C/I _{-2_2}	-2MHz offset, 2Mbps Bluetooth LE		-3		
	C/I _{+4_2}	+4MHz offset, 2Mbps Bluetooth LE		-25.3		
C/I _{-4_2}	-4MHz offset, 2Mbps Bluetooth LE		-26.3			
Adjacent Interference, (3+n) MHz Offset [n = 0, 1, 2, . . .]	C/I _{3+MHZ}	1Mbps Bluetooth LE		-34.8		dB
Adjacent Interference, (6+2n) MHz Offset [n = 0, 1, 2, . . .]	C/I _{6+MHZ}	2Mbps Bluetooth LE		-34.8		dB
Intermodulation Performance, 1Mbps Bluetooth LE with 3MHz, 4MHz, 5MHz Offset	P _{IMD_1MBPS}	1Mbps Bluetooth LE		-37.1		dBm
Intermodulation Performance, 2Mbps Bluetooth LE with 6MHz, 8MHz, 10MHz Offset	P _{IMD_2MBPS}	2Mbps Bluetooth LE		-36.4		dBm
Received Signal Strength Indicator Accuracy	RSSI _{ACC}			±3		dB
Received Signal Strength Indicator Range	RSSI _{RANGE}			-95 to -50		dB
ADC (DELTA-SIGMA)						
Resolution				10		Bits
ADC Clock Rate	f _{ACLK}		0.1		8	MHz
ADC Clock Period	t _{ACLK}			1/f _{ACLK}		µs

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{AIN}	AIN[7:0], ADC_DIVSEL = [00], ADC_CH_SEL = [7:0]	REF_SEL = 0, INPUT_SCALE = 0	$V_{SSA} + 0.05$		V_{BG}	V
		AIN[7:0], ADC_DIVSEL = [01], ADC_CH_SEL = [7:0]	REF_SCALE = 0, INPUT_SCALE = 0	$V_{SSA} + 0.05$		$2 \times V_{BG}$	
		AIN[7:0], ADC_DIVSEL = [10], ADC_CH_SEL = [7:0]	REF_SCALE = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	$V_{SSA} + 0.05$		V_{DDIOH}	
		AIN[7:0], ADC_DIVSEL = [11], ADC_CH_SEL = [7:0]	REF_SEL = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	$V_{SSA} + 0.05$		V_{DDIOH}	
Input Impedance	R_{AIN}				30		k Ω
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}			1		pF
		Dynamically switched capacitance			250		fF
Integral Nonlinearity	INL	Measured at +25°C, insignificant temperature drift due to architecture				± 2	LSb
Differential Nonlinearity	DNL	Measured at +25°C, insignificant temperature drift due to architecture				± 1	LSb
Offset Error	V_{OS}				± 1		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled			210		μA
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart				10	μs
ADC Output Latency	t_{ADC}				1067		t_{ACLK}
ADC Sample Rate	f_{ADC}					7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected			0.16		nA
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF			1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method			30		ppm
COMPARATORS							
Input Offset Voltage	V_{OFFSET}				± 1		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00			± 23		mV
		AINCOMPHYST[1:0] = 01			± 50		
		AINCOMPHYST[1:0] = 10			± 2		
		AINCOMPHYST[1:0] = 11			± 7		
Input Voltage Range	V_{IN_CMP}	Common-mode range		0.6		1.35	V

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, $f_{FLC_CLK} = 1\text{MHz}$		42		μs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	$T_A = +85^\circ\text{C}$	10			years
USB						
USB Transceiver Supply Voltage	V_{DDB}		3.0	3.3	3.6	V
Pin Capacitance (DP, DM)	C_{IN_USB}	Pin to V_{SSB}		8		pF
Driver Output Resistance	R_{DRV}	Steady state drive		$44 \pm 10\%$		Ω
USB / FULL SPEED						
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}		2.1			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}				0.5	V
Output High Voltage (DP, DM)	V_{OH_USB}	$R_L = 1.5\text{k}\Omega$ from DP and DM to V_{SSB} , $I_{OH} = -4\text{mA}$	2.8		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	$R_L = 1.5\text{k}\Omega$ from DP to V_{DDB} , $I_{OL} = 4\text{mA}$	V_{SS}		0.3	V
Differential Input Sensitivity	V_{DI}	DP to DM ; system requirement, not tested	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range; system requirement, not tested	0.8		2.5	V
Transition Time (Rise/Fall) DP, DM	t_{RF}	$C_L = 50\text{pF}$	4		20	ns
Pullup Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	k Ω
USB / HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low-Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High-Level Output Voltage	V_{HSOH}			400 ± 40		mV

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ± 200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ± 200		mV

Electrical Characteristics—SPI

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	$f_{SYS_CLK} = 96\text{MHz}$, $f_{MCK(MAX)} = f_{SYS_CLK}/2$			48	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH} , t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				48	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH} , t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		μs

Electrical Characteristics—SPI (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I²C

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			μ s
High Time SCL Clock	t_{HIGH}		4.0			μ s
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			μ s
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			μ s
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			μ s
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			μ s
Data Valid Time	$t_{VD;DAT}$		3.45			μ s
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			μ s
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			μ s
High Time SCL Clock	t_{HIGH}		0.6			μ s
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			μ s
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			μ s

Electrical Characteristics—I²C (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	t _{SU;DAT}			125		ns
Data Hold Time	t _{HD;DAT}			10		ns
Rise Time for SDA and SCL	t _R			30		ns
Fall Time for SDA and SCL	t _F			30		ns
Setup Time for a Stop Condition	t _{SU;STO}		0.6			μs
Bus Free Time Between a Stop and Start Condition	t _{BUS}		1.3			μs
Data Valid Time	t _{VD;DAT}		0.9			μs
Data Valid Acknowledge Time	t _{VD;ACK}		0.9			μs
FAST-MODE PLUS						
Output Fall Time	t _{OF}	From V _{IH(MIN)} to V _{IL(MAX)}		80		ns
Pulse Width Suppressed by Input Filter	t _{SP}			75		ns
SCL Clock Frequency	f _{SCL}		0		1000	kHz
Low Period SCL Clock	t _{LOW}		0.5			μs
High Time SCL clock	t _{HIGH}		0.26			μs
Setup Time for Repeated Start Condition	t _{SU;STA}		0.26			μs
Hold Time for Repeated Start Condition	t _{HD;STA}		0.26			μs
Data Setup Time	t _{SU;DAT}			50		ns
Data Hold Time	t _{HD;DAT}			10		ns
Rise Time for SDA and SCL	t _R			50		ns
Fall Time for SDA and SCL	t _F			30		ns
Setup Time for a Stop Condition	t _{SU;STO}		0.26			μs
Bus Free Time Between a Stop and Start Condition	t _{BUS}		0.5			μs
Data Valid Time	t _{VD;DAT}		0.45			μs
Data Valid Acknowledge Time	t _{VD;ACK}		0.45			μs

Electrical Characteristics—SD/SDIO/SDHC/MMC

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency in Data Transfer Mode	$f_{\text{SDHC_CLK}}$		0		$f_{\text{HSCLK}}/2$	MHz
Clock Period	t_{CLK}			$1/f_{\text{SDHC_CLK}}$		ns
Clock Low Time	t_{WCL}			7		ns
Clock High Time	t_{WCH}			7		ns
Input Setup Time	t_{ISU}			5		ns
Input Hold Time	t_{IHL}			1		ns
Output Valid Time	t_{OVL}			5		ns
Output Hold Time	t_{OHL}			6		ns

Electrical Characteristics—1-Wire Master

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		μs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		μs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		μs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		μs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		μs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		μs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		μs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		μs
		Overdrive		12		

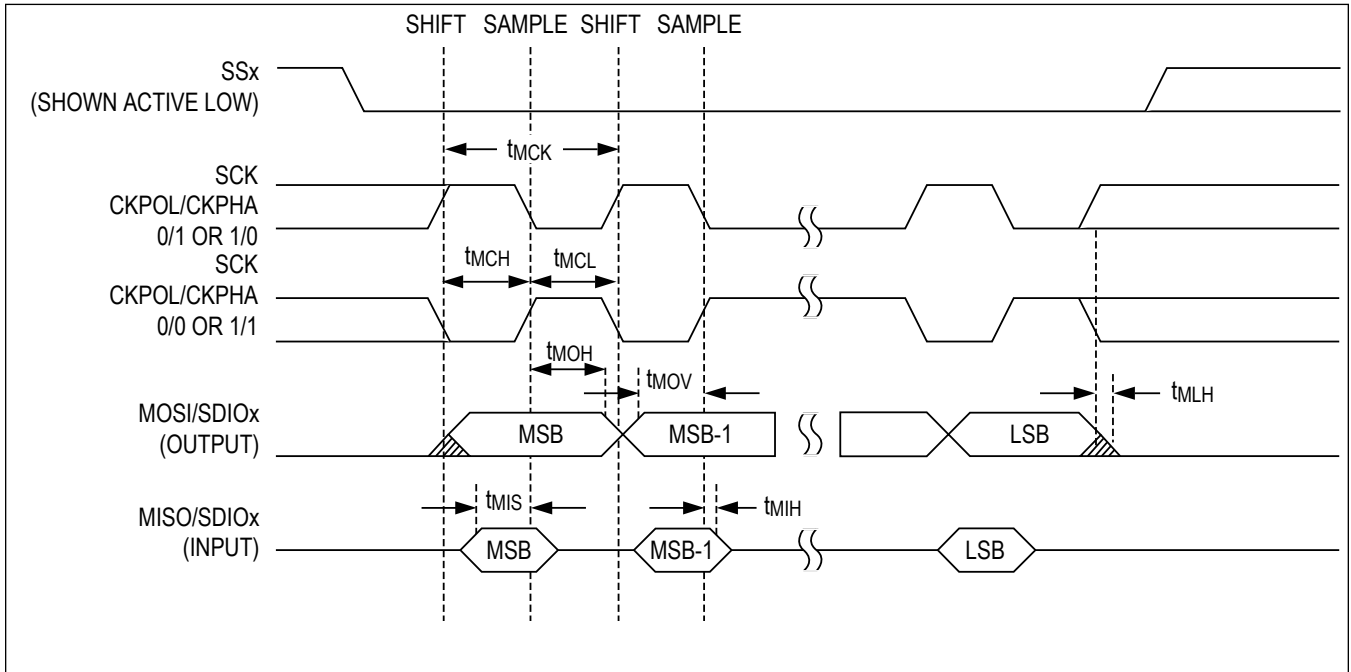


Figure 1. SPI Master Mode Timing Diagram

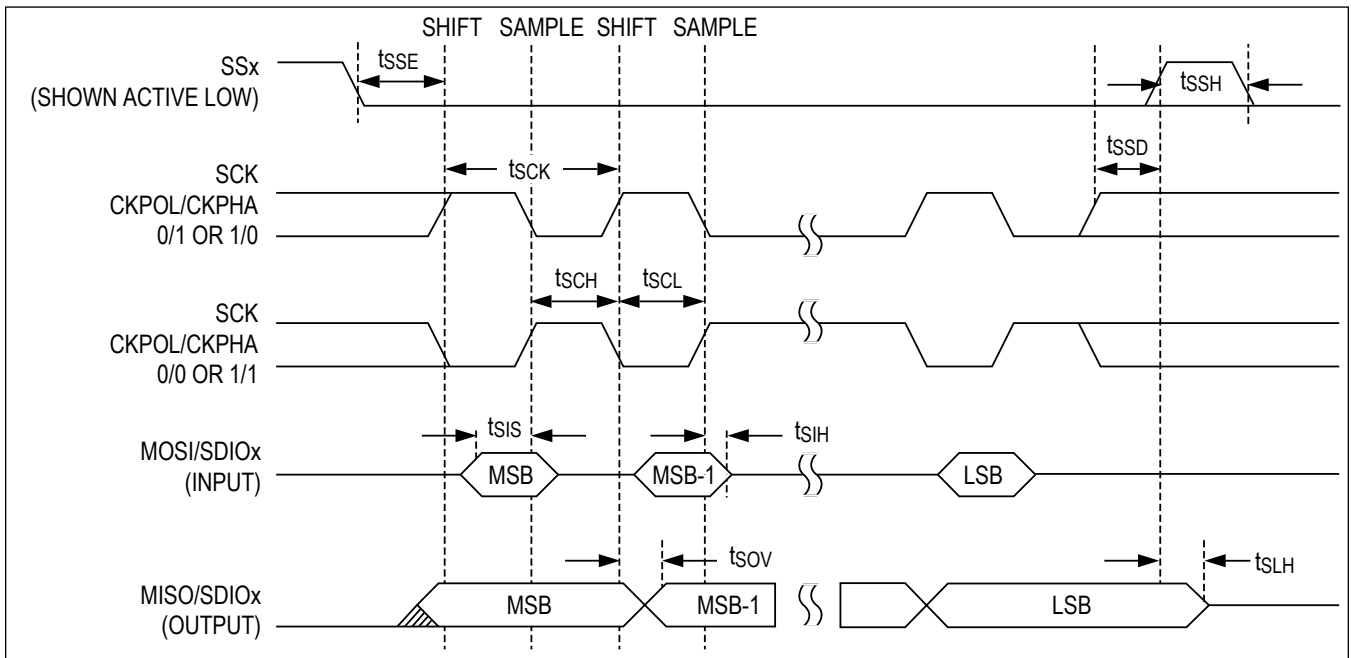


Figure 2. SPI Slave Mode Timing Diagram

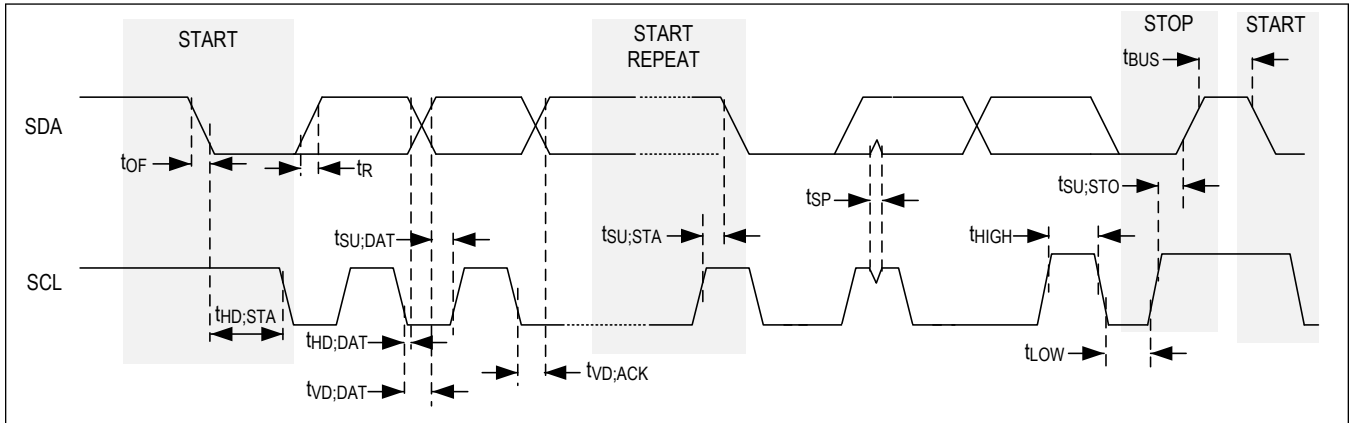


Figure 3. I²C Timing Diagram

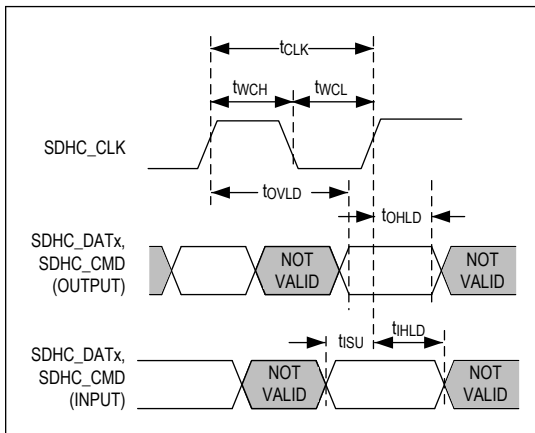


Figure 4. SD/SDIO/SDHC/MMC Timing Diagram

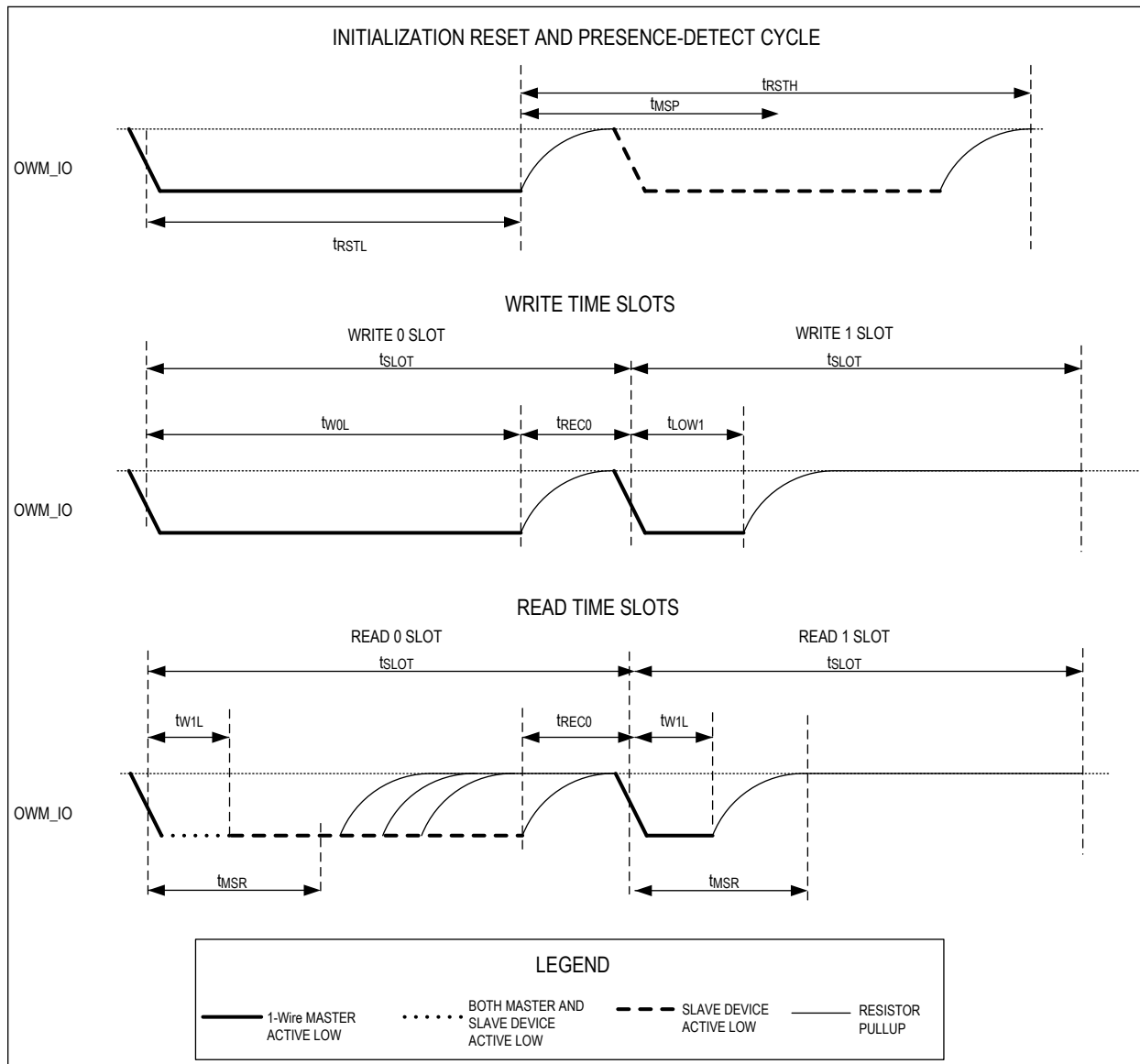
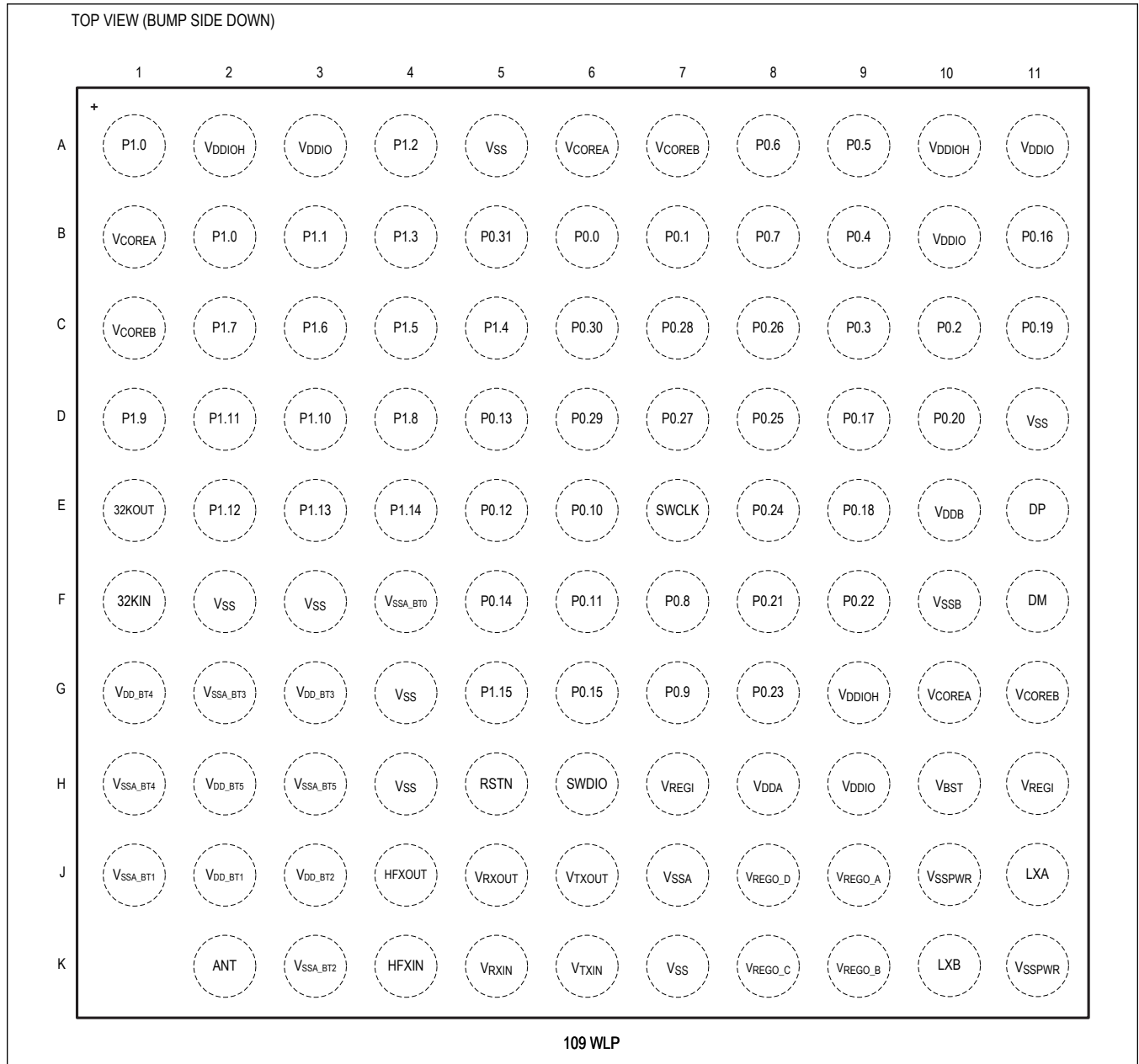


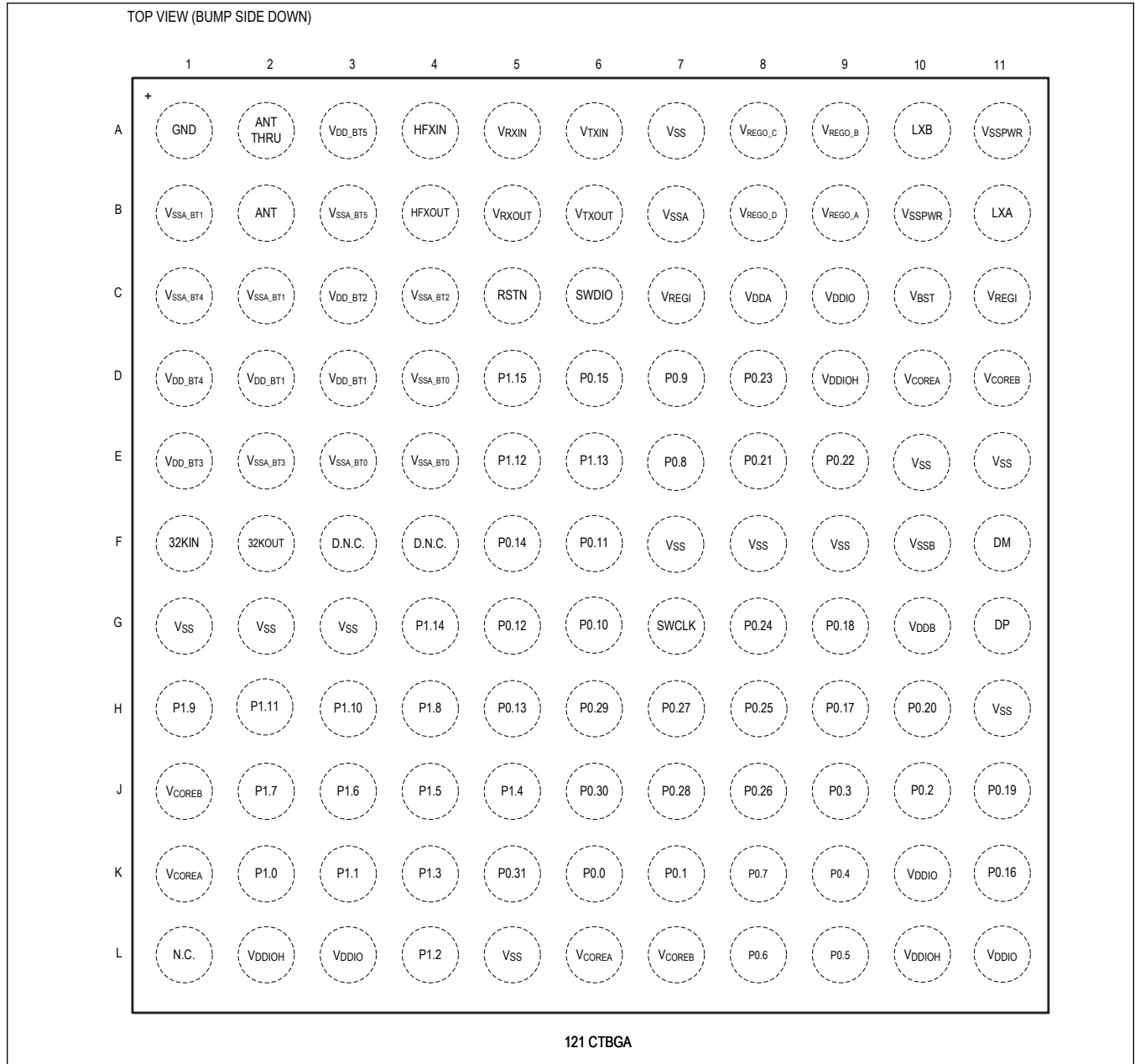
Figure 5. 1-Wire Master Data Timing Diagram

Pin Configurations

109 WLP



121 CTBGA



Pin Description

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
POWER (See Bypass Capacitor Recommendations.)			
H7, H11	C7, C11	VREGI	Battery Power Supply Input for the SIMO. See VREGI Design Considerations.
J10, K11	A11, B10	VSSPWR	Ground for the SIMO. Connect to VSS.

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
A5, D11, F2, F3, G4, H4, K7	A7, E10, E11, F7, F8, F9, G1, G2, G3, H11, L5	V _{SS}	Digital Ground
—	A1	GND	This device pin is not connected internally to the die. Connect this device pin to the ground plane of the circuit board. Do not connect any other signal to this pin.
K6	A6	V _{TXIN}	Radio Transmitter Supply Voltage Input. Bypass with 1μF to V _{SS} .
K5	A5	V _{RXIN}	Radio Receiver Supply Voltage Input. Bypass with 1μF to V _{SS} .
J11	B11	LXA	Switching Inductor Input A. Connect a 2.2μH inductor between LXA and LXB.
K10	A10	LXB	Switching Inductor Input B. Connect a 2.2μH inductor between LXA and LXB.
H10	C10	V _{BST}	The boosted supply voltage for the gate drive of high-side switches. Bypass V _{BST} to LXB with a 3.3nF capacitor.
J9	B9	V _{REGO_A}	Buck Converter A Voltage Output. Bypass with 22μF to V _{SS} , placed as close as possible to the V _{DDA} pin. Do not connect any other signal to this pin.
K9	A9	V _{REGO_B}	Buck Converter B Voltage Output. Bypass with 22μF to V _{SS} , placed as close as possible to the nearest V _{COREB} pin. Do not connect any other signal to this pin.
K8	A8	V _{REGO_C}	Buck Converter C Voltage Output. Bypass with 22μF to V _{SS} , placed as close as possible to the nearest V _{COREA} pin. Do not connect any other signal to this pin.
J8	B8	V _{REGO_D}	Buck Converter D Voltage Output. Bypass with 22μF to V _{SS} , placed as close as possible to the nearest V _{RXIN} or V _{TXIN} pin. Do not connect any other signal to this pin.
H8	C8	V _{DDA}	1.8V Analog/Digital Power Supply Input. Bypass with 1μF to V _{SS} .
J7	B7	V _{SSA}	Analog Ground
J6	B6	V _{TXOUT}	Radio Transmitter Supply Voltage Output. Bypass with 1μF to V _{SS} .
J5	B5	V _{RXOUT}	Radio Receiver Supply Voltage Output. Bypass with 1μF to V _{SS} .
A3, A11, B10, H9	C9, L3, L11, K10	V _{DDIO}	GPIO Supply Voltage Input. Bypass with 1μF to V _{SS} .
A2, A10, G9	D9, L2, L10	V _{DDIOH}	GPIO Supply Voltage Input, High. V _{DDIOH} ≥ V _{DDIO} . Bypass with 1μF to V _{SS} .
A6, B1, G10	D10, K1, L6	V _{COREA}	Digital Core Supply Voltage A Input. Bypass with 1μF to V _{SS} .
A7, C1, G11	D11, J1, L7	V _{COREB}	Digital Core Supply Voltage B Input. Bypass with 1μF to V _{SS} .
E10	G10	V _{DDB}	USB Transceiver Supply Voltage Input. See USB Design Considerations .
F10	F10	V _{SSB}	USB Transceiver Ground. Connect to V _{SS} .
J2	D2, D3	V _{DD_BT1}	0.9V Analog Power Supply for the Bluetooth Radio Low Noise Amplifier and Mixer. Connect to V _{RXOUT} . Bypass with 1μF to V _{SS} .
J3	C3	V _{DD_BT2}	1.1V Power Supply Input for the Bluetooth Radio Power Amplifier. Connect to V _{TXOUT} . Bypass with 1μF to V _{SS} .
G3	E1	V _{DD_BT3}	0.9V Power Supply Input for the Bluetooth Radio FRAC-N Divider. Connect to V _{RXOUT} . Bypass with 1μF to V _{SS} .
G1	D1	V _{DD_BT4}	0.9V Power Supply Input for the Bluetooth Radio Receiver Baseband. Connect to V _{RXOUT} . Bypass with 1μF to V _{SS} .
H2	A3	V _{DD_BT5}	0.9V Power Supply Input for the Bluetooth Radio Voltage-Controlled Oscillator. Connect to V _{RXOUT} . Bypass with 1μF to V _{SS} .
F4	D4, E3, E4	V _{SSA_BT0}	Bluetooth Radio Analog Ground 0. Connect to V _{SS} .
J1	B1, C2	V _{SSA_BT1}	Bluetooth Radio Analog Ground 1. Connect to V _{SS} .

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
K3	C4	V _{SSA_BT2}	Bluetooth Radio Analog Ground 2. Connect to V _{SS} .
G2	E2	V _{SSA_BT3}	Bluetooth Radio Analog Ground 3. Connect to V _{SS} .
H1	C1	V _{SSA_BT4}	Bluetooth Radio Analog Ground 4. Connect to V _{SS} .
H3	B3	V _{SSA_BT5}	Bluetooth Radio Analog Ground 5. Connect to V _{SS} .
CLOCK			
E1	F2	32KOUT	32kHz Crystal Oscillator Output
F1	F1	32KIN	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
J4	B4	HFXOUT	32MHz Crystal Oscillator Output
K4	A4	HFXIN	32MHz Crystal Oscillator Input. Connect a 32MHz crystal between HFXIN and HFXOUT for Bluetooth operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
USB			
E11	G11	DP	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled. See USB Design Considerations .
F11	F11	DM	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled. See USB Design Considerations .
TEST			
E7	G7	SWCLK	Serial Wire Debug Clock/TCK. This pin can also be configured as a GPIO.
H6	C6	SWDIO	Serial Wire Debug I/O/TMS. This pin can also be configured as a GPIO.
RESET			
H5	C5	RSTN	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V _{DDIO} supply.
GPIO AND ALTERNATE FUNCTION (See Applications Information for GPIO and Alternate Function Matrices.)			
B6	K6	P0.0	General-Purpose I/O, Port 0
B7	K7	P0.1	General-Purpose I/O, Port 0
C10	J10	P0.2	General-Purpose I/O, Port 0
C9	J9	P0.3	General-Purpose I/O, Port 0
B9	K9	P0.4	General-Purpose I/O, Port 0
A9	L9	P0.5	General-Purpose I/O, Port 0
A8	L8	P0.6	General-Purpose I/O, Port 0
B8	K8	P0.7	General-Purpose I/O, Port 0
F7	E7	P0.8	General-Purpose I/O, Port 0
G7	D7	P0.9	General-Purpose I/O, Port 0
E6	G6	P0.10	General-Purpose I/O, Port 0
F6	F6	P0.11	General-Purpose I/O, Port 0
E5	G5	P0.12	General-Purpose I/O, Port 0

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
D5	H5	P0.13	General-Purpose I/O, Port 0
F5	F5	P0.14	General-Purpose I/O, Port 0
G6	D6	P0.15	General-Purpose I/O, Port 0
B11	K11	P0.16	General-Purpose I/O, Port 0
D9	H9	P0.17	General-Purpose I/O, Port 0
E9	G9	P0.18	General-Purpose I/O, Port 0
C11	J11	P0.19	General-Purpose I/O, Port 0
D10	H10	P0.20	General-Purpose I/O, Port 0
F8	E8	P0.21	General-Purpose I/O, Port 0
F9	E9	P0.22	General-Purpose I/O, Port 0
G8	D8	P0.23	General-Purpose I/O, Port 0
E8	G8	P0.24	General-Purpose I/O, Port 0
D8	H8	P0.25	General-Purpose I/O, Port 0
C8	J8	P0.26	General-Purpose I/O, Port 0
D7	H7	P0.27	General-Purpose I/O, Port 0
C7	J7	P0.28	General-Purpose I/O, Port 0
D6	H6	P0.29	General-Purpose I/O, Port 0
C6	J6	P0.30	General-Purpose I/O, Port 0
B5	K5	P0.31	General-Purpose I/O, Port 0
A1, B2	K2	P1.0	General-Purpose I/O, Port 1
B3	K3	P1.1	General-Purpose I/O, Port 1
A4	L4	P1.2	General-Purpose I/O, Port 1
B4	K4	P1.3	General-Purpose I/O, Port 1
C5	J5	P1.4	General-Purpose I/O, Port 1
C4	J4	P1.5	General-Purpose I/O, Port 1
C3	J3	P1.6	General-Purpose I/O, Port 1
C2	J2	P1.7	General-Purpose I/O, Port 1
D4	H4	P1.8	General-Purpose I/O, Port 1
D1	H1	P1.9	General-Purpose I/O, Port 1
D3	H3	P1.10	General-Purpose I/O, Port 1
D2	H2	P1.11	General-Purpose I/O, Port 1
E2	E5	P1.12	General-Purpose I/O, Port 1
E3	E6	P1.13	General-Purpose I/O, Port 1
E4	G4	P1.14	General-Purpose I/O, Port 1
G5	D5	P1.15	General-Purpose I/O, Port 1
ANTENNA OUTPUT			
K2	B2	ANT	Antenna for Bluetooth radio. Attach the single-ended unbalanced Bluetooth radio antenna.
—	A2	ANT THRU	The single-ended unbalanced Bluetooth radio antenna circuit board trace uses this pin as a pass-through. Do not connect any other signal to this pin.

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
NO CONNECT			
—	F3, F4	D.N.C.	Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds.
—	L1	N.C.	No Connection. Not internally connected.

Detailed Description

MAX32665/MAX32666

The MAX32665/MAX32666 are Arm Cortex-M4 with FPU-based microcontrollers with 1MB flash and 560KB SRAM. They are ideal for wearable medical fitness applications. A second Arm Cortex-M4 with FPU supporting ROM and cache supports extended data processing capabilities such as audio processing for wireless Bluetooth applications.

The architecture includes a Bluetooth 5 Low Energy radio. The devices feature five powerful and flexible power modes. The flash memory is split into two banks of 512KB to provide flexibility when programming over the air. A built-in single inductor multiple output (SIMO) switch mode power supply allows the device to be optionally self-powered by a primary lithium cell. Dedicated hardware runs the Bluetooth 5 Low Energy stack freeing the CPUs for data processing tasks. Built-in dynamic clock gating and firmware-controlled power gating allow the user to optimize power for the specific application. Multiple SPI, UART, and I²C serial interfaces, 1-Wire Master, and USB 2.0 High-Speed Device interface allow interconnection to a wide variety of external sensors. An audio subsystem supports PDM, PCM, I²S, and TDM. An 8-input, 10-bit ADC is available to monitor analog input from external sensors and meters.

The MAX32666 incorporates a trust protection unit (TPU) with encryption and advanced security features. These features include a modular arithmetic accelerator (MAA) for fast ECDSA, a hardware AES engine, a hardware TRNG entropy generator, a SHA-2 accelerator, and a secure bootloader.

All devices are available in a 109-bump WLP with 0.35mm pitch and a 121-bump CTBGA with 0.65mm pitch packages.

Arm Cortex-M4 with FPU Processor

The Arm Cortex-M4 with FPU processors CPU0 and CPU1 are ideal for the emerging category of wearable medical and wellness applications. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned, data with or without saturation

Memory

Internal Flash Memory

1MB of internal flash memory provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 560KB SRAM provides low-power retention of application information in all power modes. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data-retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by retaining the most essential data only. SRAM can be expanded through the SPIXR SRAM serial interface supported by 16KB of cache. The SPIXR SRAM interface can address an additional 512MB.

Secure Digital Interface

The secure digital interface (SDI) provides high-speed, high-density data storage capability for media files and large long-term data logs. This interface supports eMMC, SD, SDHC, and SDXC memory devices at transfer rates up to 24MB/s. The 7-pin interface (4 data, 1 clock, 1 command, 1 write-protect) supports the following specifications:

- SD Host Controller Standard Specification Version 3.00
- SDIO Card Specification Version 3.0
- SD Memory Card Specification Version 3.01

- SD Memory Card Security Specification Version 1.01
- MMC Specification Version 4.51

Bluetooth 5

Bluetooth 5 Low Energy Radio

Bluetooth 5 Low Energy is the latest version of the Bluetooth wireless communication standard. It is used for wireless headphones and other audio hardware, as well as for communication between various smart home and Internet of Things (IoT) devices. Devices operate in the unlicensed 2.4GHz ISM (Industrial, Scientific, Medical) band. A frequency-hopping transceiver is used to combat interference and fading. The system operates in the 2.4GHz ISM band at 2400MHz–2483.5MHz. It uses 40 RF channels. These RF channels have center frequencies $2402 + k \times 2\text{MHz}$, where $k = 0, \dots, 39$. The Bluetooth stack runs on dedicated hardware so that CPU0 and CPU1 can be freed to run application code. The features of the radio include the following:

- Higher transmit power up to +4.5dbm
- 1Mbps, 2Mbps, and long range coded (125kbps and 500kbps)
- Increased broadcast capability
 - Advertising packet up to 255 bytes
- On-chip matching network to the antenna
- Provides hardware on-the-fly encryption and decryption for lower power consumption
- Low transmit current of 4.30mA at 0dbm at 3.3V
- Low receive current of 3.20mA at 3.3V
- Supports mesh networking
- Supports high-quality audio streaming (isochronous)

Bluetooth 5 Software Stack

A Bluetooth 5 software stack is available for application developers to quickly add support to devices. The Arm Cordio®-B50 software stack is provided in library form and provides application developers access to Bluetooth without validation and development of a software stack. The Cordio-B50 software stack interfaces to the Bluetooth link layer running on dedicated hardware. The dedicated hardware for the stack enables the ultimate in power management for IoT applications. Cordio-B50 features the following:

- C library for linking directly into an application development tool
- Change PHY Support
 - Host selects the PHY it needs to use at any given time enabling long range or higher bandwidth only when required
 - LE 1M
 - LE Coded S = 2
 - LE Coded S = 8
 - LE 2M
- Bluetooth 5 advertising extension support for enabling next generation Bluetooth beacons
 - Larger packets and advertising channel offloading
 - Packets up to 255 octets long
 - Advertising packet chaining
 - Advertising sets
 - Periodic advertising
 - High-duty cycle non-connectable advertising
 - Sample applications using standard profiles built on the Cordio-B50 software framework

Comparators

The eight AIN[7:0] inputs can be configured as four pairs and deployed as four independent comparators with the following features:

- Comparison events can trigger interrupts
- Events can wake the CPU from SLEEP, DEEPSLEEP, or BACKUP operating modes
- Can be active in all power modes

Dynamic Voltage Scaling Controller

The Dynamic Voltage Scaling (DVS) Controller works using the fixed high-speed oscillator and the V_{COREA} supply voltage to optimally operate the Arm core at the lowest practical voltage. The ability to adaptively adjust the voltage provides a significant reduction in dynamic power consumption.

The DVS Controller provides the following features:

- Controls DVS monitoring and adjustment functions
- Continuous monitoring with programmable monitor sample period
- Controlled transition to a programmable operating point
- Independent high and low operating limits for safe, bounded operation
- Independent high, center, and low operating range delay line delay monitors
- Programmable adjustment rate – when an adjustment is required
- Single clock operation
- APB interface provides IP control and status access
- Interrupt capability during error

Clocking Scheme

Multiple system clock sources are available to maximize performance and minimize power consumption:

- 96MHz high-frequency oscillator (f_{HSCLK} or IPO)
- 60MHz low-power oscillator (f_{LPCLK} or ISO)
- 8kHz nanoring oscillator (f_{NANO} or INRO)
- 32.768kHz RTC oscillator (external crystal required) (ERTCO)
- 7.3728MHz oscillator (f_{MCLK} or IBRO)
- 32MHz RF oscillator (external crystal required) (f_{RFCLK} or ERFO)

Some peripherals may have selectable clock sources that allow them to operate in low-power modes. An external 32.768kHz timebase is required when using the RTC. The audio interface is clocked by an external source on EXT_AUDCLK.

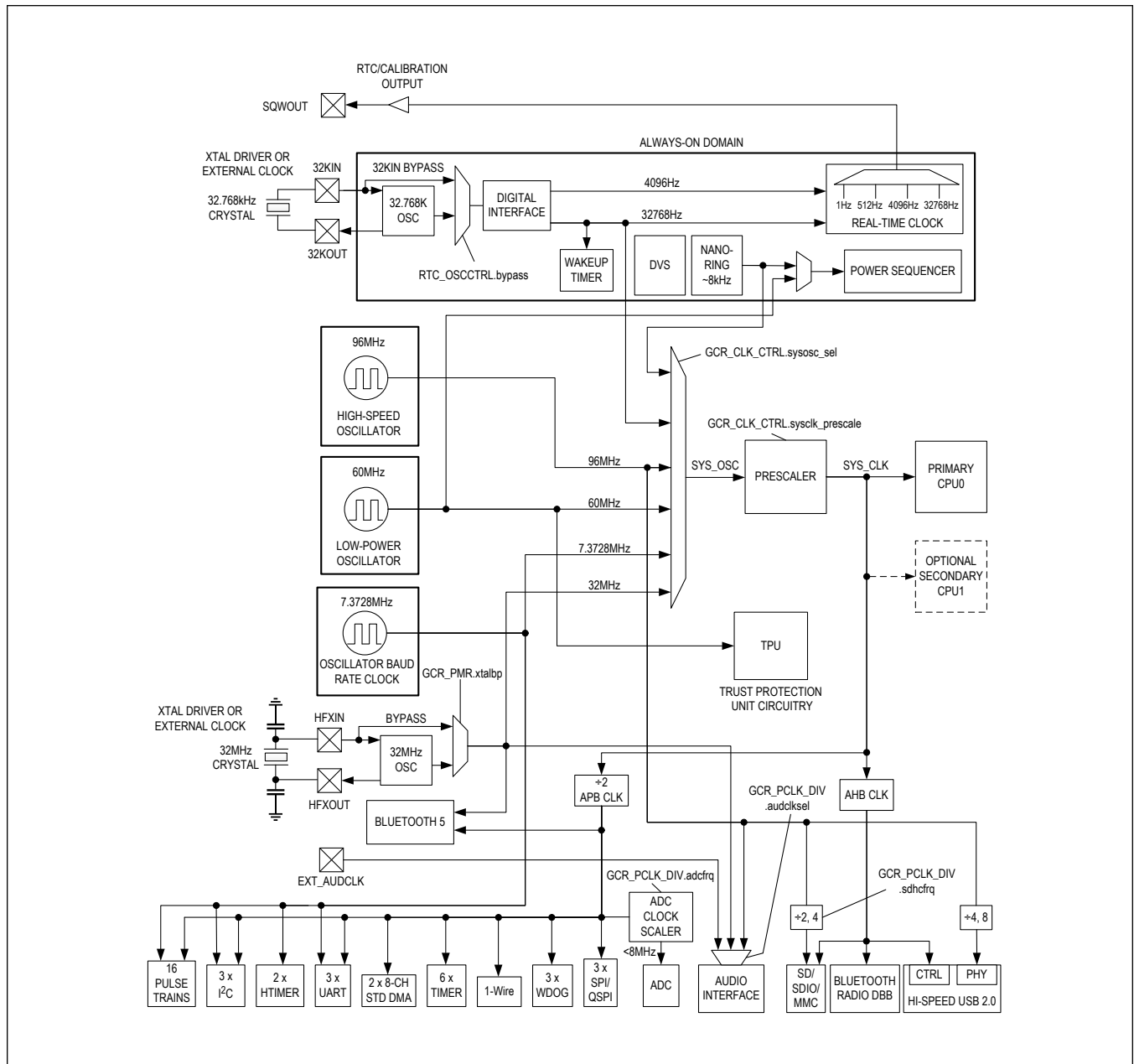


Figure 6. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more alternate functions associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Although this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the [Electrical Characteristics](#) tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be

independently enabled and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector.

When configured as GPIO, the following features are provided. The features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32665/MAX32666 provide up to 50 GPIO pins.

Analog-to-Digital Converter (ADC)

The 10-bit delta-sigma ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the eight external analog input signals (AIN0–AIN7) or the internal power supply inputs.

The reference for the ADC can be:

- Internal 1.22V bandgap
- V_{DDA} analog supply

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low-power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the CPU is in SLEEP or DEEPSLEEP mode. The eight AIN[7:0] inputs can be configured a four pairs and deployed as four independent comparators.

The ADC measures the following voltages:

- AIN[7:0] up to 3.3V
- V_{REGI}
- V_{TXOUT}
- V_{RXOUT}
- V_{COREA}
- V_{COREB}
- V_{DDIOH}
- V_{DDIO}
- V_{DDB}
- V_{DDA}

Single-Inductor Multiple-Output Switch-Mode Power Supply (SIMO SMPS)

The SIMO SMPS built into the device provides a monolithic power supply architecture for operation from a single lithium cell. The SIMO provides four buck regulator outputs that are voltage programmable. This architecture optimizes power consumption efficiency of the device and minimizes the bill of materials for the circuit design since only a single inductor/capacitor pair is required.

Power Management

Power Management Unit

The power management unit (PMU) provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPUs and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple power domains

- Fast wake-up of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption.

SLEEP Mode

This mode consumes less power, but wakes faster because the clocks can optionally be enabled.

The device status is as follows:

- CPU is asleep
- Peripherals are on
- Standard DMA blocks are available for optional use

DEEPSLEEP Mode

This mode corresponds to the Arm Cortex-M4 with FPU DEEPSLEEP mode. In this mode, CPU and critical peripheral configuration settings and all volatile memory is preserved.

The device status is a follows:

- CPU is off. System state and all SRAM is retained.
- The GPIO pins retain their state.
- The transition from DEEPSLEEP to ACTIVE mode is faster than the transition from BACKUP to ACTIVE mode because system initialization is not required.
- The system oscillators are all disabled to provide additional power savings over SLEEP mode:
 - 96MHz high-speed oscillator
 - 60MHz low-power oscillator
 - 7.3728MHz oscillator system clock shuts down.

BACKUP Mode

This mode places the CPUs in a static, low-power state that supports a fast wake-up to ACTIVE mode feature.

The device status is as follows:

- CPU is off. System state is not retained.
- Either 32KB, 64KB, or all the SRAM can be retained using the BACKUP recovery vector feature.
- The RTC can be enabled.

Wake-up Sources

The sources of wakeup from the SLEEP, DEEPSLEEP, and BACKUP operating modes can be summarized in [Table 1](#).

Table 1. MAX32665/MAX32666 Wake-up Sources

OPERATING MODE	WAKE-UP SOURCE
SLEEP	Interrupts (RTC, GPIO, USB, comparators, all peripherals), RSTN assertion, wake-up timer
DEEPSLEEP	Interrupts (RTC, GPIO, USB, comparators), RSTN assertion, wake-up timer
BACKUP	Interrupts (RTC, GPIO, USB, comparators), RSTN assertion, wake-up timer

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days.

When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed with a tick resolution of 244µs. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the [Electrical Characteristics](#) table.

The RTC calibration feature provides the ability for user software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the SQWOUT alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC polynomial is programmable to support custom CRC algorithms as well as the standard algorithms shown in [Table 2](#).

Table 2. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION
CRC-32-ETHERNET	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + x^0$
CRC-CCITT	$x^{16} + x^{12} + x^5 + x^0$
CRC-16	$x^{16} + x^{15} + x^5 + x^0$
USB Data	$x^{16} + x^{15} + x^5 + x^0$
Parity	$x^1 + x^0$

Programmable Timers

32-Bit Timer/Counter/PWM (TMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- Timer interrupt

A block diagram of the timer is shown in [Figure 7](#).

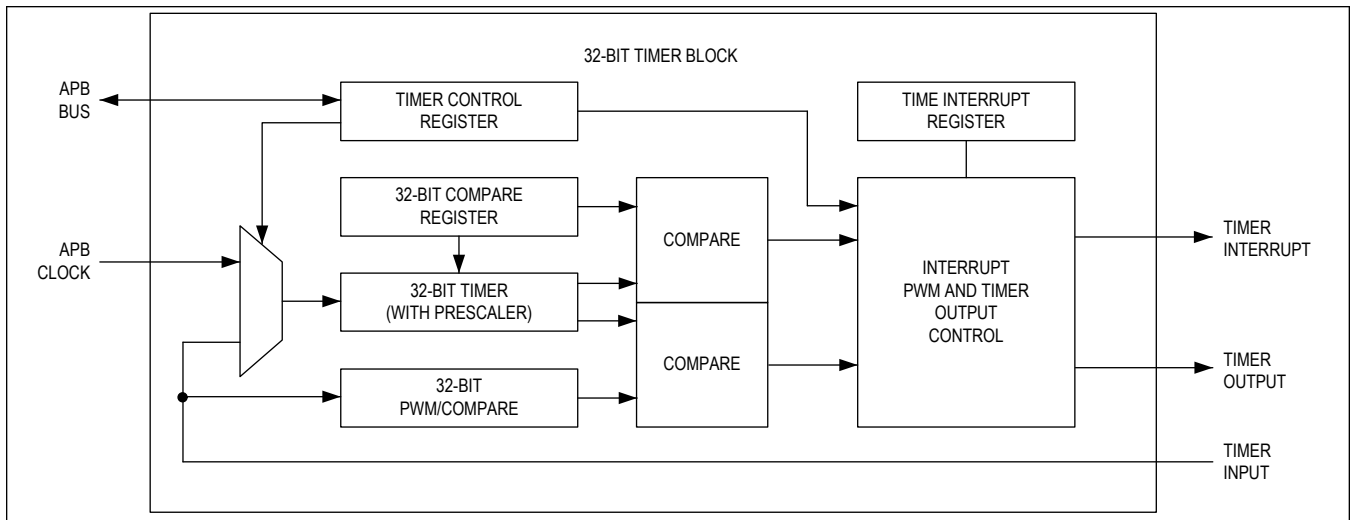


Figure 7. 32-Bit Timer

One or more instances of the peripheral are provided as shown in [Table 3](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 3. MAX32665/MAX32666 32-Bit Timer Instances

INSTANCE	SINGLE 32-BIT TIMER	POWER MODES	CLOCK SOURCE
TMR0	YES	ACTIVE SLEEP	PCLK
TMR1	YES	ACTIVE SLEEP	PCLK
TMR2	YES	ACTIVE SLEEP	PCLK
TMR3	YES	ACTIVE SLEEP	PCLK
TMR4	YES	ACTIVE SLEEP	PCLK
TMR5	YES	ACTIVE SLEEP	PCLK

Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the watchdog timer (WDT), which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. All instances are identical and independent of each other. Each has a dedicated reset bit, reset and/or interrupt enable bits, and status flags. They all share the same timebase, which is a scaled version of the system clock, but have independent prescale values.

When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution.

One or more instances of the peripheral are provided as shown in [Table 4](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 4. MAX32665/MAX32666 Watchdog Timer Instances

INSTANCE	POWER MODES	CLOCK
WDT0	ACTIVE SLEEP	PCLK
WDT1	ACTIVE SLEEP	PCLK
WDT2	ACTIVE SLEEP	PCLK

Pulse Train Engine (PT)

Multiple, independent pulse train generators can provide either a square wave or a repeating pattern from 2 to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Input pulse train module clock can be optionally configured to be independent from the system AHB clock
- Multiple repetition options
 - Single shot (nonrepeating pattern of 2 to 32 bits)
 - Pattern repeats user-configurable number of times or indefinitely
 - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

One or more instances of the peripheral are provided as shown in [Table 5](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 5. MAX32665/MAX32666 Pulse Train Instances

INSTANCES	POWER MODES	CLOCK SOURCE
PT[15:0]	ACTIVE SLEEP	PCLK

HTIMER

The HTIMER is a 44-bit timer that is driven by the 7.3728MHz source clock resulting in a tick resolution of 135.63ns. It is programmable to provide interrupts at count comparison.

One or more instances of the peripheral are provided as shown in [Table 6](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 6. MAX32665/MAX32666 HTIMER Instances

INSTANCES	POWER MODES	CLOCK SOURCE
HTMR0	ACTIVE SLEEP	IBRO
HTMR1	ACTIVE SLEEP	IBRO

Serial Peripherals

USB Controller

The integrated USB slave controller is compliant with the High-Speed (480Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. 11 endpoint buffers are a configurable selection of IN or OUT in addition to endpoint 0.

Audio Interface

The audio interface allows the device to communicate with external audio devices using standard I²S pulse-coded modulation (PCM) and pulse density modulation (PDM) audio interfaces in a slave-only configuration. This allows audio algorithms to be run such as dynamic speaker management (DSM) or ambient noise cancellation (ANC).

I²S PCM mode features the following:

- Single 4-wire I²S PCM interface allowing transmit and receive of audio data and is intended to connect to speaker driver devices
- Four transmit channels and eight receive channels are supported to allow 4-channel DSM
- Support four PDM receive channels at the same time as PCM support
- Sample rates from 8kHz to 192kHz

PDM mode features the following:

- Up to four PDM transmit channels at 3.072MHz
- Up to six PDM receive channels at 3.072MHz
- Interpolation and decimation filtering to save MIPS in the DSP

I²C Interface

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communication medium. The I²C master/slave interface to a wide variety of I²C-compatible peripherals. These engines support Standard mode, Fast mode, and Fast-mode Plus I²C speeds. It provides the following master or slave mode operation features:

- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed buses
- Multiple transfer rates
 - Standard mode: 100kbps
 - Fast mode: 400kbps
 - Fast-mode Plus: 1000kbps
 - High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

One or more instances of the peripheral are provided as shown in [Table 7](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 7. MAX32665/MAX32666 I²C Instances

INSTANCES	POWER MODES
I2C0	ACTIVE SLEEP
I2C1	ACTIVE SLEEP

Table 7. MAX32665/MAX32666 I²C Instances (continued)

I2C2	ACTIVE SLEEP
------	-----------------

Serial Peripheral Interface

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface between multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad data modes supported
- Multiple slave select lines on some instances
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing with respect to leading/trailing SCK edge

One or more instances of the peripheral are provided as shown in [Table 8](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 8. MAX32665/MAX32666 SPI Instances

INSTANCE	DATA	SLAVE SELECT LINES	MAXIMUM FREQUENCY (MASTER MODE) (MHz)	MAXIMUM FREQUENCY (SLAVE MODE) (MHz)
SPI0	3-wire, 4-wire, dual, or quad data support	3	48	48
SPI1	3-wire, 4-wire, dual, or quad data support	3	48	48
SPI2	3-wire, 4-wire, dual, or quad data support	3	48	48

SPI Execute in Place (SPIX) Master

There are two SPI execute in place (SPIX) master interfaces. One is dedicated for SRAM (SPIXR) and one is dedicated for flash (SPIXF) with dedicated slave selects. This allows the CPU to transparently execute instructions stored in an external SPI memory device. Instructions fetched through the SPI master are cached just like instructions fetched from internal program memory. The SPI SRAM master provides write-through capability. These two SPI execute in place master interfaces can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

UART

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) flow control signaling. Each UART is individually programmable.

The UART supports the following features:

- Baud rate generation with $\pm 2\%$ optionally utilizing the 7.3727MHz relaxation oscillator
- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO

- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

One or more instances of the peripheral are provided as shown in [Table 9](#). See the [Ordering Information](#) table for the specific instances available by part number.

Table 9. MAX32665/MAX32666 UART Instances

INSTANCE	FLOW CONTROL
UART0	Yes
UART1	Yes
UART2	Yes

1-Wire Master (OWM)

Analog Devices' 1-Wire bus consists of one signal that carries data and also supplies power to the slave devices and a ground return. The bus master communicates serially with one or more slave devices through the bidirectional, multidrop 1-Wire bus. The single contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire master supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The OWM supports both standard (15.6kbps) and overdrive (110kbps) speeds.

Standard DMA Controller

The standard DMA controller allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 8-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

The MAX32665/MAX32666 provide two instances of the standard DMA controller.

Trusted Protection Unit (TPU)

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application, providing random numbers that can be used for cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This is helpful in thwarting replay attacks or key search approaches. An effective true random number generator (TRNG) must be continuously updated by a high-entropy source.

The provided TRNG is continuously driven by a physically-unpredictable entropy source. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Analog Devices for details of compliance with specific standards.

MAA

The provided high-speed, hardware-based modulo arithmetic accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms. These include:

- 2048-bit DSA
- 4096-bit RSA
- Elliptic curve public key infrastructure

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

SHA-2

SHA-2 is a cryptographic hash function. It authenticates user data and verifies its integrity. It is used for digital signatures.

The device provides a hardware SHA-2 engine for fast computation of digests supporting:

- SHA-224
- SHA-256
- SHA-384
- SHA-512

Memory Decryption Integrity Unit (MDIU)

The external SPI flash can optionally be encrypted for additional security. Data can be transparently encrypted when it is loaded and decrypted on the fly. Encryption keys are stored in the always-on domain and preserved as long as V_{COREA} is present.

Software Integrity and Root of Trust

Root of Trust

On devices that support SCPBL, the root of trust starts with trusted software and the microcontroller's complement of security features. Communications between a host and the device must be secure and authenticated, and program integrity must be verified each time before execution to ensure the device's trustworthiness. The device's root of trust is based on a secret Analog Devices root verification key and a signed customer verification key (CVK). Customers submit their public CVK, which is then signed, and a certificate is sent back to the customer. This process is quick and required only once, before the software is released for the first time, and is unnecessary during the software development. A customer can then load their own key and download their signed binary executable code.

Secure Communications Protocol Bootloader (SCPBL)

On devices that support SCPBL, communication between a host system and the device uses a system of ECDSA-256 digitally signed packets. This guarantees the integrity and authenticity of all communication before executing configuration commands and the loading or verification of program memory. One or more serial interfaces are available for communication. This also enables the assembly and programming of the customer's final product by third-party assembly houses without the required cost and complexity of ensuring that the assembly house implements and maintains a secure production facility. It also allows for in-field software upgrades to deployed products, thus eliminating the costly need to return a product to the manufacturer for any software changes. The serial interfaces available for

SCPBL communication are shown in [Table 11](#). Following any reset or exit from certain low-power modes, the device tests the assigned stimulus pin and, if active, begins an SCPBL session. The stimulus pin can be reassigned once an SCPBL session begins. The host can disable the bootloader interface before deployment to prevent any changes to program memory.

See the [Ordering Information](#) table for availability.

Secure Boot

On devices that support SCPBL, the device performs a secure boot to confirm that the root of trust has not been compromised. Following every reset and exit from certain low-power modes, the secure boot verifies the digital signature of the program memory to confirm it has not been modified or corrupted, ensuring the trustworthiness of the application software. Failure to verify the digital signature transitions the device to safe mode, which prevents execution of the customer code. During the development phase, the bootloader can be reactivated and a new, trusted program memory loaded.

Applications Information

Bypass Capacitor Recommendations

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The [Pin Description](#) indicates which pins should be connected to bypass capacitors, the capacitance, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the [Pin Description](#) shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Place capacitors as close as possible to their corresponding device pins. Pins that recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

USB Design Considerations

If USB is not used, the DP and DM signals should be left unconnected, V_{DDB} should be tied to V_{SS} through a 500 Ω resistor, and V_{SSB} connected to V_{SS} .

The device does not provide a dedicated USB VBUS detect pin, so the 3.3V V_{DDB} supply input serves as both the power supply for the embedded USB transceiver and the detect for the VBUS signal. Voltage should be applied to the V_{DDB} pin only while the VBUS signal is present and removed whenever the VBUS signal is not present. [Figure 8](#) suggests two solutions.

1. Power can be controlled by connecting a 3.3V LDO regulator between VBUS and the V_{DDB} pin. The LDO requires a 1 μ F capacitor placed as close as possible to the LDO for proper operation. The 1 μ F capacitor can be omitted if the capacitor required by the USB specification is located close to the LDO.
2. V_{DDB} can be connected to a 3.3V supply through a load switch. The 5V-compatible enable of the load switch should be tied to VBUS. A 10k Ω resistor between VBUS and V_{SS} is required to discharge the capacitance on VBUS for the load switch enable.

In any implementation, bypass the V_{DDB} signal to V_{SSB} (or V_{SS} , if V_{SSB} is not pinned out) through an additional 1 μ F capacitor placed as close as possible to the V_{DDB} pin.

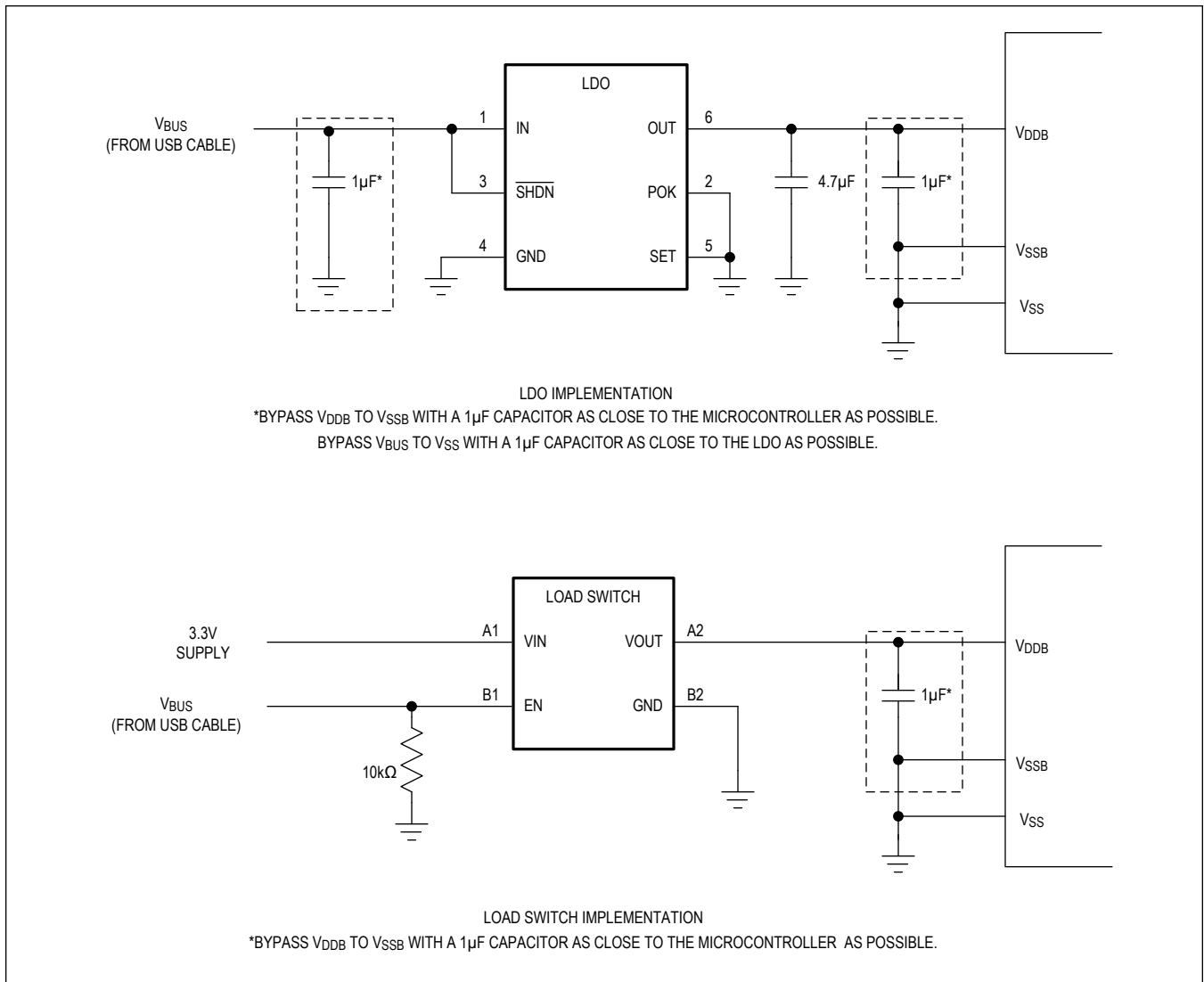


Figure 8. V_{DDB} Signal Implementation

V_{REG1} Design Considerations

The internal SIMO regulator requires one minimum $22\mu\text{F}$ capacitor between V_{REG1} and V_{SSPW} . Larger capacitance values improve decoupling for the SIMO regulator and reduce current peaks drawn from the battery.

Place the capacitor as close as possible to the pin shown in [Table 10](#). The ESR/ESL of the input capacitor should be very low (i.e., $\leq 5\text{m}\Omega + \leq 500\text{pH}$) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Table 10. MAX32665/MAX32666 V_{REG1} Capacitor Placement Priority

PACKAGE	PLACEMENT
109 WLP	H11
121 CTBGA	C11

Proper operation requires low inductance routing and minimization of the loop area between V_{REG1} , the capacitor, and the V_{SSPW} ground plane.

Transmitted Spurious Emissions

Various local regulatory agencies can impose limits on transmitted spurious emissions. At maximum output power of +4.5dbm, compliance with local regulations can require either an antenna with at least 6dB rejection at the 7.2GHz third harmonic or the use of a lowpass filter network between the device RF port and antenna. The MAX32665/MAX32666 are designed with an on-chip matching network providing a 50Ω impedance at the ANT device pin. Filter design must match this impedance for best efficiency.

Bootloader Activation

The SCPBL is activated following any reset or exiting certain low-power modes if the assigned stimulus pin is asserted. The design must ensure that the bootloader communication port shown in [Table 11](#) is available or the SCPBL cannot be activated.

Unlike other SCPBL implementations, the device does not use a default stimulus pin. A stimulus pin can be explicitly defined using the SCPBL WRITE_PARAMS command.

Until a stimulus pin is defined, the device will monitor UART0_RX for the transport layer SYNCH pattern. If the pattern is detected within 6s following a reset, the device will activate the SCPBL. If the pattern is not detected, the device will perform a secure boot.

Table 11. MAX32666 Bootloader Activation Summary

PART NUMBER	BOOTLOADER COMMUNICATION PORT		DEFAULT STIMULUS PIN
	RECEIVE	TRANSMIT	
MAX32666GWPBL	UART0_RX (P0.10)	UART0_TX (P0.9)	N/A

GPIO and Alternate Function Matrix

Table 12. GPIO and Alternate Function Matrix

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3	ALTERNATE FUNCTION 4	GPIOOUT_ENABLE	TTAP_ENABLE
P0.0	SPIXF_SS0		UART2_CTS	TMR0		
P0.1	SPIXF_MOSI/ SDIO0		UART2_TX	TMR1		
P0.2	SPIXF_MISO/ SDIO1		UART2_RX	TMR2		
P0.3	SPIXF_SCK		UART2_RTS	TMR3		
P0.4	SPIXF_SDIO2		OWM_IO	TMR4		
P0.5	SPIXF_SDIO3		OWM_PE	TMR5		
P0.6	I2C0_SCL		SWDIO2	TMR0		
P0.7	I2C0_SDA		SWCLK2	TMR1		
P0.8	SPIXR_SS0	QSPI0_SS0	UART0_CTS	TMR2		
P0.9	SPIXR_MOSI/ SDIO0	QSPI0_MOSI/ SDIO0	UART0_TX	TMR3		
P0.10	SPIXR_MISO/ SDIO1	QSPI0_MISO/ SDIO1	UART0_RX	TMR4		
P0.11	SPIXR_SCK	QSPI0_SCK	UART0_RTS	TMR5		
P0.12	SPIXR_SDIO2	QSPI0_SDIO2	OWM_IO	TMR0		
P0.13	SPIXR_SDIO3	QSPI0_SDIO3	OWM_PE	TMR1		
P0.14	I2C1_SCL	QSPI0_SS1		TMR2		
P0.15	I2C1_SDA	QSPI0_SS2		TMR3		
P0.16	AIN0/AIN0N	QSPI1_SS0	OWM_IO	TMR4		

Table 12. GPIO and Alternate Function Matrix (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3	ALTERNATE FUNCTION 4	GPIOOUT_ENABLE	TTAP_ENABLE
P0.17	AIN1/AIN0P	QSPI1_MOSI/ SDIO0	OWM_PE	TMR5		
P0.18	AIN2/AIN1N	QSPI1_MISO/ SDIO1		TMR0	PDOWN (active low)	
P0.19	AIN3/AIN1P	QSPI1_SCK		TMR1	SQWOUT	
P0.20	AIN4/AIN2N	QSPI1_SDIO2	UART1_RX	TMR2		
P0.21	AIN5/AIN2P	QSPI1_SDIO3	UART1_TX	TMR3		
P0.22	AIN6/AIN3N	QSPI1_SS1	UART1_CTS	TMR4		
P0.23	AIN7/AIN3P	QSPI1_SS2	UART1_RTS	TMR5	EXT_AUDCLK	
P0.24	PCM_LRCLK	QSPI2_SS0	OWM_IO	TMR0		
P0.25	PCM_DOUT	QSPI2_MOSI/ SDIO0	OWM_PE	TMR1		
P0.26	PCM_DIN	QSPI2_MISO/ SDIO1		TMR2	PDOWN (active low)	
P0.27	PCM_BCLK	QSPI2_SCK		TMR3	SQWOUT	
P0.28	PDM_DATA2	QSPI2_SDIO2	UART2_RX	TMR4		
P0.29	PDM_DATA3	QSPI2_SDIO3	UART2_TX	TMR5		
P0.30	PDM_RX_CLK	QSPI2_SS1	UART2_CTS	TMR0		
P0.31	PDM_MCLK	QSPI2_SS2	UART2_RTS	TMR1		
P1.0	SDHC_DAT3		SDMA_TMS	PT0		
P1.1	SDHC_CMD		SDMA_TDO	PT1		
P1.2	SDHC_DAT0		SDMA_TDI	PT2		
P1.3	SDHC_CLK		SDMA_TCK	PT3		
P1.4	SDHC_DAT1		UART0_RX	PT4		
P1.5	SDHC_DAT2		UART0_TX	PT5		
P1.6	SDHC_WP		UART0_CTS	PT6		
P1.7	SDHC_CDN		UART0_RTS	PT7		
P1.8	QSPI0_SS0			PT8		
P1.9	QSPI0_MOSI/ SDIO0			PT9		
P1.10	QSPI0_MISO/ SDIO1			PT10		
P1.11	QSPI0_SCK			PT11		
P1.12	QSPI0_SDIO2		UART1_RX	PT12		
P1.13	QSPI0_SDIO3		UART1_TX	PT13		
P1.14	I2C2_SCL		UART1_CTS	PT14		JTAG TDI
P1.15	I2C2_SDA		UART1_RTS	PT15		JTAG TDO
SWDIO	GPIO					
SWCLK	GPIO					

Ordering Information

PART	BLE	TMR	HTMR	WDT	I ² C	SPI	UART	PT	EXT ADC INPUTS	TPU	SCPBL	GPIO	PIN-PACKAGE
MAX32665GWPBT+*	Yes	6	2	3	3	3	3	16	8	No	No	50	109 WLP
MAX32665GWPBT+T*	Yes	6	2	3	3	3	3	16	8	No	No	50	109 WLP
MAX32665GXMBT+*	Yes	6	2	3	3	3	3	16	8	No	No	50	121 CTBGA
MAX32665GXMBT+T*	Yes	6	2	3	3	3	3	16	8	No	No	50	121 CTBGA
MAX32666GWP+	No	6	2	3	3	3	3	16	8	Yes	No	50	109 WLP
MAX32666GWP+T	No	6	2	3	3	3	3	16	8	Yes	No	50	109 WLP
MAX32666GWPBT+	Yes	6	2	3	3	3	3	16	8	Yes	No	50	109 WLP
MAX32666GWPBT+T	Yes	6	2	3	3	3	3	16	8	Yes	No	50	109 WLP
MAX32666GXMBT+	Yes	6	2	3	3	3	3	16	8	Yes	No	50	121 CTBGA
MAX32666GXMBT+T	Yes	6	2	3	3	3	3	16	8	Yes	No	50	121 CTBGA
MAX32666GWPBL+*	Yes	6	2	3	3	3	3	16	8	Yes	Yes	50	109 WLP
MAX32666GWPBL+T*	Yes	6	2	3	3	3	3	16	8	Yes	Yes	50	109 WLP
MAX32666GXMBL+	Yes	6	2	3	3	3	3	16	8	Yes	Yes	50	121 CTBGA
MAX32666GXMBL+T	Yes	6	2	3	3	3	3	16	8	Yes	Yes	50	121 CTBGA

All packages contain one RTC, USB 2.0 device, CRC accelerator, OWM, secure digital interface, and audio subsystem supporting I²S. BLE = Bluetooth Low Energy; TMR = 32-bit timer; HTMR = HTimer; WDT = watchdog timer; PT = pulse train generator; TPU = trusted protection unit; GPIO = general-purpose I/O pins.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel. Full reel.

*Future product—contact factory for availability.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	4/19	Updated Benefits and Features, Electrical Characteristics table, Pin Description, Bluetooth 5 Low Energy Radio, Bluetooth 5 Software Stack, and Ordering Information sections	1, 4, 7–9, 21, 25, 26, 37
2	8/19	Updated General Description, Electrical Characteristics table, Detailed Description, DeepSleep Mode, Backup Mode, I ² C Interface sections, and Table 4	1, 4, 5, 8, 24, 29, 35, 36
2.1		Corrected typos in the Electrical Characteristics table.	4
3	2/20	Updated Benefits and Features, Simplified Block Diagram, Electrical Characteristics table, Pin Description, Detailed Description, Bluetooth 5 Low Energy Radio, Bluetooth 5 Software Stack, Clocking Scheme, Figure 6, DeepSleep Mode, Backup Mode, Audio Interface, I ² C Interface, Bypass Capacitors, Transmitted Spurious Emissions, Table 4, and Ordering Information	1, 2, 10–17, 26–34, 36, 39, 43–45
4	4/20	Updated Absolute Maximum Ratings V _{DDB} and DM, DP signal descriptions. Updated the V _{REGI} Current, Backup Mode and V _{REGI} Fixed Current DeepSleep Mode Electrical Characteristics table specs. Updated the Parameter descriptions for USB in the Electrical Characteristics table. Updated the RSTN pin description in the Pin Descriptions table. Updated the Programmable Timers Detailed Description. Updated the Ordering Information table.	7, 9, 16, 28, 37, 45–46
5	1/21	Updated the Ordering Information table.	45
6	10/21	Updated secure bootloader and secure boot features in the <i>Detailed Description</i> , added external audio clock source to <i>Clocking Scheme Diagram</i> and <i>GPIO and Alternate Function Matrix</i> table. Corrected the polarity of differential inputs in the <i>GPIO and Alternate Function Matrix</i> table. Fixed typo V _{OH} V _{DDIOH} condition from 8mA to 4mA to match UG description. Removed all references to MAX32667 and MAX32668 which required changing all pages. Corrected UART baud rate to 921.6kBaud. Added Bootloader Activation to <i>Additional Information</i> .	All
7	2/23	Updated bypass capacitor requirements. Clarified the maximum voltage on any pin is 3.6V. Reduced maximum storage temperature to +125°C. Reduced maximum operating temperature to +85°C. Clarified that the BACKUP recovery vector feature preserves SRAM contents when exiting BACKUP. Added note to EC Table clarifying voltage sequencing of V _{DDA} and V _{REGI} supplies. Removed references maximum baud rate of UARTs from Table 3. Removed ECC support. Changed global EC header to "All specifications apply across the entire operating conditions range unless otherwise noted."; no change to product testing. Added design guidance sections for the use of V _{DDB} signal and V _{REGI} pins. Clarified the number of peripheral instances in the Detailed Description and the Ordering Information table. Clarified SCPBL and secure boot are activated following exit from certain low-power modes.	1, 2, 7–19, 25–27, 30, 32, 35–42

