19-0382; Rev 1; 8/95

MAXIM

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

General Description

The MAX624 is a dual DC-DC converter intended for size-constrained applications, such as power supplies that must fit inside PCMCIA memory cards. At the heart of the MAX624 are two boost-topology converters, plus auxiliary functions including a start-up inrush surge-current limiter and a power-on reset output with timer (power-good signal). The MAX624 accepts input voltages from 3V to 5.5V and generates two outputs: a fixed 5V ±4% output at 200mA (guaranteed), and an adjustable auxiliary output that is configurable for various loads with an external power transistor. The auxiliary output is typically set to 12V ±2% for flash memory applications, but can be adjusted via a resistor divider from V_{IN} to 30V or more.

The MAX624's high switching frequency (1MHz) reduces external component sizes. High-frequency switching losses have minimal impact on efficiency, which is 85% for the main 5V supply. Small ceramic filter capacitors, together with the soft-start function, reduce start-up inrush current surges.

Applications

PCMCIA Memory Cards

Solid-State Disk Drives

Host-Side PCMCIA Adapters

LCD Bias Power Supplies

Features

- ♦ **1MHz Switching Frequency for Small Components**
- ♦ **5V ±4% Boost Converter with Internal Power Switch**
- ♦ **Adjustable ±2% Output Boost Converter with External Power Switch**
- ♦ **Optional Inrush Surge-Current Limiting**
- ♦ **40µA Shutdown Current**
- ♦ **0.5mA Quiescent Current**
- ♦ **3.0V to 5.5V Input Range**
- ♦ **85% Main 5V SMPS Efficiency**
- ♦ **Independent Soft-Start for Each Supply**
- ♦ **Reset Output with 2.8V ±3% Threshold and 4ms Timeout**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX624C/D	0°C to +70°C	Dice*
MAX624ISE	-25°C to +85°C	16 Narrow SO

** Dice are tested at T_A = +25°C. Contact factory for dice specifications.*

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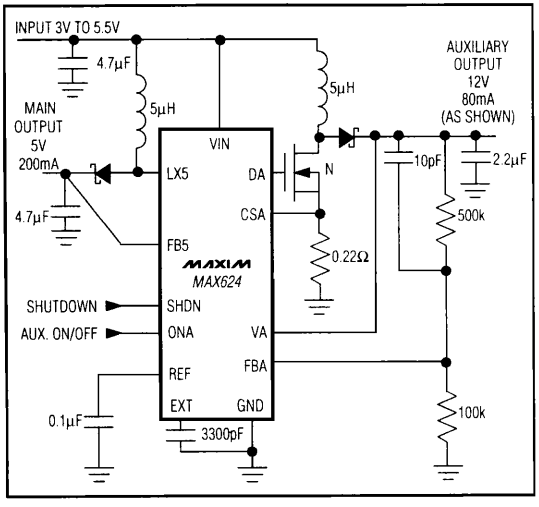
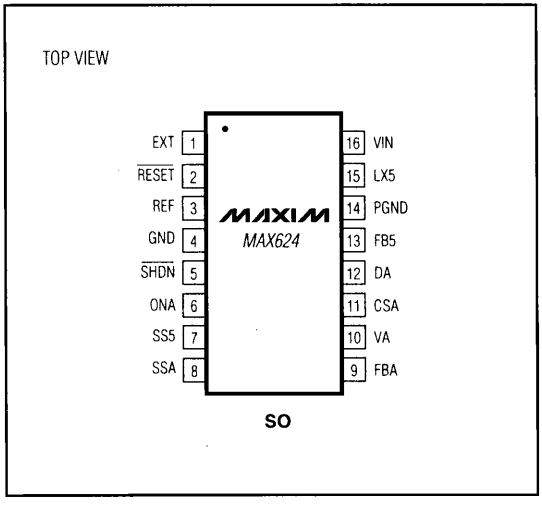
Typical Operating Circuit



Pin Configuration



Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

ABSOLUTE MAXIMUM RATINGS

VIN, FB5, LX5, $\overline{SHDN}$, ONA to GND .....-0.3V to 7V
$\overline{EXT}$ to GND .....-0.3V to 12V
$\overline{RESET}$, REF to GND .....-0.3V to (VIN + 0.3V)
PGND to GND .....±0.3V
SS5, SSA, DA, CSA, FBA to GND .....-0.3V to (FB5 + 0.3V)
VA to GND .....-0.3V to 17V

Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range
MAX624ISE .....-25°C to +85°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, GND = PGND = 0V, $\overline{SHDN}$ = V_{IN}, EXT open, FBA feedback resistors set for 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range		3.0		5.5	V
OUTPUT VOLTAGES					
5V Output Voltage		4.80		5.20	V
FBA Regulation Point		1.96		2.04	V
SUPPLY CURRENTS					
V_{IN} Shutdown Current	V_{IN} = 5.5V, $\overline{SHDN}$ = ONA = 0V		40	60	µA
V_{IN} Quiescent Current	Circuit of Figure 1, V_{IN} = 3.3V, ONA = 0V		500		µA
FB5 Quiescent Current	FB5 = 5.5V, $\overline{SHDN}$ = 3V, ONA = 0V		200	400	µA
VA Quiescent Current	FB5 = 5.5V, VA = 12.5V		30	60	µA
FB5 Shutdown Discharge Current	FB5 = 5V, V_{IN} = 3V, $\overline{SHDN}$ = 0V, internal V_{IN} to FB5 discharge switch	100	5000		µA
VA Shutdown Discharge Current	VA = 12V, V_{IN} = 3V, ONA = 0V, internal V_{IN} to VA discharge switch	5	15		µA
FBA Leakage Current	VA = 12V, FBA = 2.1V			100	nA
5V MAIN SMPS					
Line Regulation	3V < V_{IN} < 5.5V (Note 1)		0.03	0.2	%
Switch On-Resistance			0.33	0.6	Ω
Switch Leakage Current	LX5 = 7V			10	µA
Switch Current Limit		0.7	0.9	1.1	A
Switch On-Time Constant (K5)	3V < V_{IN} < 5V, t_{ON5} = K5 / V_{IN}	0.8	1.3	1.7	µs-V
Switch Off-Time Ratio (SR5)	3V < V_{IN} < 5V, FB5 = 5V (Note 2)	0.2		0.8	
Efficiency	Circuit of Figure 1, I_{LOAD} = 100mA		85		%
AUXILIARY SMPS CONTROLLER					
Line Regulation	3V < V_{IN} < 5.5V (Note 1)		0.03	0.2	%
Enable Trip Voltage Level	ONA input will be inhibited until FB5 rises above this level	3.5	4.0	4.5	V
CSA Bias Current				10	µA
CSA Current-Limit Threshold		180		220	mV
DA On-Resistance	FB5 = 5.5V		4	15	Ω
DA Drive Current	DA = 2.5V		0.5		A
Switch On-Time Constant (KA)	3V < V_{IN} < 5V, t_{ONA} = KA / V_{IN}	1.5	2.2	3.0	µs-V
Switch Off-Time Ratio (SRA)	3V < V_{IN} < 5V, 7V < FBA < 11V (Note 3)	0.2		0.9	
Efficiency	Circuit of Figure 1, I_{LOAD} = 60mA		75		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, GND = PGND = 0V, $\overline{SHDN}$ = V_{IN}, EXT open, FBA feedback resistors set for 12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START CONTROL					
Source Resistance	SS5, SSA; $\overline{SHDN}$ = ONA = 3V	14	20	28	kΩ
Discharge Resistance	SS5, SSA; $\overline{SHDN}$ = ONA = 0V		50	300	Ω
LOGIC INPUTS AND OUTPUTS					
Input Low Voltage	$\overline{SHDN}$, ONA			0.8	V
Input High Voltage	$\overline{SHDN}$, ONA	2			V
Input Leakage	$\overline{SHDN}$, ONA			±1	µA
Output Low Voltage	$\overline{RESET}$, I_{SINK} = 2mA, V_{IN} = 2.6V			0.4	V
Output High Voltage	$\overline{RESET}$, I_{SINK} = 1mA, V_{IN} = 3V	V_{IN} - 0.8			V
$\overline{RESET}$ Trip Level	Rising V_{IN} edge, typical hysteresis = 1%	2.7		2.9	V
$\overline{RESET}$ Timeout		2		10	ms
EXT Output Voltage	V_{IN} = 2.9V, I_{SOURCE} = 2µA	6.5			V
	V_{IN} = 5.5V, I_{SOURCE} = 0µA			11.8	
EXT Output Voltage in Reset	V_{IN} = 2V, I_{SINK} = 0.1mA			1	V

Note 1: Line Regulation is tested by measuring the reference line regulation, since both converters are supplied from the regulated 5V output.

Note 2: Switch off-time ratio guarantees that the inductor will go into continuous conduction. The ratio is tested for two cases for the main SMPS:

1) V_{IN} = 5V, FB5 = 5V SR5 = 0.120 x t_{OFF} / t_{ON}
2) V_{IN} = 3V, FB5 = 5V SR5 = 0.867 x t_{OFF} / t_{ON}

Note that the constants are calculated from: (FB5 + 0.6V - V_{IN}) / V_{IN}

Note 3: Switch off-time ratio guarantees that the inductor will go into continuous conduction. The ratio is tested for two cases for the auxiliary SMPS:

1) V_{IN} = 5V, VA = 7V SRA = 0.520 x t_{OFF} / t_{ON}
2) V_{IN} = 3V, VA = 11V SRA = 2.867 x t_{OFF} / t_{ON}

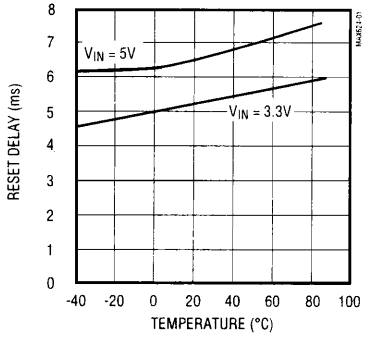
Note that the constants are calculated from: (VA + 0.6V - V_{IN}) / V_{IN}

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

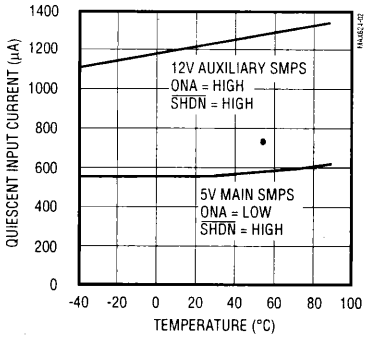
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

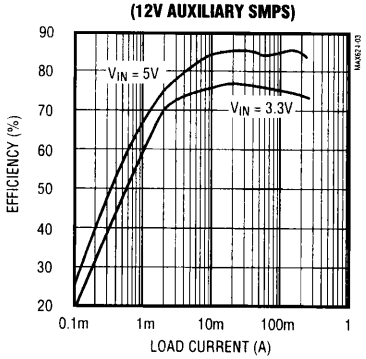
RESET DELAY vs. TEMPERATURE



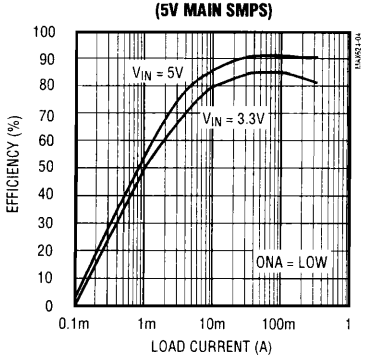
QUIESCENT INPUT CURRENT vs. TEMPERATURE



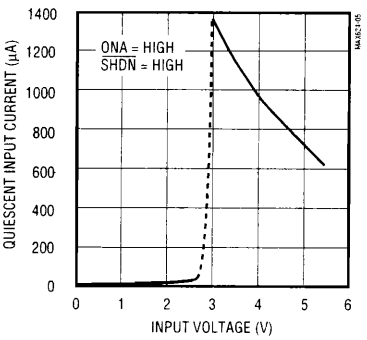
EFFICIENCY vs. LOAD CURRENT (12V AUXILIARY SMPS)



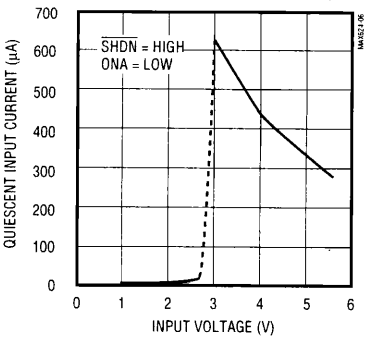
EFFICIENCY vs. LOAD CURRENT (5V MAIN SMPS)



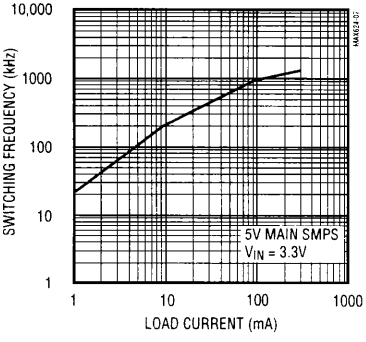
QUIESCENT INPUT CURRENT vs. INPUT VOLTAGE (12V AUXILIARY SMPS)



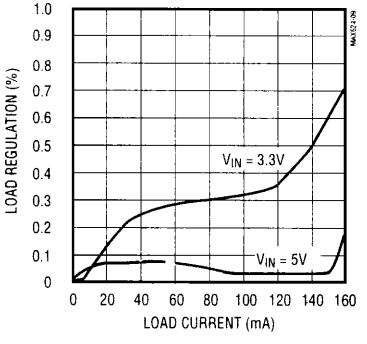
QUIESCENT INPUT CURRENT vs. INPUT VOLTAGE (5V MAIN SMPS)



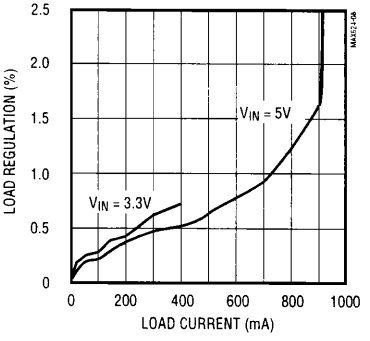
SWITCHING FREQUENCY vs. LOAD CURRENT



LOAD REGULATION vs. LOAD CURRENT (12V AUXILIARY SMPS)



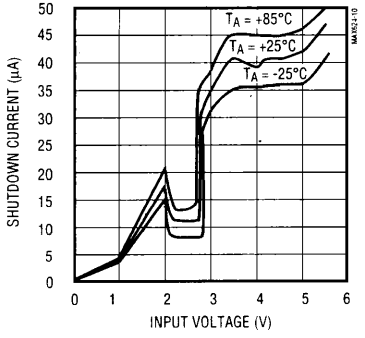
LOAD REGULATION vs. LOAD CURRENT (5V MAIN SMPS)



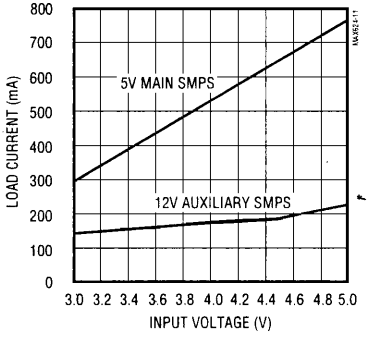
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

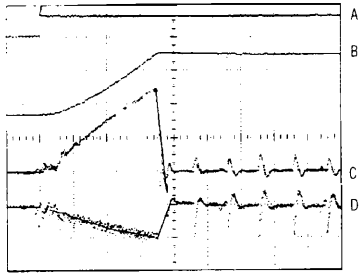
SHUTDOWN CURRENT vs. INPUT VOLTAGE



LOAD CURRENT CAPABILITY vs. INPUT VOLTAGE



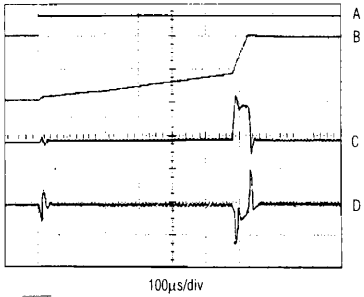
START-UP WAVEFORMS (12V AUXILIARY SMPS)
(V_{IN} = 3.3V, I_{LOAD} = 1.2mA, $\overline{SHDN}$ = HIGH)



100µs/div

A: ONA (5V/div)
B: 12V AUXILIARY SMPS (5V/div)
C: I_{IN} (200mA/div)
D: $V_{SWITCHED}$ (100mV/div, AC-COUPLED)

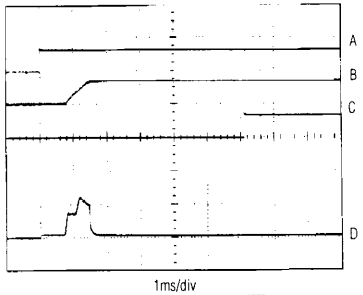
START-UP WAVEFORMS (5V MAIN SMPS)
(V_{IN} = 3.3V, I_{LOAD} = 0A, ONA = LOW)



100µs/div

A: $\overline{SHDN}$ (5V/div)
B: 5V MAIN SMPS (1V/div)
C: I_{IN} (200mA/div)
D: $V_{SWITCHED}$ (100mV/div, AC-COUPLED)

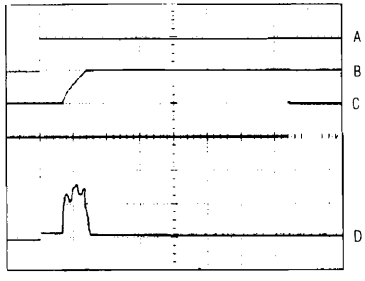
START-UP INRUSH CURRENT (V_{IN} = 3.3V)
(I_{LOAD} = 5mA, $\overline{SHDN}$ = ONA = LOW)



1ms/div

A: V_{IN} (5V/div)
B: $V_{SWITCHED}$ (5V/div)
C: $\overline{RESET}$ (5V/div)
D: I_{IN} (50mA/div)

START-UP INRUSH CURRENT (V_{IN} = 5V)
(I_{LOAD} = 5mA, $\overline{SHDN}$ = ONA = LOW)



1ms/div

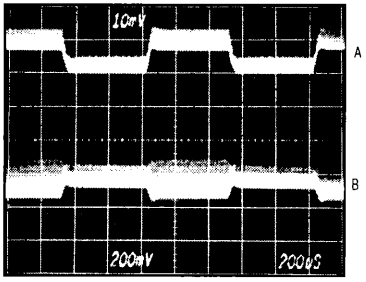
A: V_{IN} (5V/div)
B: $V_{SWITCHED}$ (5V/div)
C: $\overline{RESET}$ (5V/div)
D: I_{IN} (50mA/div)

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Typical Operating Characteristics (continued)

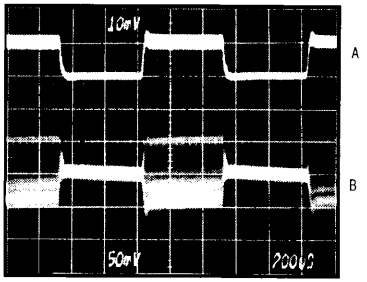
(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (12V AUXILIARY SMPS)



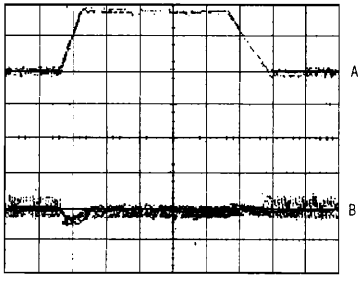
A: I_{LOAD} = 0mA to 80mA
B: 12V AUXILIARY SMPS (200mV/div, AC-COUPLED)

LOAD-TRANSIENT RESPONSE (5V MAIN SMPS)



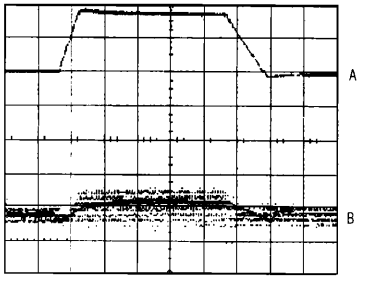
A: I_{LOAD} = 0mA to 200mA
B: 5V MAIN SMPS (50mV/div, AC-COUPLED)

LINE-TRANSIENT RESPONSE (12V AUXILIARY SMPS)



I_{LOAD} = 20mA
A: V_{IN} = 3.3V to 5V
B: 12V AUXILIARY OUTPUT (200mV/div, AC-COUPLED)

LINE-TRANSIENT RESPONSE (5V MAIN SMPS)



I_{LOAD} = 40mA
A: V_{IN} = 3.3V to 5V
B: 5V MAIN OUTPUT (50mV/div, AC-COUPLED)

Pin Description

PIN	NAME	FUNCTION
1	EXT	Gate-Drive Output. Drives inrush surge-current limiting MOSFET. EXT is fed by an internal charge-pump tripler that swings from GND to V_{IN} x 3.
2	$\overline{RESET}$	Power-On Reset Output. Low when V_{IN} < 2.8V and for 4ms after V_{IN} > 2.8V. EXT is low when $\overline{RESET}$ is low. Swings from GND to V_{IN}.
3	REF	2V Reference Output. Bypass to GND with 0.1µF. No external load current is allowed.
4	GND	Quiet Analog Ground and Low-Side Current-Sense Input for Auxiliary SMPS
5	$\overline{SHDN}$	Shutdown. Disables both SMPSs when low. In shutdown, the surge-protection input MOSFET is kept on.
6	ONA	On/Off Control Input for Auxiliary SMPS, low = off
7	SS5	Soft-Start Input for 5V Main SMPS. An external soft-start capacitor varies the 5V start-up time. Ramp time to full current limit is approximately 50µs per nF of soft-start capacitance.
8	SSA	Soft-Start Input for Auxiliary SMPS. An external soft-start capacitor varies the auxiliary SMPS start-up time. Ramp time to full current limit is approximately 50µs per nF of soft-start capacitance.
9	FBA	Feedback Input for Auxiliary SMPS. Regulates around REF (2V nominal). FBA is a high-impedance CMOS input.
10	VA	Output Voltage Sense Input for Auxiliary SMPS. The only purpose of this pin is to set the SMPS timing algorithm. Internally, VA connects to the top of a 250kΩ ±30% resistor that connects to V_{IN}.
11	CSA	Current-Sense Input for Auxiliary SMPS. Current-limit threshold is 200mV nominal with respect to GND.
12	DA	Gate-Drive Output for Auxiliary SMPS. Swings 0V to FB5.
13	FB5	Feedback Input for 5V Main SMPS. FB5 also serves as the supply voltage rail for much of the internal circuitry for both SMPSs (bootstrap supply input).
14	PGND	Power Ground, source connection for the main 5V SMPS power MOSFET
15	LX5	Drain Connection for 5V Main SMPS Power MOSFET
16	VIN	Input Supply Voltage from the External Supply. Normal operating range is 3V to 5.5V.

Dual-Output, 1MHz DC-DC Boost Converter for PCMCIA Applications

Standard Application Circuit

In the standard application circuit (Figure 1), the MAX624 generates 5V at 200mA (guaranteed) and 12V at 80mA from a 3.3V or 5V input, and includes soft-start and inrush surge-current limiting features. Successful use of the circuit does not require calculations; use the values given in Figure 1. For more detailed applications information, see the *Design Procedure for Main and Auxiliary SMPS.*

Detailed Description

The MAX624 is a dual-output DC-DC boost converter. The device accepts input voltages from 3V to 5.5V and generates two outputs: a 5V output at 200mA, and an adjustable output (i.e. 12V or 30V). The main 5V output has an internal MOSFET switch and current-sense resistor (0.15Ω), which senses the output current and triggers the current-limit comparator. The auxiliary SMPS's current-limit resistor and MOSFET switch are external to the device. The current-limit voltage of the auxiliary SMPS is 200mV. Both the main and auxiliary SMPS have a soft-start feature that varies the start-up time of the outputs. The SS output source impedance of the two outputs is 20kΩ to charge the external SS capacitor to 150mV (5V output) or 200mV (auxiliary output). The impedance of the SS pin when the device is in reset (5V) and when ONA = low (auxiliary) is 50Ω to GND. Full current limit is reached at a 50µs/nF rate.

To prevent surge currents when the card is plugged into a live socket, this device is capable of driving an external high-side N-channel MOSFET in series with the main V_{CC} supply to the card. The EXT pin drives the gate of the external MOSFET and is fed by an internal charge-pump tripler that delivers three-times V_{IN}, even in shutdown mode. The output source impedance of EXT is approximately 100kΩ, and has an active pull-down.

The SS capacitor and the external inrush-limiting MOSFET are optional components, not necessary unless inrush current is a concern. However, do not remove C9.

When the MAX624 is in reset, the FB5 and VA outputs are discharged to V_{IN} via two internal switches (Figure 2). Discharging the output capacitors to a low voltage level protects against false programming of flash memory chips.

5V Main SMPS

The main output is powered from the FB5 pin (i.e., bootstrapped) for higher speed and lower on-resistance of the power MOSFET. This SMPS consists of an error comparator, an output undervoltage-lockout comparator (set at 4V output), a timing generator for t_{ON} and t_{OFF}, a current-limit comparator, a MOSFET driver, and the power switch (Figure 2).

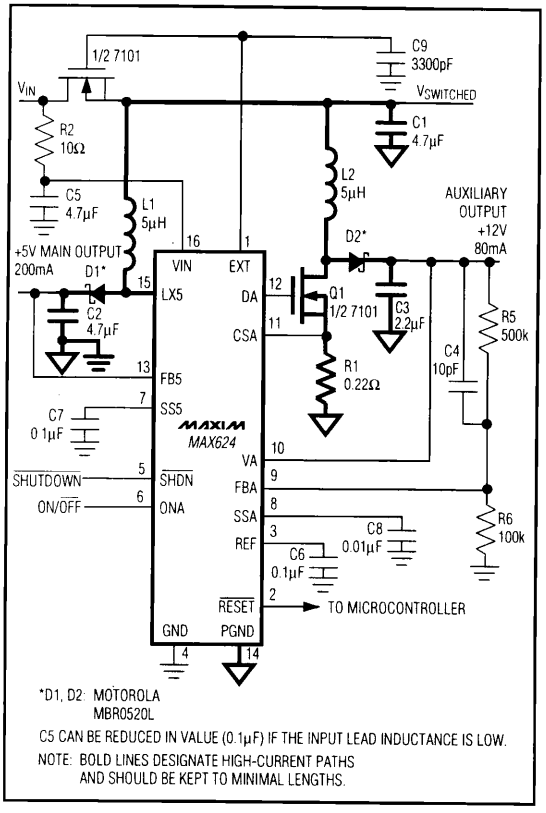


Figure 1. Standard Application Circuit

The error comparator's noninverting input voltage is internally set to V_{REF}. FB5's voltage is scaled internally, so that when it exceeds 5V the comparator output trips and shuts down the PFM.

Leaving only the error comparator on when the switch is off keeps the quiescent current low. The current comparator is powered up after the switch is turned on. This provides leading-edge blanking on the current comparator, in order to filter noise spikes caused by switch gate capacitance so they don't trip the overcurrent comparator and turn off the switch.

The main PFM has an undervoltage-lockout circuit that trips at 4V (preset internal threshold). Until the 4V threshold is reached, the timing generator is disabled and a 100kHz start-up oscillator is used to generate the output.