



Dual-Phase, Parallelable, Average Current-Mode Controllers

MAX5038/MAX5041

General Description

The MAX5038/MAX5041 dual-phase, PWM controllers provide high-output-current capability in a compact package with a minimum number of external components. The MAX5038/MAX5041 utilize a dual-phase, average current-mode control that enables optimal use of low $R_{DS(ON)}$ MOSFETs, eliminating the need for external heatsinks even when delivering high output currents.

Differential sensing enables accurate control of the output voltage, while adaptive voltage positioning provides optimum transient response. An internal regulator enables operation with input voltage ranges of +4.75V to +5.5V or +8V to +28V. The high switching frequency, up to 500kHz per phase, and dual-phase operation allow the use of low-output inductor values and input capacitor values. This accommodates the use of PC board-embedded planar magnetics achieving superior reliability, current sharing, thermal management, compact size, and low system cost.

The MAX5038/MAX5041 also feature a clock input (CLKIN) for synchronization to an external clock, and a clock output (CLKOUT) with programmable phase delay (relative to CLKIN) for paralleling multiple phases. The MAX5038 offers a variety of factory-trimmed preset output voltages (see *Selector Guide*) and the MAX5041 offers an adjustable output voltage from +1.0V to +3.3V.

The MAX5038/MAX5041 operate over the extended industrial temperature range (-40°C to +85°C) and are available in a 28-pin SSOP package. Refer to the MAX5037 data sheet for a VRM 9.0-compatible, VID-controlled output voltage controller in a 44-pin MQFP or QFN package.

Applications

Servers and Workstations
 Point-Of-Load High-Current/High-Density
 Telecom DC-DC Regulators
 Networking Systems
 Large-Memory Arrays
 RAID Systems
 High-End Desktop Computers

Features

- ◆ **+4.75V to +5.5V or +8V to +28V Input Voltage Range**
- ◆ **Up to 60A Output Current**
- ◆ **Internal Voltage Regulator for a +12V or +24V Power Bus**
- ◆ **True Differential Remote Output Sensing**
- ◆ **Two Out-Of-Phase Controllers Reduce Input Capacitance Requirement and Distribute Power Dissipation**
- ◆ **Average Current-Mode Control**
 Superior Current Sharing Between Individual Phases and Paralleled Modules
 Accurate Current Limit Eliminates MOSFET and Inductor Derating
- ◆ **Integrated 4A Gate Drivers**
- ◆ **Selectable Fixed Frequency 250kHz or 500kHz Per Phase (Up to 1MHz for 2 Phases)**
- ◆ **Fixed (MAX5038) or Adjustable (MAX5041) Output Voltages**
- ◆ **0.5% Accurate Reference (MAX5041B)**
- ◆ **External Frequency Synchronization from 125kHz to 600kHz**
- ◆ **Internal PLL with Clock Output for Paralleling Multiple DC-DC Converters**
- ◆ **Thermal Protection**
- ◆ **28-Pin SSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OUTPUT VOLTAGE
MAX5038EAI12	-40°C to +85°C	28 SSOP	Fixed +1.2V
MAX5038EAI15	-40°C to +85°C	28 SSOP	Fixed +1.5V
MAX5038EAI18	-40°C to +85°C	28 SSOP	Fixed +1.8V
MAX5038EAI25	-40°C to +85°C	28 SSOP	Fixed +2.5V
MAX5038EAI33	-40°C to +85°C	28 SSOP	Fixed +3.3V
MAX5041EAI	-40°C to +85°C	28 SSOP	Adj +1.0V to +3.3V
MAX5041BEAI	-40°C to +85°C	28 SSOP	Adj +1.0V to +3.3V

Pin Configuration appears at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

IN to SGND	-0.3V to +30V
BST_ to SGND	-0.3V to +35V
DH_ to LX_	-0.3V to [(V _{BST_} - V _{LX_}) + 0.3V]
DL_ to PGND	-0.3V to (V _{CC} + 0.3V)
BST_ to LX_	-0.3V to +6V
V _{CC} to SGND	-0.3V to +6V
V _{CC} to PGND	-0.3V to +6V
SGND to PGND	-0.3V to +0.3V

All Other Pins to SGND	-0.3V to (V _{CC} + 0.3V)
Continuous Power Dissipation (T _A = +70°C)	
28-Pin SSOP (derate 9.5mW/°C above +70°C)	762mW
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V _{IN}		8		28	V
		Short IN and V _{CC} together for +5V input operation	4.75		5.5	
Quiescent Supply Current	I _Q	EN = V _{CC} or SGND		4	10	mA
Efficiency	η	I _{LOAD} = 52A (26A per phase)		90		%
OUTPUT VOLTAGE						
Nominal Output Voltage Accuracy		MAX5038 only, no load	-0.8		+0.8	%
		MAX5038 only, no load, V _{IN} = V _{CC} = +4.75V to +5.5V or V _{IN} = +8V to +28V (Note 2)	-1		+1	
SENSE+ to SENSE- Voltage Accuracy		MAX5041 only, no load	0.992		1.008	V
		MAX5041 only, no load, V _{IN} = V _{CC} = +4.75V to +5.5V or V _{IN} = +8V to +28V	0.990		1.010	
		MAX5041B only, no load	0.995		1.005	
		MAX5041B only, no load, V _{IN} = +8V to +28V	0.995		1.005	
STARTUP/INTERNAL REGULATOR						
V _{CC} Undervoltage Lockout	UVLO	V _{CC} falling	4.0	4.15	4.5	V
V _{CC} Undervoltage Lockout Hysteresis				200		mV
V _{CC} Output Accuracy		V _{IN} = +8V to +28V, I _{SOURCE} = 0 to 80mA	4.85	5.1	5.30	V
MOSFET DRIVERS						
Output Driver Impedance	R _{ON}	Low or high output		1	3	Ω
Output Driver Source/Sink Current	I _{DH_} , I _{DL_}			4		A
Non-Overlap Time	t _{NO}	C _{DH_/DL_} = 5nF		60		ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR AND PLL						
Switching Frequency	f _{SW}	CLKIN = SGND	238	250	262	kHz
		CLKIN = V _{CC}	475	500	525	
PLL Lock Range	f _{PLL}		125		600	kHz
PLL Locking Time	t _{PLL}			200		μs
CLKOUT Phase Shift (at f _{SW} = 125kHz)	∅ _{CLKOUT}	PHASE = V _{CC}	115	120	125	degrees
		PHASE = unconnected	85	90	95	
		PHASE = SGND	55	60	65	
CLKIN Input Pulldown Current	I _{CLKIN}		3	5	7	μA
CLKIN High Threshold	V _{CLKINH}		2.4			V
CLKIN Low Threshold	V _{CLKINL}				0.8	V
CLKIN High Pulse Width	t _{CLKIN}		200			ns
PHASE High Threshold	V _{PHASEH}		4			V
PHASE Low Threshold	V _{PHASEL}				1	V
PHASE Input Bias Current	I _{PHASEBIA}		-50		+50	μA
CLKOUT Output Low Level	V _{CLKOUTL}	I _{SINK} = 2mA (Note 2)			100	mV
CLKOUT Output High Level	V _{CLKOUTH}	I _{SOURCE} = 2mA (Note 2)	4.5			V
CURRENT LIMIT						
Average Current-Limit Threshold	V _{CL}	CSP_ to CSN_	45	48	51	mV
Cycle-by-Cycle Current Limit	V _{CLPK}	CSP_ to CSN_ (Note 3)	90	112	130	mV
Cycle-by-Cycle Overload Response Time	t _R	V _{CSP_} to V _{CSN_} = +150mV		260		ns
CURRENT-SENSE AMPLIFIER						
CSP_ to CSN_ Input Resistance	R _{CS_}			4		kΩ
Common-Mode Range	V _{CMR(CS)}		-0.3		+3.6	V
Input Offset Voltage	V _{OS(CS)}		-1		+1	mV
Amplifier Gain	A _{V(CS)}			18		V/V
3dB Bandwidth	f _{3dB}			4		MHz
CURRENT-ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)						
Transconductance	g _{mca}			550		μS
Open-Loop Gain	A _{VOL(CE)}	No load		50		dB
DIFFERENTIAL VOLTAGE AMPLIFIER (DIFF)						
Common-Mode Voltage Range	V _{CMR(DIFF)}		-0.3		+1.0	V
DIFF Output Voltage	V _{CM}	V _{SENSE+} = V _{SENSE-} = 0		0.6		V
Input Offset Voltage	V _{OS(DIFF)}		-1		+1	mV
Amplifier Gain	A _{V(DIFF)}	MAX5038/MAX5041 (+1.2V, +1.5V, +1.8V output versions)	0.997	1	1.003	V/V
		MAX5038 (+2.5V and +3.3V output versions)	0.495	0.5	0.505	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +5V$, circuit of Figure 1, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical specifications are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3dB Bandwidth	f_{3dB}	$C_{DIFF} = 20pF$		3		MHz
Minimum Output Current Drive	$I_{OUT(DIFF)}$		1.0			mA
SENSE+ to SENSE- Input Resistance	$R_{VS_}$		50	100		$k\Omega$
VOLTAGE-ERROR AMPLIFIER (EAOUT)						
Open-Loop Gain	$A_{VOL(EA)}$			70		dB
Unity-Gain Bandwidth	f_{UGEA}			3		MHz
EAN Input Bias Current	$I_{B(EA)}$	$V_{EAN} = +2.0V$	-100		+100	nA
Error-Amplifier Output Clamping Voltage	$V_{CLAMP(EA)}$	With respect to V_{CM}	810		918	mV
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}			150		$^{\circ}C$
Thermal-Shutdown Hysteresis				8		$^{\circ}C$
EN INPUT						
EN Input Low Voltage	V_{ENL}				1	V
EN Input High Voltage	V_{ENH}		3			V
EN Pullup Current	I_{EN}		4.5	5	5.5	μA

Note 1: Specifications from $-40^{\circ}C$ to $0^{\circ}C$ are guaranteed by characterization but not production tested.

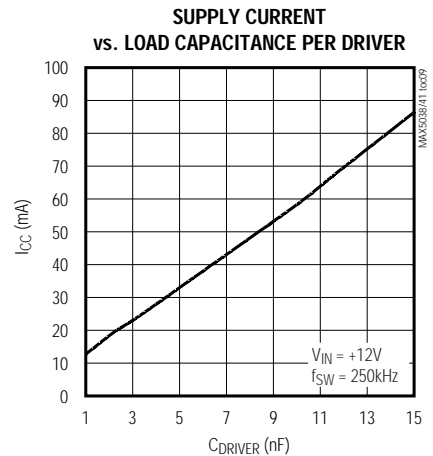
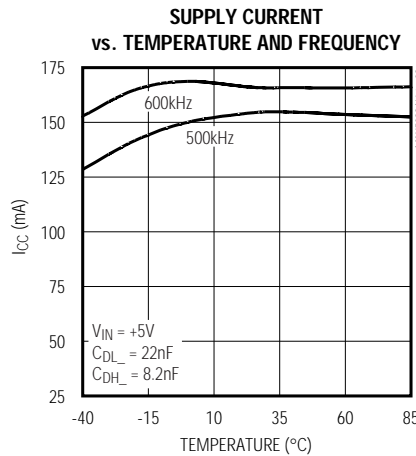
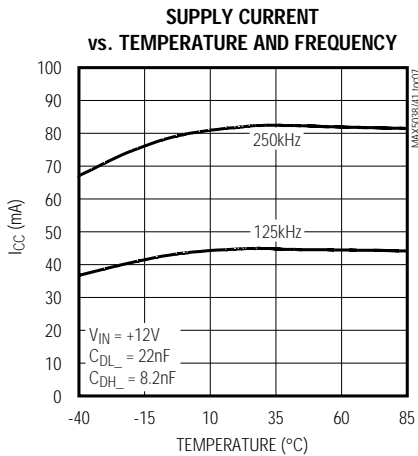
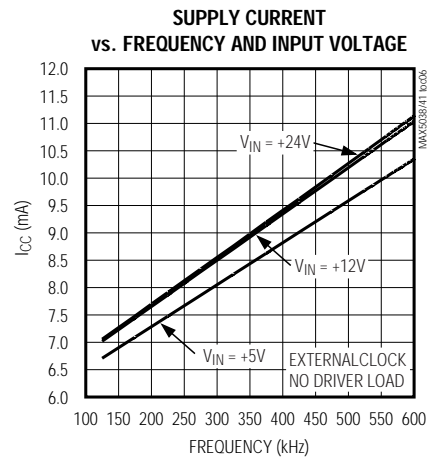
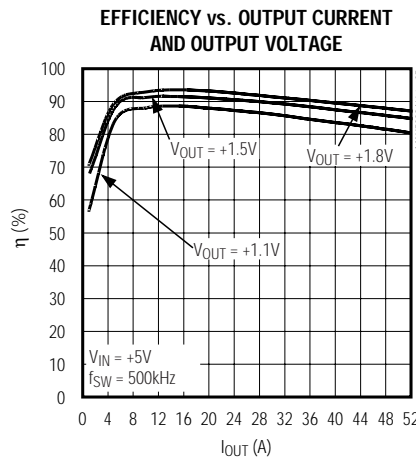
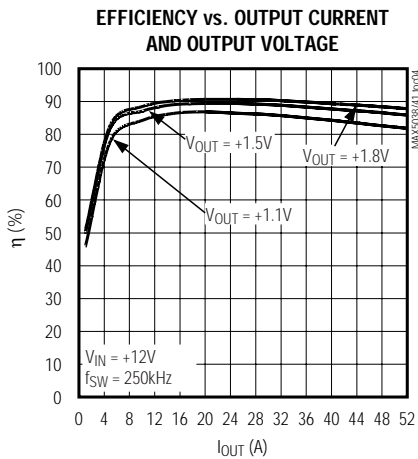
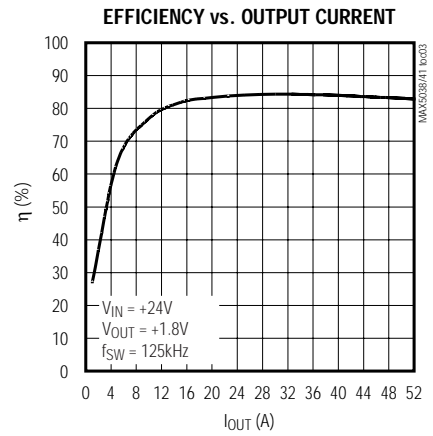
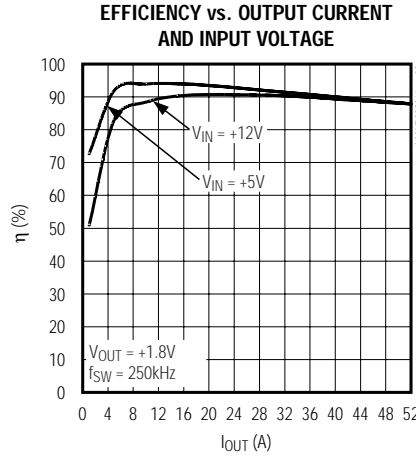
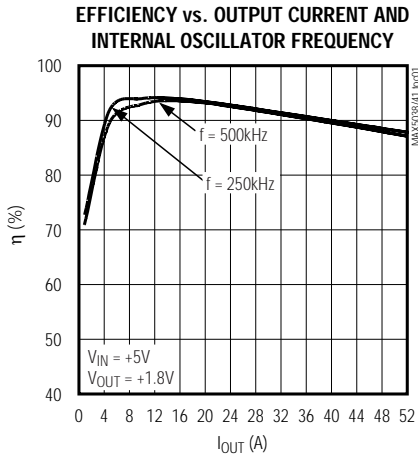
Note 2: Guaranteed by design. Not production tested.

Note 3: See *Peak-Current Comparator* section.

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Typical Operating Characteristics

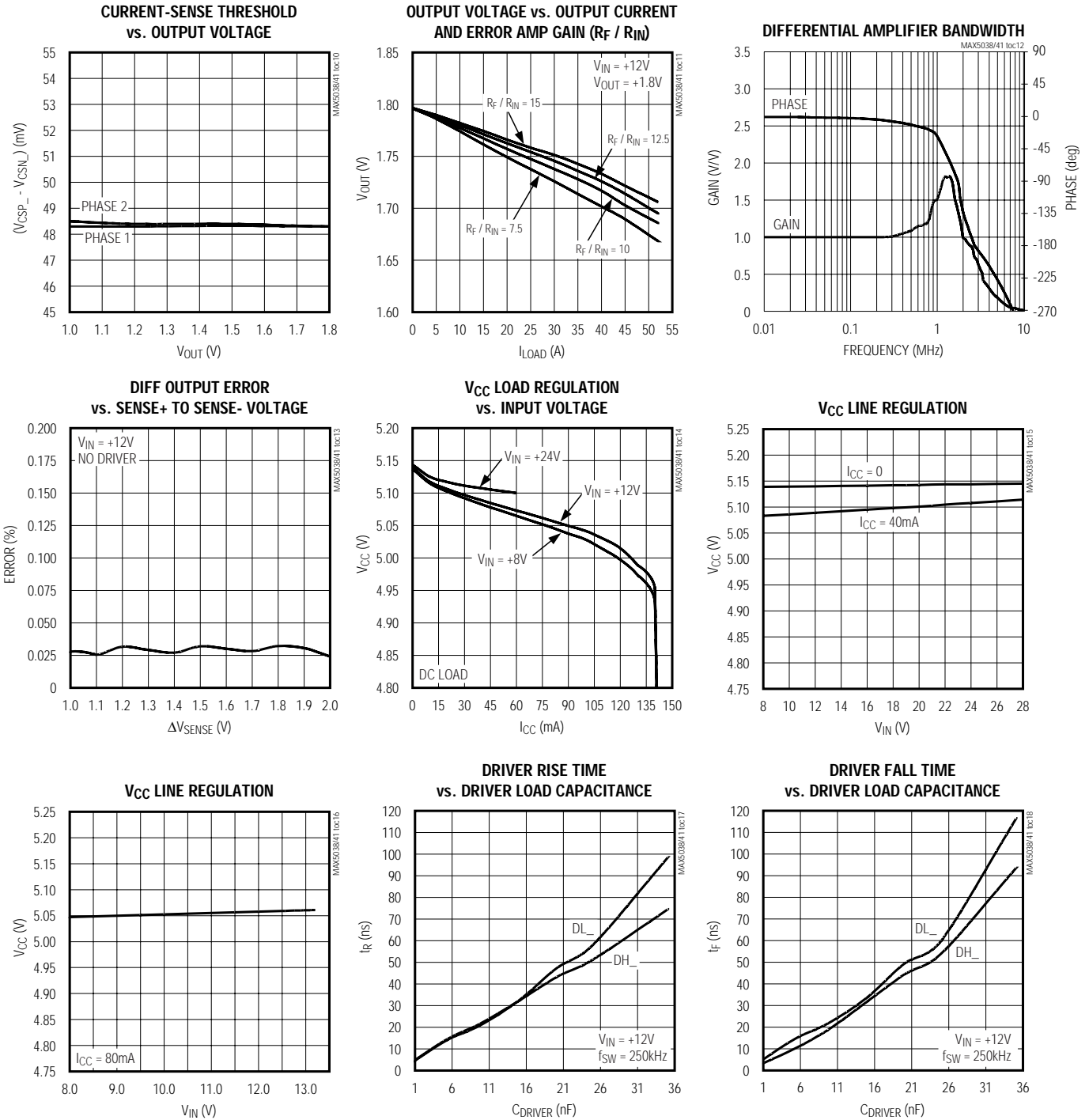
(Circuit of Figure 1. $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Dual-Phase, Parallelable, Average Current-Mode Controllers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



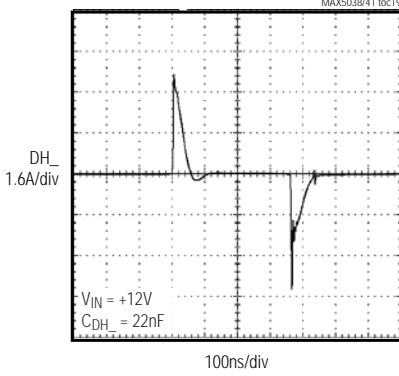
Dual-Phase, Parallelable, Average Current-Mode Controllers

Typical Operating Characteristics (continued)

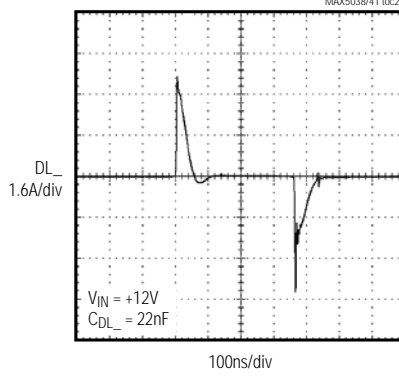
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MAX5038/MAX5041

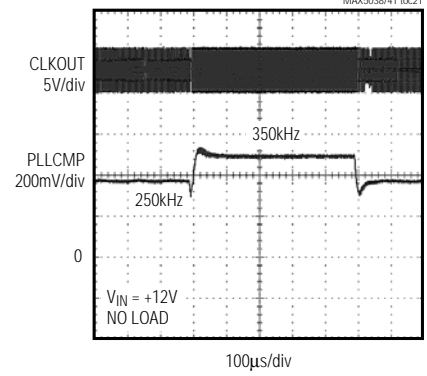
**HIGH-SIDE DRIVER (DH_)
SINK AND SOURCE CURRENT**



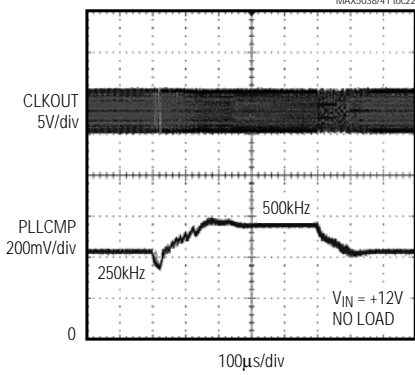
**LOW-SIDE DRIVER (DL_)
SINK AND SOURCE CURRENT**



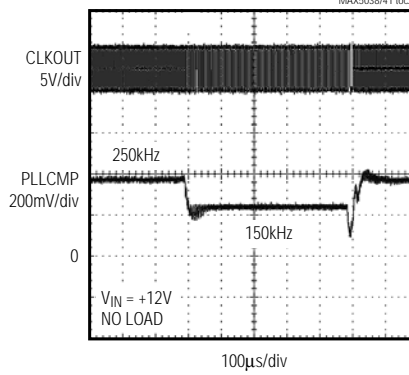
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350kHz TO 250kHz**



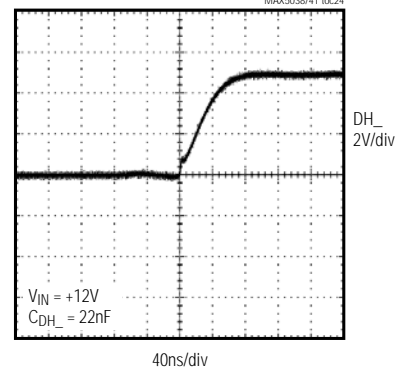
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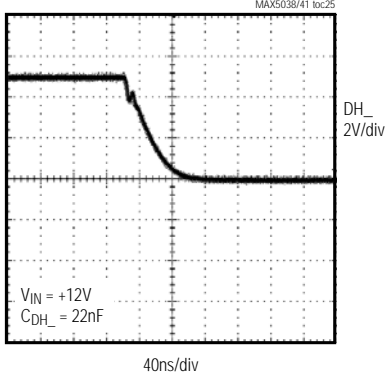
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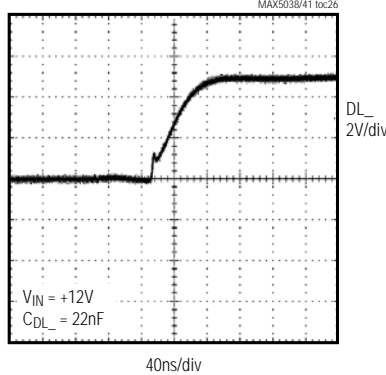
**HIGH-SIDE DRIVER (DH_)
RISE TIME**



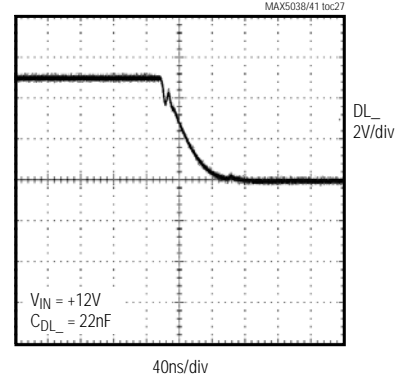
**HIGH-SIDE DRIVER (DH_)
FALL TIME**



**LOW-SIDE DRIVER (DL_)
RISE TIME**



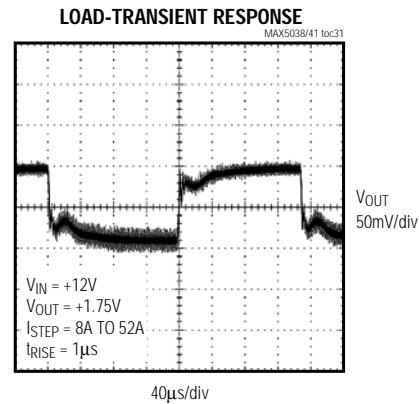
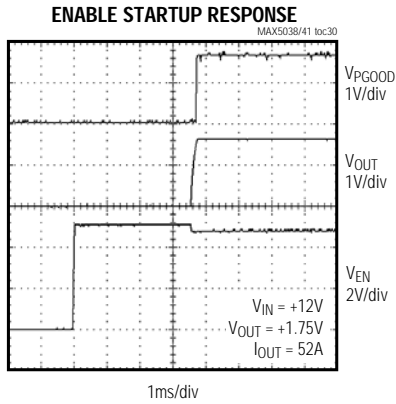
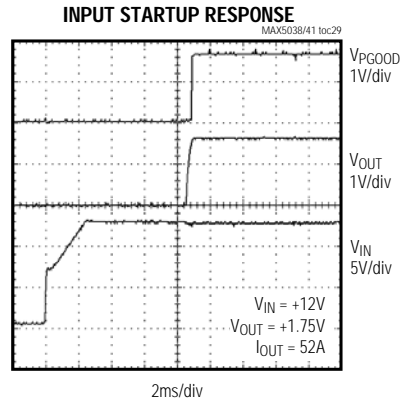
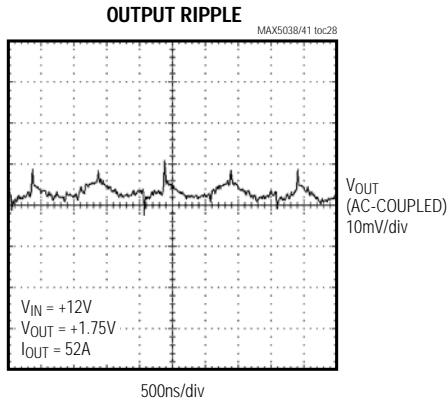
**LOW-SIDE DRIVER (DL_)
FALL TIME**



Dual-Phase, Parallelable, Average Current-Mode Controllers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Dual-Phase, Parallelable, Average Current-Mode Controllers

Pin Description

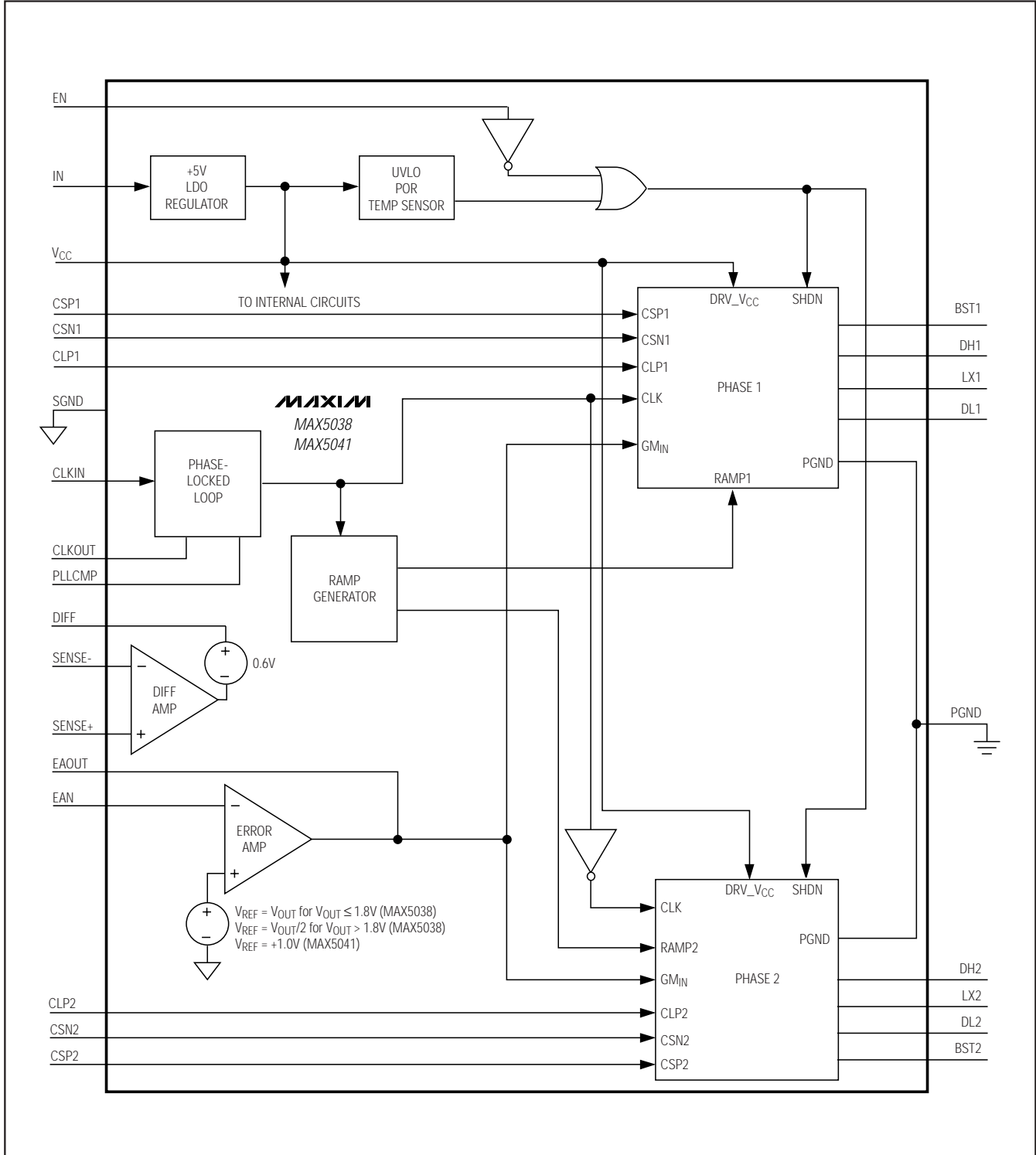
MAX5038/MAX5041

PIN	NAME	FUNCTION
1, 13	CSP2, CSP1	Current-Sense Differential Amplifier Positive Input. Senses the inductor current. The differential voltage between CSP_ and CSN_ is amplified internally by the current-sense amplifier gain of 18.
2, 14	CSN2, CSN1	Current-Sense Differential Amplifier Negative Input. Senses the inductor current.
3	PHASE	Phase-Shift Setting Input. Connect PHASE to V _{CC} for 120°, leave PHASE unconnected for 90°, or connect PHASE to SGND for 60° of phase shift between the rising edges of CLKOUT and CLKIN/DH1.
4	PLLCMP	External Loop-Compensation Input. Connect compensation network for the phase lock loop (see <i>Phase-Locked Loop</i> section).
5, 7	CLP2, CLP1	Current-Error Amplifier Output. Compensate the current loop by connecting an RC network to ground.
6	SGND	Signal Ground. Ground connection for the internal control circuitry.
8	SENSE+	Differential Output Voltage-Sensing Positive Input. Used to sense a remote load. Connect SENSE+ to V _{OUT+} at the load. The MAX5038 regulates the difference between SENSE+ and SENSE- according to the factory preset output voltage. The MAX5041 regulates the SENSE+ to SENSE- difference to +1.0V.
9	SENSE-	Differential Output Voltage-Sensing Negative Input. Used to sense a remote load. Connect SENSE- to V _{OUT-} or PGND at the load.
10	DIFF	Differential Remote-Sense Amplifier Output. DIFF is the output of a precision unity-gain amplifier.
11	EAN	Voltage-Error Amplifier Inverting Input. Receives the output of the differential remote-sense amplifier. Referenced to SGND.
12	EAOUT	Voltage-Error Amplifier Output. Connect to the external gain-setting feedback resistor. The external error amplifier gain-setting resistors determine the amount of adaptive voltage positioning.
15	EN	Output Enable. A logic low shuts down the power drivers. EN has an internal 5μA pullup current.
16, 26	BST1, BST2	Boost Flying-Capacitor Connection. Reservoir capacitor connection for the high-side FET driver supply. Connect 0.47μF ceramic capacitors between BST_ and LX_.
17, 25	DH1, DH2	High-Side Gate Driver Output. Drives the gate of the high-side MOSFET.
18, 24	LX1, LX2	Inductor Connection. Source connection for the high-side MOSFETs. Also serves as the return terminal for the high-side driver.
19, 23	DL1, DL2	Low-Side Gate Driver Output. Synchronous MOSFET gate drivers for the two phases.
20	V _{CC}	Internal +5V Regulator Output. V _{CC} is derived internally from the IN voltage. Bypass to SGND with 4.7μF and 0.1μF ceramic capacitors.
21	IN	Supply Voltage Connection. Connect IN to V _{CC} for a +5V system. Connect the VRM input to IN through an RC lowpass filter, a 2.2Ω resistor and a 0.1μF ceramic capacitor.
22	PGND	Power Ground. Connect PGND, low-side synchronous MOSFET's source, and V _{CC} bypass capacitor returns together.
27	CLKOUT	Oscillator Output. CLKOUT is phase-shifted from CLKIN by the amount specified by PHASE. Use CLKOUT to parallel additional MAX5038/MAX5041s.
28	CLKIN	CMOS Logic Clock Input. Drive the internal oscillator with a frequency range between 125kHz and 600kHz. The PWM frequency defaults to the internal oscillator if CLKIN is connected to V _{CC} or SGND. Connect CLKIN to SGND to set the internal oscillator to 250kHz or connect to V _{CC} to set the internal oscillator to 500kHz. CLKIN has an internal 5μA pulldown current.

Dual-Phase, Parallelable, Average Current-Mode Controllers

Functional Diagram

MAX5038/MAX5041



Dual-Phase, Parallelable, Average Current-Mode Controllers

Detailed Description

The MAX5038/MAX5041 (Figures 1 and 2) average current-mode PWM controllers drive two out-of-phase buck converter channels. Average current-mode control improves current sharing between the channels while minimizing component derating and size. Parallel multiple MAX5038/MAX5041 regulators to increase the

output current capacity. For maximum ripple rejection at the input, set the phase shift between phases to 90° for two paralleled converters, or 60° for three paralleled converters. Paralleling the MAX5038/MAX5041s improves design flexibility in applications requiring upgrades (higher load).

MAX5038/MAX5041

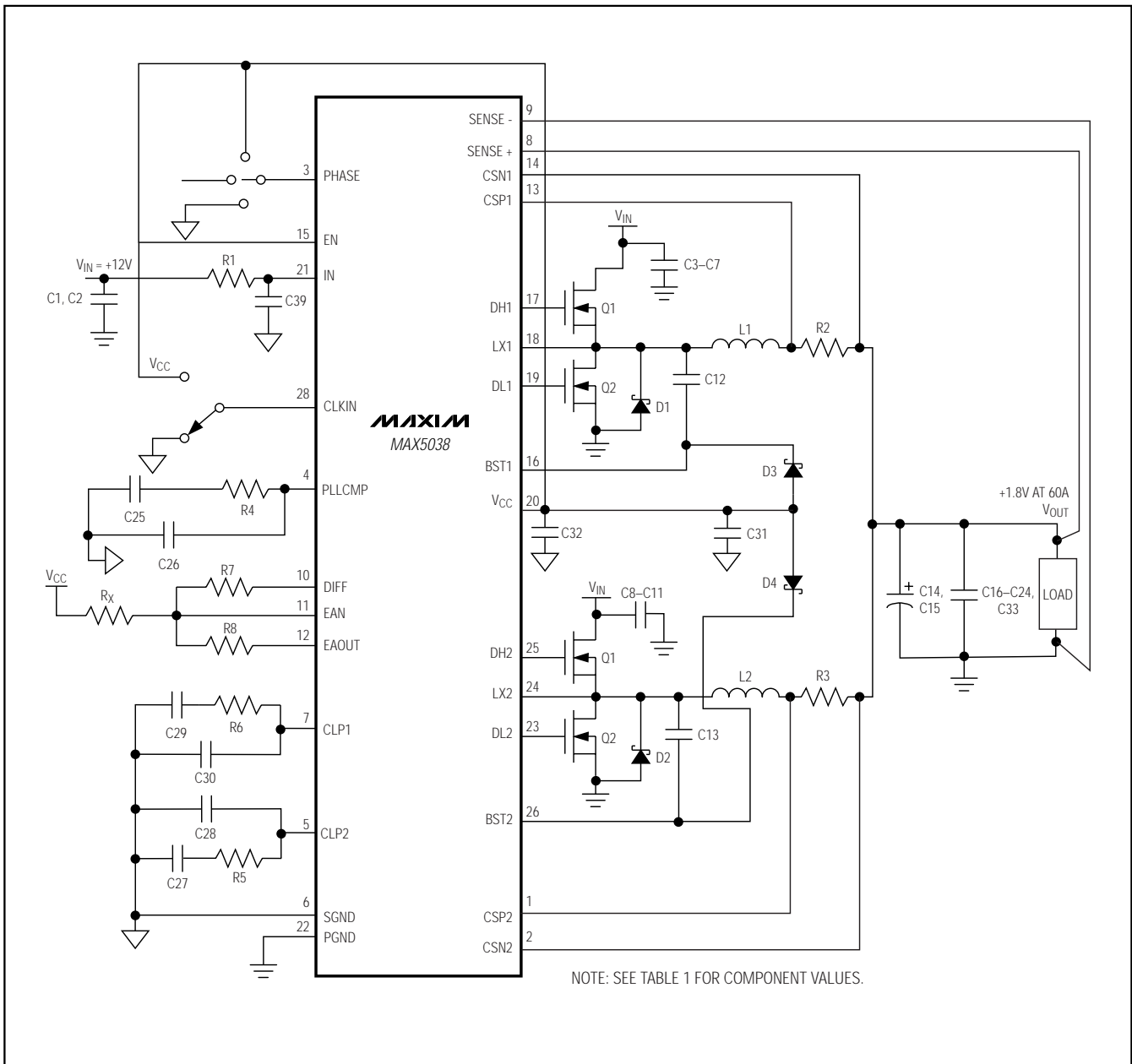


Figure 1. MAX5038 Typical Application Circuit, $V_{IN} = +12V$

Dual-Phase, Parallelable, Average Current-Mode Controllers

Dual-phase converters with an out-of-phase locking arrangement reduce the input and output capacitor ripple current, effectively multiplying the switching frequency by the number of phases. Each phase of the MAX5038/MAX5041 consists of an inner average current loop controlled by a common outer-loop voltage-

error amplifier (VEA) that corrects the output voltage errors. The MAX5038/MAX5041 utilize a single controlling VEA and an average current mode to force the phase currents to be equal.

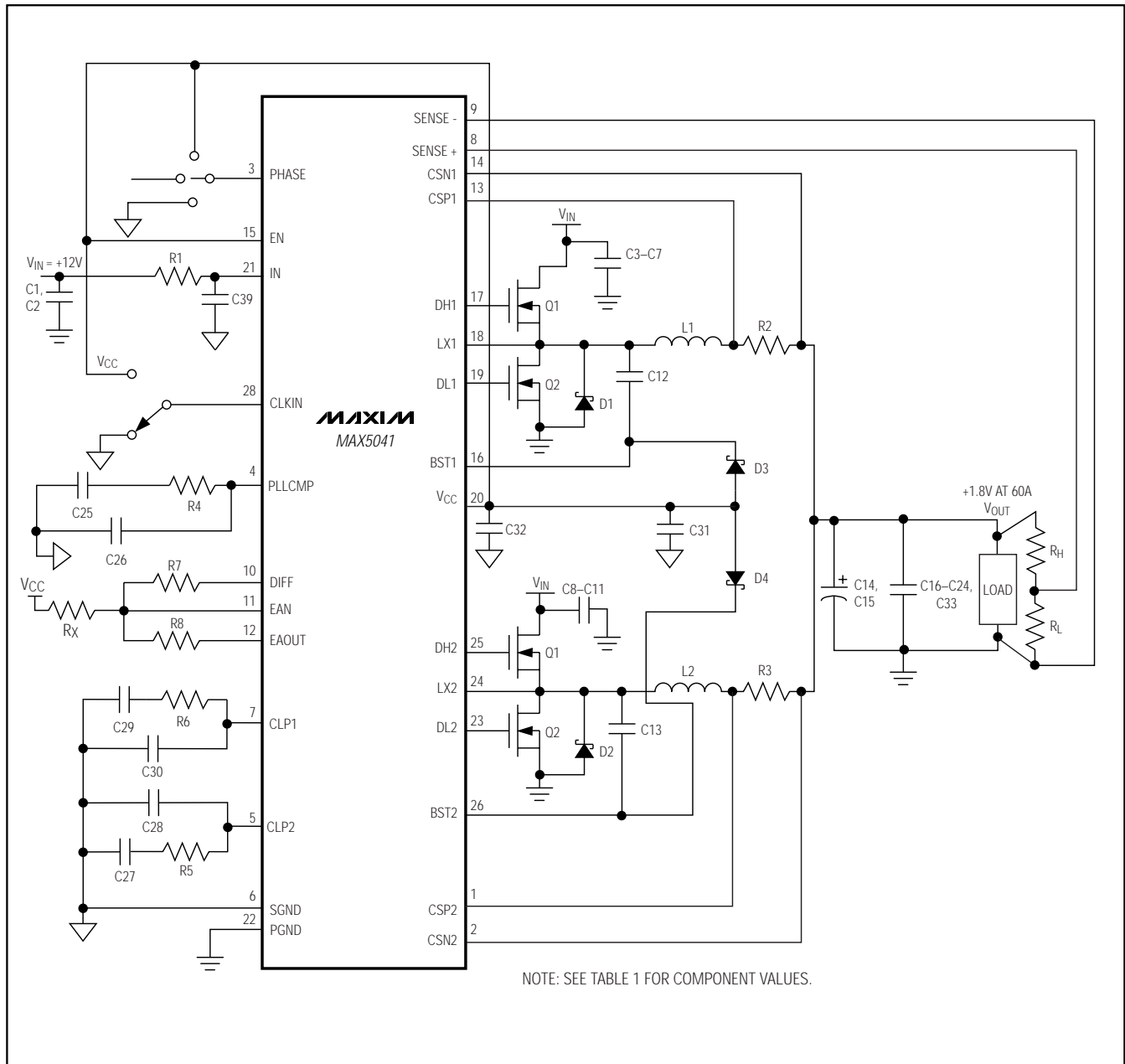


Figure 2. MAX5041 Typical Application Circuit, $V_{IN} = +12V$

Dual-Phase, Parallelable, Average Current-Mode Controllers

V_{IN} and V_{CC}

The MAX5038/MAX5041 accept a wide input voltage range of +4.75V to +5.5V or +8V to +28V. All internal control circuitry operates from an internally regulated nominal voltage of +5V (V_{CC}). For input voltages of +8V or greater, the internal V_{CC} regulator steps the voltage down to +5V. The V_{CC} output voltage regulates to +5V while sourcing up to 80mA. Bypass V_{CC} to SGND with 4.7μF and 0.1μF low-ESR ceramic capacitors for high-frequency noise rejection and stable operation (Figures 1 and 2).

Calculate power dissipation in the MAX5038/MAX5041 as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC} \quad (1)$$

$$I_{CC} = I_Q + f_{SW} \times (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4}) \quad (2)$$

where, Q_{G1}, Q_{G2}, Q_{G3}, and Q_{G4} are the total gate charge of the low-side and high-side external MOSFETs, I_Q is 4mA (typ), and f_{SW} is the switching frequency of each individual phase.

For applications utilizing a +5V input voltage, disable the V_{CC} regulator by connecting IN and V_{CC} together.

Undervoltage Lockout (UVLO)/Power-On Reset (POR)/Soft-Start

The MAX5038/MAX5041 include an undervoltage lockout with hysteresis and a power-on reset circuit for converter turn-on and monotonic rise of the output voltage. The UVLO threshold is internally set between +4.0V and +4.5V with a 200mV hysteresis. Hysteresis at UVLO eliminates “chattering” during startup.

Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches +4V. The MAX5038/MAX5041 draw up to 4mA of current before the input voltage reaches the UVLO threshold.

The compensation network at the current error amplifiers (CLP1 and CLP2) provides an inherent soft-start of the output voltage. It includes a parallel combination of capacitors (C28, C30) and resistors (R5, R6) in series with other capacitors (C27, C29) (see Figures 1 and 2). The voltage at CLP₋ limits the maximum current available to charge output capacitors. The capacitor on CLP₋ in conjunction with the finite output-drive current of the current-error amplifier yields a finite rise time for the output current and thus the output voltage.

Internal Oscillator

The internal oscillator generates the 180° out-of-phase clock signals required by the pulse-width modulation (PWM) circuits. The oscillator also generates the 2V_{p-p} voltage ramp signals necessary for the PWM comparators. Connect CLKIN to SGND to set the internal oscillator frequency to 250kHz or connect CLKIN to V_{CC} to set the internal oscillator to 500kHz.

CLKIN is a CMOS logic clock input for the phase-locked loop (PLL). When driven externally, the internal oscillator locks to the signal at CLKIN. A rising edge at CLKIN starts the ON cycle of the PWM. Ensure that the external clock pulse width is at least 200ns. CLKOUT provides a phase-shifted output with respect to the rising edge of the signal at CLKIN. PHASE sets the amount of phase shift at CLKOUT. Connect PHASE to V_{CC} for 120° of phase shift, leave PHASE unconnected for 90° of phase shift, or connect PHASE to SGND for 60° of phase shift with respect to CLKIN.

The MAX5038/MAX5041 require compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL in order to generate the proper clock signal required for PWM operation.

Control Loop

The MAX5038/MAX5041 use an average current-mode control scheme to regulate the output voltage (Figures 3a and 3b). The main control loop consists of an inner current loop and an outer voltage loop. The inner loop controls the output currents (I_{PHASE1} and I_{PHASE2}) while the outer loop controls the output voltage. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

The current loop consists of a current-sense resistor (R_S), a current-sense amplifier (CA₋), a current-error amplifier (CEA₋), an oscillator providing the carrier ramp, and a PWM comparator (CPWM₋). The precision CA₋ amplifies the sense voltage across R_S by a factor of 18. The inverting input to the CEA₋ senses the CA₋ output. The CEA₋ output is the difference between the voltage-error amplifier output (EAOUT) and the gained-up voltage from the CA₋. The RC compensation network connected to CLP1 and CLP2 provides external frequency compensation for the respective CEA₋. The start of every clock cycle enables the high-side drivers and initiates a PWM ON cycle. Comparator CPWM₋ compares the output voltage from the CEA₋ with a 0 to +2V ramp from the oscillator. The PWM ON cycle terminates when the ramp voltage exceeds the error voltage.

Dual-Phase, Parallelable, Average Current-Mode Controllers

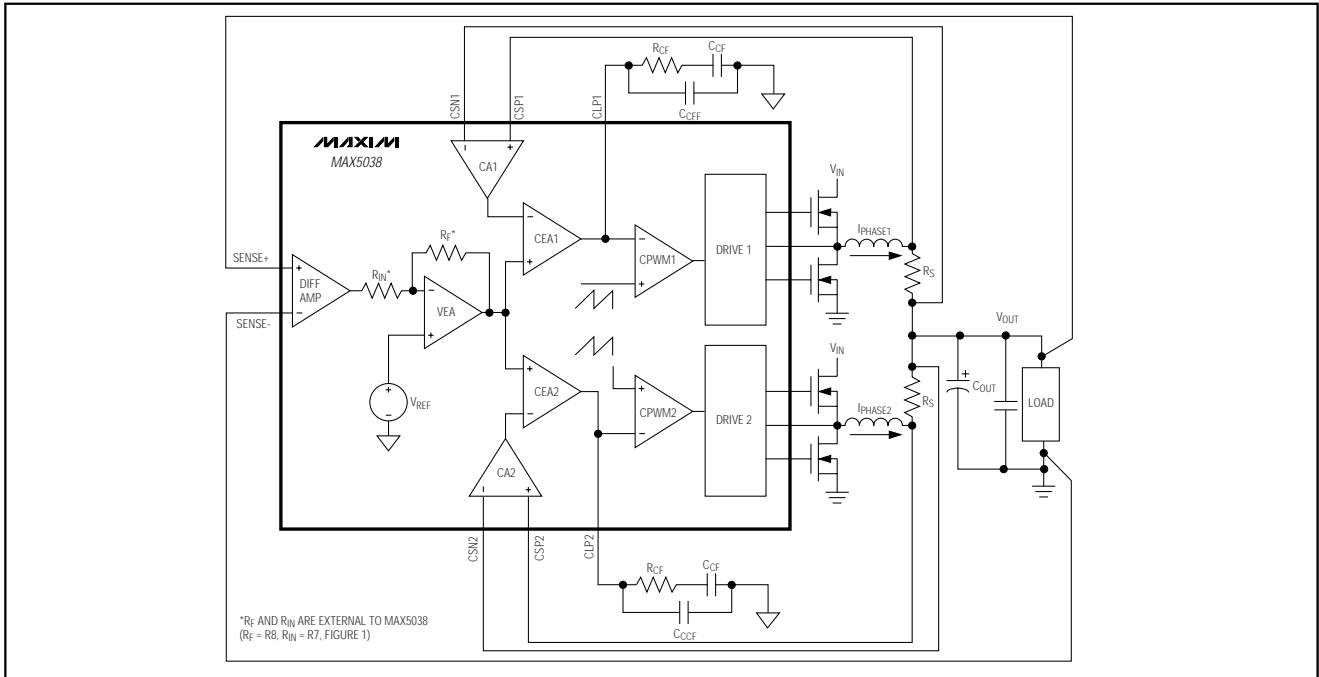


Figure 3a. MAX5038 Control Loop

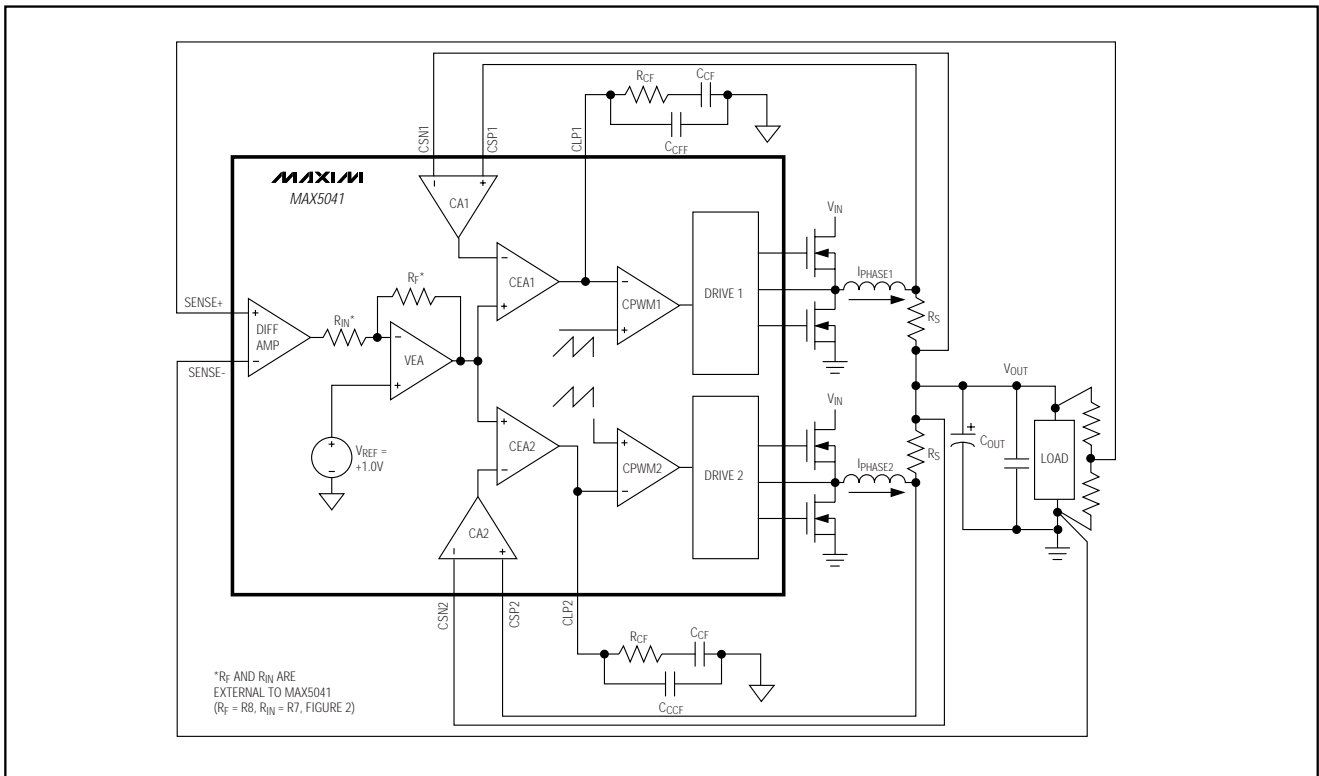


Figure 3b. MAX5041 Control Loop

Dual-Phase, Parallelable, Average Current-Mode Controllers

The outer voltage control loop consists of the differential amplifier (DIFF AMP), reference voltage, and VEA. The unity-gain differential amplifier provides true differential remote sensing of the output voltage. The differential amplifier output connects to the inverting input (EAN) of the VEA. The noninverting input of the VEA is internally connected to an internal precision reference voltage. The MAX5041 reference voltage is set to +1.0V and the MAX5038 reference is set to the preset output voltage. The VEA controls the two inner current loops (Figures 3a and 3b). Use a resistive feedback network to set the VEA gain as required by the adaptive voltage-positioning circuit (see the *Adaptive Voltage Positioning* section).

Current-Sense Amplifier

The differential current-sense amplifier (CA₋) provides a DC gain of 18. The maximum input offset voltage of the current-sense amplifier is 1mV and the common-mode voltage range is -0.3V to +3.6V. The current-sense amplifier senses the voltage across a current-sense resistor.

Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions such as an output inductor malfunction (Figure 4). Note that the average current-limit threshold of 48mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an output inductor with a saturation current specification greater

than the average current limit (48mV). Proper inductor selection ensures that only extreme conditions trip the peak-current comparator, such as a cracked output inductor. The 112mV voltage threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has a delay of only 260ns.

Current-Error Amplifier

Each phase of the MAX5038/MAX5041 has a dedicated transconductance current-error amplifier (CEA₋) with a typical g_m of 550 μ S and 320 μ A output sink and source current capability. The current-error amplifier outputs, CLP1 and CLP2, serve as the inverting input to the PWM comparator. CLP1 and CLP2 are externally accessible to provide frequency compensation for the inner current loops (Figures 3a and 3b). Compensate CEA₋ such that the inductor current down slope, which becomes the up slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM) sets the duty cycle for each cycle by comparing the output of the current-error amplifier to a 2V_{p-p} ramp. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH₋) turns on. The comparator sets the flip-flop as soon as the ramp voltage exceeds the CLP₋ voltage, thus terminating the ON cycle (Figure 4).

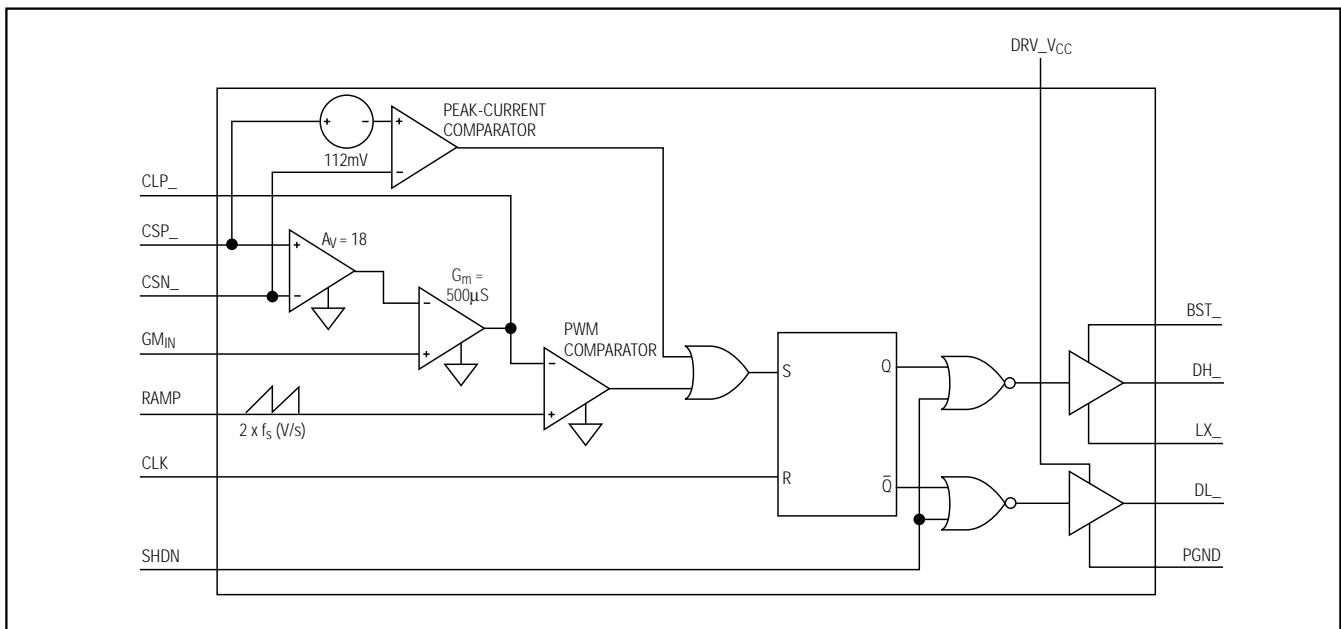


Figure 4. Phase Circuit (Phase 1/Phase 2)

Dual-Phase, Parallelable, Average Current-Mode Controllers

Differential Amplifier

The differential amplifier (DIFF AMP) facilitates output voltage remote sensing at the load (Figures 3a and 3b). It provides true differential output voltage sensing while rejecting the common-mode voltage errors due to high-current ground paths. Sensing the output voltage directly at the load provides accurate load voltage sensing in high-current environments. The VEA provides the difference between the differential amplifier output (DIFF) and the desired output voltage. The differential amplifier has a bandwidth of 3MHz. The difference between SENSE+ and SENSE- regulates to the preset output voltage for the MAX5038 and regulates to +1V for the MAX5041.

Voltage-Error Amplifier

The VEA sets the gain of the voltage control loop and determines the error between the differential amplifier output and the internal reference voltage (V_{REF}).

V_{REF} equals $V_{OUT(NOM)}$ for the +1.8V or lower voltage versions of the MAX5038 and V_{REF} equals $V_{OUT(NOM)}/2$ for the +2.5V and +3.3V versions. For MAX5041, V_{REF} equals +1V.

An offset is added to the output voltage of the MAX5038/MAX5041 with a finite gain (R_F/R_{IN}) of the VEA such that the no-load output voltage is higher than the nominal value. Choose R_F and R_{IN} from the *Adaptive Voltage Positioning* section and use the following equations to calculate the no-load output voltage.

MAX5038:

$$V_{OUT(NL)} = \left(1 + \frac{R_{IN}}{R_F}\right) \times V_{OUT(NOM)} \quad (3)$$

MAX5041:

$$V_{OUT(NL)} = \left(1 + \frac{R_{IN}}{R_F}\right) \times \left(\frac{R_H + R_L}{R_L}\right) \times V_{REF} \quad (4)$$

where R_H and R_L are the feedback resistor network (Figure 2).

Some applications require V_{OUT} equal to $V_{OUT(NOM)}$ at no load. To ensure that the output voltage does not exceed the nominal output voltage ($V_{OUT(NOM)}$), add a resistor R_X from V_{CC} to EAN.

Use the following equations to calculate the value of R_X .

For MAX5038 versions of $V_{OUT(NOM)} \leq +1.8V$:

$$R_X = [V_{CC} - (V_{NOM} + 0.6)] \times \frac{R_F}{V_{NOM}} \quad (5)$$

For MAX5038 versions of $V_{OUT(NOM)} > +1.8V$:

$$R_X = [2V_{CC} - (V_{NOM} + 1.2)] \times \frac{R_F}{V_{NOM}} \quad (6)$$

For MAX5041:

$$R_X = [V_{CC} - 1.6] \times \frac{R_F}{V_{REF}} \quad (7)$$

The VEA output clamps to +0.9V (plus the common-mode voltage of +0.6V), thus limiting the average maximum current from individual phases. The maximum average current-limit threshold for each phase is equal to the maximum clamp voltage of the VEA divided by the gain (18) of the current-sense amplifier. This allows for accurate settings for the average maximum current for each phase. Set the VEA gain using R_F and R_{IN} for the amount of output voltage positioning required as discussed in the *Adaptive Voltage Positioning* section (Figures 3a and 3b).

Adaptive Voltage Positioning

Powering new-generation processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher than the output voltage during nominally loaded conditions allows a larger downward voltage excursion when the output current suddenly increases. Regulating at a lower output voltage under a heavy load allows a larger upward-voltage excursion when the output current suddenly decreases. A larger allowed, voltage-step excursion reduces the required number of output capacitors or allows for the use of higher ESR capacitors.

Voltage positioning and the ability to operate with multiple reference voltages may require the output to regulate away from a center value. Define the center value as the voltage where the output drops ($\Delta V_{OUT}/2$) at one half the maximum output current (Figure 5).

Dual-Phase, Parallelable, Average Current-Mode Controllers

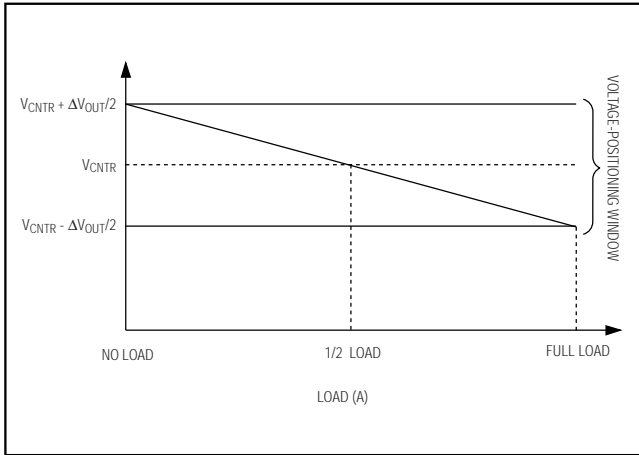


Figure 5. Defining the Voltage-Positioning Window

Set the voltage-positioning window (ΔV_{OUT}) using the resistive feedback of the VEA. Use the following equations to calculate the voltage-positioning window for the MAX5038:

$$\Delta V_{OUT} = \frac{I_{OUT} \times R_{IN}}{2 \times G_C \times R_F} \quad (8)$$

$$G_C = \frac{0.05}{R_S} \quad (9)$$

Use the following equation to calculate the voltage-positioning window for the MAX5041:

$$\Delta V_{OUT} = \frac{I_{OUT} \times R_{IN}}{(2 \times G_C \times R_F)} \times \frac{R_H + R_L}{R_L} \quad (10)$$

$$G_C = \frac{0.05}{R_S} \quad (11)$$

where R_{IN} and R_F are the input and feedback resistors of the VEA, G_C is the current-loop gain and R_S is the current-sense resistor or, if using lossless inductor current sensing, the DC resistance of the inductor.

Phase-Locked Loop: Operation and Compensation

The PLL synchronizes the internal oscillator to the external frequency source when driving CLKIN. Connecting CLKIN to VCC or SGND forces the PWM frequency to default to the internal oscillator frequency of 500kHz or 250kHz, respectively. The PLL uses a conventional architecture consisting of a phase detector and a charge pump capable of providing 20 μ A of output current. Connect an external series combination capacitor (C25) and resistor (R4) and a parallel capacitor (C26) from PLLCMP to SGND to provide frequency compensation for the PLL (Figure 1). The pole-zero pair compensation provides a zero at $f_z = 1 / [R4 \times (C25 + C26)]$ and a pole at $f_p = 1 / (R4 \times C26)$. Use the following typical values for compensating the PLL: $R4 = 7.5k\Omega$, $C25 = 4.7nF$, $C26 = 470pF$. If changing the PLL frequency, expect a finite locking time of approximately 200 μ s.

The MAX5038/MAX5041 require compensation on PLLCMP even when operating from the internal oscillator. The device requires an active PLL in order to generate the proper internal PWM clocks.

MOSFET Gate Drivers (DH₋, DL₋)

The high-side (DH₋) and low-side (DL₋) drivers drive the gates of external N-channel MOSFETs (Figures 1 and 2). The drivers' high-peak sink and source current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. For modern CPU voltage-regulating module applications where the duty cycle is less than 50%, choose high-side MOSFETs (Q1 and Q3) with a moderate $R_{DS(ON)}$ and a very low gate charge. Choose low-side MOSFETs (Q2 and Q4) with very low $R_{DS(ON)}$ and moderate gate charge.

The driver block also includes a logic circuit that provides an adaptive non-overlap time to prevent shoot-through currents during transition. The typical non-overlap time is 60ns between the high-side and low-side MOSFETs.

BST₋

VDD powers the low- and high-side MOSFET drivers. Connect a 0.47 μ F low-ESR ceramic capacitor between BST₋ and LX₋. Bypass VCC to PGND with 4.7 μ F and 0.1 μ F low-ESR ceramic capacitors. Reduce the PC board area formed by these capacitors, the rectifier diodes between VCC and the boost capacitor, the MAX5038/MAX5041, and the switching MOSFETs.

Dual-Phase, Parallelable, Average Current-Mode Controllers

Overload Conditions

Average current-mode control has the ability to limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to +0.9V with respect to the common-mode voltage ($V_{CM} = +0.6V$) and is compared with the output of the current-sense amplifiers (CA1 and CA2) (see Figures 3a and 3b). The current-sense amplifier's gain of 18 limits the maximum current in the inductor or sense resistor to $I_{LIMIT} = 50mV/R_S$.

Parallel Operation

For applications requiring large output current, parallel up to three MAX5038/MAX5041s (six phases) to triple the available output current. The paralleled converters operate at the same switching frequency but different phases keep the capacitor ripple RMS currents to a minimum. Three parallel MAX5038/MAX5041 converters deliver up to 180A of output current. To set the phase shift of the on-board PLL, leave PHASE unconnected for 90° of phase shift (2 paralleled converters), or connect PHASE to SGND for 60° of phase shift (3 converters in parallel). Designate one converter as master and the remaining converters as slaves. Connect the master and slave controllers in a daisy-chain configuration as shown in Figure 6. Connect CLKOUT from the master controller to CLKIN of the first slaved controller, and CLKOUT from the first slaved controller to CLKIN of the second slaved controller. Choose the appropriate phase shift for minimum ripple currents at the input and output capacitors. The master controller senses the output differential voltage through SENSE+ and SENSE- and generates the DIFF voltage. Disable the voltage sensing of the slaved controllers by leaving DIFF unconnected (floating). Figure 7 shows a detailed typical parallel application circuit using two MAX5038s. This circuit provides four phases at an input voltage of +12V and an output voltage range of +1V to +3.3V at 104A.

Applications Information

Each MAX5038/MAX5041 circuit drives two 180° out-of-phase channels. Parallel two or three MAX5038/MAX5041 circuits to achieve four- or six-phase operation, respectively. Figure 1 shows the typical application circuit for a two-phase operation. The design criteria for a two-phase converter includes frequency selection, inductor value, input/output capacitance, switching MOSFETs, sense resistors, and the compensation network. Follow the same procedure for the four- and six-phase converter design, except for the input and output capacitance. The input and output capacitance requirements vary depending on the operating duty cycle.

The examples discussed in this data sheet pertain to a typical application with the following specifications:

$$V_{IN} = +12V$$

$$V_{OUT} = +1.8V$$

$$I_{OUT(MAX)} = 52A$$

$$f_{SW} = 250kHz$$

$$\text{Peak-to-Peak Inductor Current } (\Delta I_L) = 10A$$

Table 1 shows a list of recommended external components (Figure 1) and Table 2 provides component supplier information.

Number of Phases

Selecting the number of phases for a voltage regulator depends mainly on the ratio of input-to-output voltage (operating duty cycle). Optimum output-ripple cancellation depends on the right combination of operating duty cycle and the number of phases. Use the following equation as a starting point to choose the number of phases:

$$N_{PH} \approx K/D \quad (12)$$

where $K = 1, 2, \text{ or } 3$ and the duty cycle is $D = V_{OUT}/V_{IN}$.

Choose K to make N_{PH} an integer number. For example, converting $V_{IN} = +12V$ to $V_{OUT} = +1.8V$ yields better ripple cancellation in the six-phase converter than in the four-phase converter. Ensure that the output load justifies the greater number of components for multiphase conversion. Generally limiting the maximum output current to 25A per phase yields the most cost-effective solution. The maximum ripple cancellation occurs when $N_{PH} = K/D$.

Single-phase conversion requires greater size and power dissipation for external components such as the switching MOSFETs and the inductor. Multiphase conversion eliminates the heatsink by distributing the power dissipation in the external components. The multiple phases operating at given phase shifts effectively increase the switching frequency seen by the input/output capacitors, thereby reducing the input/output capacitance requirement for the same ripple performance. The lower inductance value improves the large-signal response of the converter during a transient load at the output. Consider all these issues when determining the number of phases necessary for the voltage regulator application.

Inductor Selection

The switching frequency per phase, peak-to-peak ripple current in each phase, and allowable ripple at the output determine the inductance value.

Dual-Phase, Parallelable, Average Current-Mode Controllers

MAX5038/MAX5041

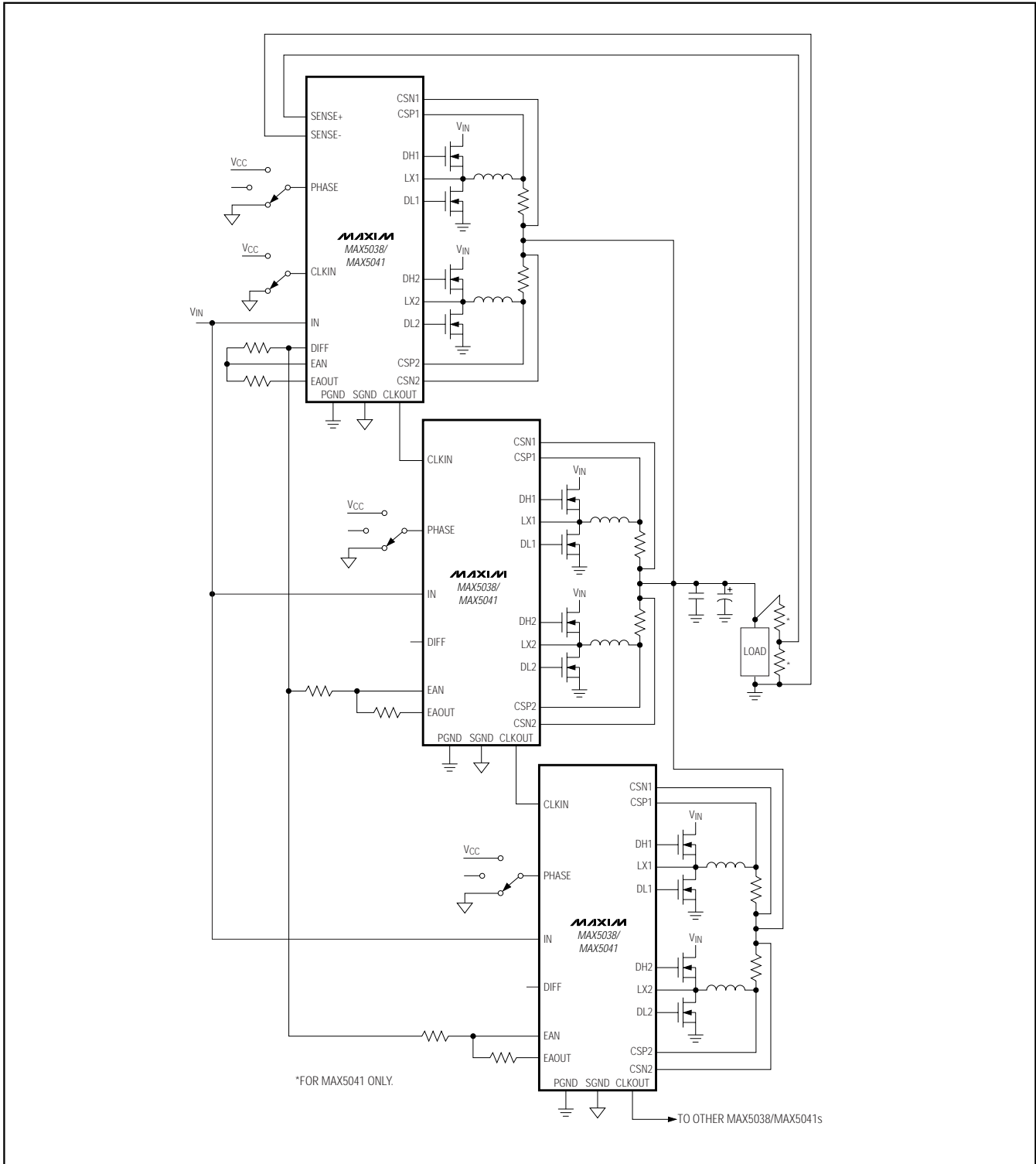


Figure 6. Parallel Configuration of Multiple MAX5038/MAX5041s

Dual-Phase, Parallelable, Average Current-Mode Controllers

MAX5038/MAX5041

Table 1. Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2	2	47 μ F, 16V X5R input-filter capacitors TDK C5750X5R1C476M
C3–C11	9	22 μ F, 16V input-filter capacitors TDK C4532X5R1C226M
C12, C13	2	0.47 μ F, 16V capacitors TDK C1608X5R1A474K
C14, C15	2	100 μ F, 6.3V, output-filter capacitors Murata GRM44-1X5R107K6.3
C16–C24, C33	10	270 μ F, 2V output-filter capacitors Panasonic EEFUE0D271R
C25	1	4700pF, 16V X7R capacitor Vishay-Siliconix VJ0603Y471JXJ
C26, C28, C30	3	470pF 16V capacitors Murata GRM1885C1H471JAB01
C27, C29	2	0.01 μ F 50V X7R capacitors Murata GRM188R71H103KA01
C31	1	4.7 μ F 16V X5R capacitor Murata GRM40-034X5R475k6.3
C32	3	0.1 μ F 16V X7R capacitors Murata GRM188R71C104KA01
D1, D2	2	Schottky diodes ON-Semiconductor MBRS340T3
D3, D4	2	Schottky diodes ON-Semiconductor MBR0520LT1
L1, L2	2	0.6 μ H, 27A inductors Panasonic ETOP1H0R6BFX
Q1, Q3	2	Upper-power MOSFETs Vishay-Siliconix Si7860DP
Q2, Q4	2	Lower-power MOSFETs Vishay-Siliconix Si7886DP
R1	1	2.2 Ω \pm 1% resistor
R2, R3	4	Current-sense resistors, use two 2.7m Ω resistors in parallel, Panasonic ERJM1WSF2M7U
R4	1	7.5k Ω \pm 1% resistor
R5, R6	2	1k Ω \pm 1% resistors
R7	1	4.99k Ω \pm 1% resistor
R8, R9	2	37.4k Ω \pm 1% resistors

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Murata	770-436-1300	770-436-3030	www.murata.com
ON Semiconductor	602-244-6600	602-244-3345	www.on-semi.com
Panasonic	714-373-7939	714-373-7183	www.panasonic.com
TDK	847-803-6100	847-390-4405	www.tcs.tdk.com
Vishay-Siliconix	1-800-551-6933	619-474-8920	www.vishay.com

Dual-Phase, Parallelable, Average Current-Mode Controllers

Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency. The charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs create switching losses. The situation worsens at higher input voltages, since switching losses are proportional to the square of input voltage. Use 500kHz per phase for $V_{IN} = +5V$ and 250kHz or less per phase for $V_{IN} \geq +12V$.

Although lower switching frequencies per phase increase the peak-to-peak inductor ripple current (ΔI_L), the ripple cancellation in the multiphase topology reduces the input and output capacitor RMS ripple current.

Use the following equation to determine the minimum inductance value:

$$L_{MIN} = \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I_L} \quad (13)$$

Choose ΔI_L equal to about 40% of the output current per phase. Since ΔI_L affects the output-ripple voltage, the inductance value may need minor adjustment after choosing the output capacitors for full-rated efficiency.

Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High ΔI_L causes large peak-to-peak flux excursion increasing the core losses at higher frequencies. The high-frequency operation coupled with high ΔI_L , reduces the required minimum inductance and even makes the use of planar inductors possible. The advantages of using planar magnetics include low-profile design, excellent current-sharing between phases due to the tight control of parasitics, and low cost.

For example, calculate the minimum inductance at $V_{IN(MAX)} = +13.2V$, $V_{OUT} = +1.8V$, $\Delta I_L = 10A$, and $f_{SW} = 250kHz$:

$$L_{MIN} = \frac{(13.2 - 1.8) \times 1.8}{13.2 \times 250k \times 10} = 0.6\mu H \quad (14)$$

The average current-mode control feature of the MAX5038/MAX5041 limits the maximum peak inductor current which prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current.

Use the following equation to determine the worst-case inductor current for each phase:

$$I_{L_PEAK} = \frac{0.051}{R_{SENSE}} + \frac{\Delta I_L}{2} \quad (15)$$

where R_{SENSE} is the sense resistor in each phase.

Switching MOSFETs

when choosing a MOSFET for voltage regulators, consider the total gate charge, $R_{DS(ON)}$, power dissipation, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications.

The average gate-drive current from the MAX5038/MAX5041 output is proportional to the total capacitance it drives from DH1, DH2, DL1, and DL2. The power dissipated in the MAX5038/MAX5041 is proportional to the input voltage and the average drive current. See the V_{IN} and V_{CC} section to determine the maximum total gate charge allowed from all the driver outputs together.

The gate charge and drain capacitance (CV^2) loss, the cross-conduction loss in the upper MOSFET due to finite rise/fall time, and the I^2R loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET. Estimate the power loss (PD_{MOS_HI}) in the high-side and low-side MOSFETs using following equations:

$$PD_{MOS-HI} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4} \right) + 1.4 R_{DS(ON)} \times I_{RMS-HI}^2 \quad (16)$$

where Q_G , $R_{DS(ON)}$, t_R , and t_F are the upper-switching MOSFET's total gate charge, on-resistance at $+25^\circ C$, rise time, and fall time, respectively.

$$I_{RMS-HI} = \sqrt{(I_{DC}^2 + I_{PK}^2 + I_{DC} \times I_{PK}) \times \frac{D}{3}} \quad (17)$$

where $D = V_{OUT}/V_{IN}$, $I_{DC} = (I_{OUT} - \Delta I_L)/2$ and $I_{PK} = (I_{OUT} + \Delta I_L)/2$

Dual-Phase, Parallelable, Average Current-Mode Controllers

$$PD_{MOS-LO} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{2 \times C_{OSS} \times V_{IN}^2 \times f_{SW}}{3} \right) + 1.4 R_{DS(ON)} \times I_{RMS-LO}^2 \quad (18)$$

$$I_{RMS-LO} = \sqrt{\left(I_{DC}^2 + I_{PK}^2 + I_{DC} \times I_{PK} \right) \times \frac{(1-D)}{3}} \quad (19)$$

For example, from the typical specifications in the *Applications Information* section with $V_{OUT} = +1.8V$, the high-side and low-side MOSFET RMS currents are 9.9A and 24.1A, respectively. Ensure that the thermal impedance of the MOSFET package keeps the junction temperature at least 25°C below the absolute maximum rating. Use the following equation to calculate maximum junction temperature:

$$T_J = PD_{MOS} \times \theta_{J-A} + T_A \quad (20)$$

Table 3. Peak-to-Peak Output Ripple Current Calculations

NUMBER OF PHASES (N)	DUTY CYCLE (D)	EQUATION FOR ΔI_{P-P}
2	< 50%	$\Delta I = \frac{V_O(1-2D)}{L \times f_{SW}}$
2	> 50%	$\Delta I = \frac{(V_{IN} - V_O)(2D-1)}{L \times f_{SW}}$
4	0 to 25%	$\Delta I = \frac{V_O(1-4D)}{L \times f_{SW}}$
4	25% to 50%	$\Delta I = \frac{V_O(1-2D)(4D-1)}{2 \times D \times L \times f_{SW}}$
4	> 50%	$\Delta I = \frac{V_O(2D-1)(3-4D)}{D \times L \times f_{SW}}$
6	< 17%	$\Delta I = \frac{V_O(1-6D)}{L \times f_{SW}}$

Input Capacitors

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. Increasing the number of phases increases the effective switching frequency and lowers the peak-to-average current ratio, yielding lower input capacitance requirement.

The input ripple is comprised of ΔV_O (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contributions from the ESR and capacitor discharge are equal to 30% and 70%, respectively. Calculate the input capacitance and ESR required for a specified ripple using the following equation:

$$ESR_{IN} = \frac{(\Delta V_{ESR})}{\left(\frac{I_{OUT}}{N} + \frac{\Delta I_L}{2} \right)} \quad (21)$$

$$C_{IN} = \frac{\frac{I_{OUT}}{N} \times D(1-D)}{\Delta V_O \times f_{SW}} \quad (22)$$

where I_{OUT} is the total output current of the multiphase converter and N is the number of phases.

For example, at $V_{OUT} = +1.8V$, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 1mΩ and 200μF.

Output Capacitors

The worst-case peak-to-peak and capacitor RMS ripple current, the allowable peak-to-peak output ripple voltage, and the maximum deviation of the output voltage during step loads determine the capacitance and the ESR requirements for the output capacitors.

In multiphase converter design, the ripple currents from the individual phases cancel each other and lower the ripple current. The degree of ripple cancellation depends on the operating duty cycle and the number of phases. Choose the right equation from Table 3 to calculate the peak-to-peak output ripple for a given duty cycle of two-, four-, and six-phase converters. The maximum ripple cancellation occurs when $N_{PH} = K / D$.

Dual-Phase, Parallelable, Average Current-Mode Controllers

The allowable deviation of the output voltage during the fast transient load dictates the output capacitance and ESR. The output capacitors supply the load step until the controller responds with a greater duty cycle. The response time (t_{RESPONSE}) depends on the closed-loop bandwidth of the converter. The resistive drop across the capacitor ESR and capacitor discharge causes a voltage drop during a step load. Use a combination of SP polymer and ceramic capacitors for better transient load and ripple/noise performance.

Keep the maximum output voltage deviation less than or equal to the adaptive voltage-positioning window (ΔV_{OUT}). Assume 50% contribution each from the output capacitance discharge and the ESR drop. Use the following equations to calculate the required ESR and capacitance value:

$$\text{ESR}_{\text{OUT}} = \frac{\Delta V_{\text{ESR}}}{I_{\text{STEP}}} \quad (23)$$

$$C_{\text{OUT}} = \frac{I_{\text{STEP}} \times t_{\text{RESPONSE}}}{\Delta V_{\text{O}}} \quad (24)$$

where I_{STEP} is the load step and t_{RESPONSE} is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Current Limit

The average current-mode control technique of the MAX5038/MAX5041 accurately limits the maximum output current per phase. The MAX5038/MAX5041 sense the voltage across the sense resistor and limit the peak inductor current ($I_{\text{L-PK}}$) accordingly. The ON cycle terminates when the current-sense voltage reaches 45mV (min). Use the following equation to calculate maximum current-sense resistor value:

$$R_{\text{SENSE}} = \frac{0.045}{\frac{I_{\text{OUT}}}{N}} \quad (25)$$

$$\text{PDR} = \frac{2.5 \times 10^{-3}}{R_{\text{SENSE}}} \quad (26)$$

where PDR is the power dissipation in sense resistors. Select 5% lower value of R_{SENSE} to compensate for any parasitics associated with the PC board. Also, select a non-inductive resistor with the appropriate wattage rating.

Compensation

The main control loop consists of an inner current loop and an outer voltage loop. The MAX5038/MAX5041 use an average current-mode control scheme to regulate the output voltage (Figures 3a and 3b). I_{PHASE1} and I_{PHASE2} are the inner average current loops. The VEA output provides the controlling voltage for these current sources. The inner current loop absorbs the inductor pole reducing the order of the outer voltage loop to that of a single-pole system.

A resistive feedback around the VEA provides the best possible response, since there are no capacitors to charge and discharge during large-signal excursions, R_{F} and R_{IN} determine the VEA gain. Use the following equation to calculate the value for R_{F} :

$$R_{\text{F}} = \frac{I_{\text{OUT}} \times R_{\text{IN}}}{N \times G_{\text{C}} \times \Delta V_{\text{OUT}}} \quad (27)$$

$$G_{\text{C}} = \frac{0.05}{R_{\text{S}}} \quad (28)$$

where G_{C} is the current-loop gain and N is number of phases.

When designing the current-control loop ensure that the inductor downslope (when it becomes an upslope at the CEA output) does not exceed the ramp slope. This is a necessary condition to avoid sub-harmonic oscillations similar to those in peak current-mode control with insufficient slope compensation. Use the following equation to calculate the resistor R_{CF} :

$$R_{\text{CF}} \leq \frac{2 \times f_{\text{SW}} \times L \times 10^2}{V_{\text{OUT}} \times R_{\text{SENSE}}} \quad (29)$$

For example, the maximum R_{CF} is 12k Ω for $R_{\text{SENSE}} = 1.35\text{m}\Omega$.

C_{CF} provides a low-frequency pole while R_{CF} provides a midband zero. Place a zero at f_{Z} to obtain a phase bump at the crossover frequency. Place a high-frequency pole (f_{P}) at least a decade away from the crossover frequency to achieve maximum phase margin.

Dual-Phase, Parallelable, Average Current-Mode Controllers

Use the following equations to calculate C_{CF} and C_{CFF} :

$$C_{CF} = \frac{1}{2 \times \pi \times f_z \times R_{CF}} \quad (30)$$

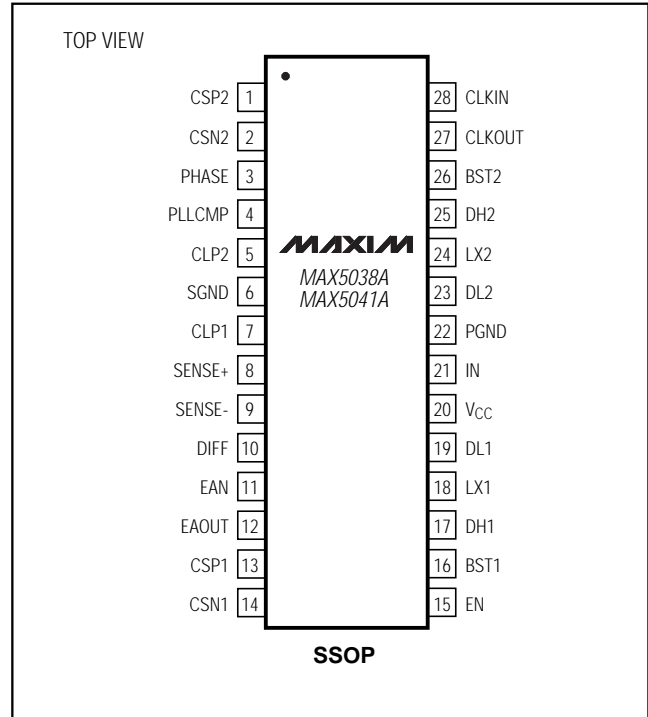
$$C_{CFF} = \frac{1}{2 \times \pi \times f_p \times R_{CF}} \quad (31)$$

PC Board Layout

Use the following guidelines to layout the switching voltage regulator.

- 1) Place the V_{IN} and V_{CC} bypass capacitors close to the MAX5038/MAX5041.
- 2) Minimize the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
- 3) Keep short the current loop from the lower switching MOSFET, inductor, and output capacitor and return to the source of the lower MOSFET.
- 4) Place the Schottky diodes close to the lower MOSFETs and on the same side of the PC board.
- 5) Keep the SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
- 6) Run the current-sense lines CS+ and CS- very close to each other to minimize the loop area. Similarly, run the remote voltage sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of current-sense resistors.
- 7) Avoid long traces between the V_{CC} bypass capacitors, driver output of the MAX5038/MAX5041, MOSFET gates and PGND pin. Minimize the loop formed by the V_{CC} bypass capacitors, bootstrap diode, bootstrap capacitor, MAX5038/MAX5041, and upper MOSFET gate.
- 8) Place the bank of output capacitors close to the load.

Pin Configuration



- 9) Distribute the power components evenly across the board for proper heat dissipation.
- 10) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
- 11) Use at least 4oz copper to keep the trace inductance and resistance to a minimum. Thin copper PC boards can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Chip Information

TRANSISTOR COUNT: 5431

PROCESS: BiCMOS

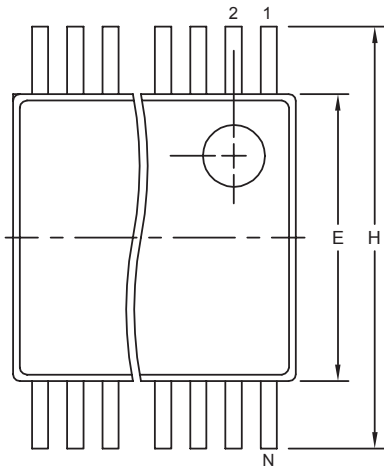
MAX5038/MAX5041

Dual-Phase, Parallelable, Average Current-Mode Controllers

Package Information

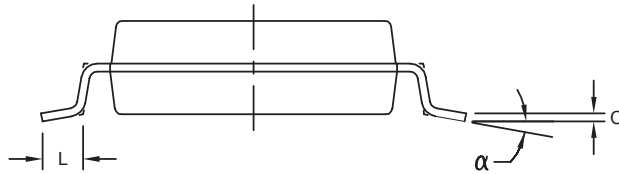
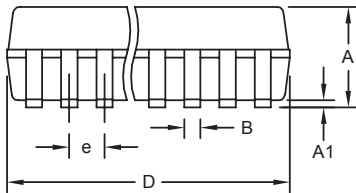
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.

SSOP/EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0 $^\infty$	8 $^\infty$	0 $^\infty$	8 $^\infty$

D	INCHES		MILLIMETERS		N
	MIN	MAX	MIN	MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

<small>PROPRIETARY INFORMATION</small>	
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM	
APPROVAL	DOCUMENT CONTROL NO. 21-0056
REV. C	1/1

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