

Click [here](#) to ask an associate for production status of specific part numbers.

## MAX20461

# Automotive High-Current Step-Down Converter with USB-C Protection/Host Charger

### General Description

The MAX20461 combines a 3A high-efficiency, automotive-grade, step-down converter, a USB Type-C/BC1.2 host charger emulator, and high bandwidth USB protection switches for automotive USB 2.0 host applications. The device also includes a USB load current-sense amplifier and a configurable feedback-adjustment circuit that provides automatic USB voltage compensation for voltage drops in captive cables often found in automotive applications. The device limits the USB load current using both a fixed internal peak-current threshold and a user-configurable external current-sense USB load threshold.

The MAX20461 is optimized for high-frequency operation and includes programmable frequency selection from 310kHz to 2.2MHz, allowing optimization of efficiency, noise, and board space based on the application requirements. The fully synchronous DC-DC converter integrates high-side and low-side MOSFETs with an external SYNC input/output, and can be configured for spread-spectrum operation.

The MAX20461 allows flexible configuration and advanced diagnostic options for both standalone and supervised applications. The device can be programmed using either external programming resistors and/or internal I<sup>2</sup>C registers via the I<sup>2</sup>C bus.

The MAX20461 is available in a small 5mm x 5mm 32-pin TQFN package and is designed to minimize required external components and layout area.

### Applications

- Automotive Radio and Navigation
- USB Port for Host and Hub Applications
- Automotive Connectivity/Telematics

### Benefits and Features

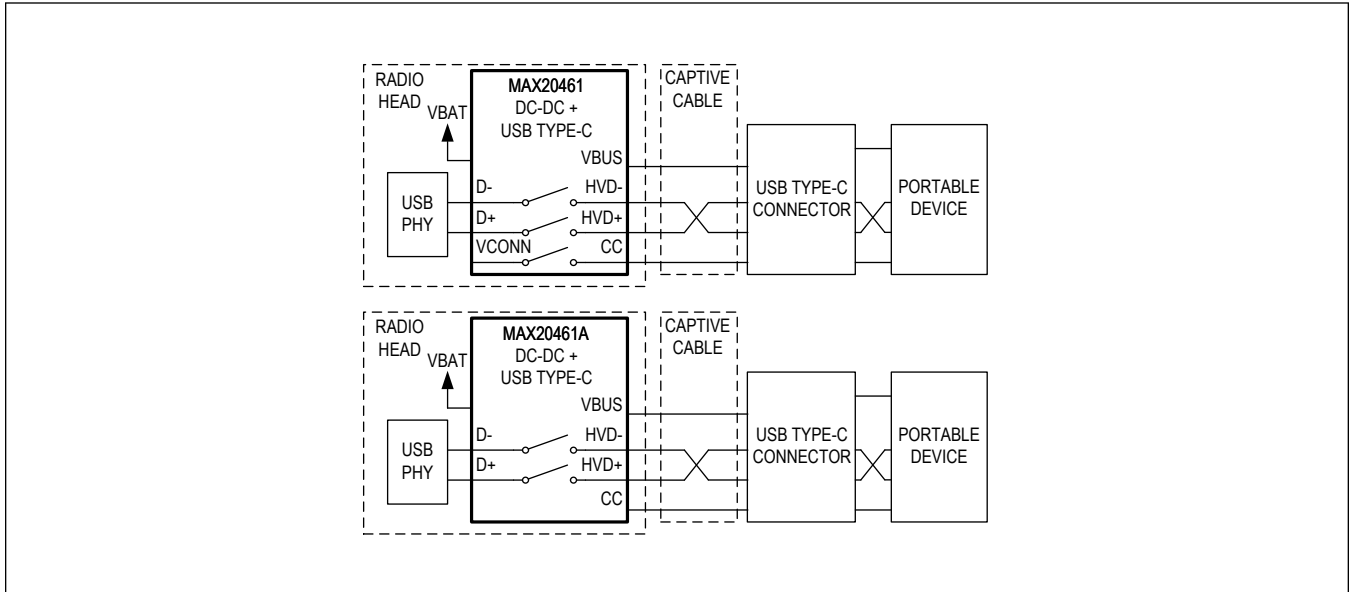
- One-Chip Type-C Solution Directly from Car Battery to Portable Device
  - MAX20461: USB Type-C Compliant DFP Controller with V<sub>CONN</sub> Protection
  - MAX20461A: USB Type-C Compliant DFP Controller
  - 1GHz Bandwidth USB 2.0 Data Switches
  - 4.5V to 28V Input (40V Load Dump), Synchronous Buck Converter
  - 5V to 7V, 3A Output Capability
- Optimal USB Charging and Communication for Portable Devices
  - User-Programmable Voltage Gain Adjusts Output for Up to 474mΩ Cable Resistance
  - User-Programmable USB Current Limit
  - Type-C Cable Orientation Indicator for USB3 Applications
  - Supports USB BC1.2 CDP and SDP Modes
  - Compatible with USB On-the-Go Specification and Apple CarPlay®
- Low-Noise Features Prevent Interference with AM Band and Portable Devices
  - Fixed-Frequency 310kHz to 2.2MHz Operation
  - Fixed-PWM Option at No Load
  - Spread Spectrum for EMI Reduction
  - SYNC Input/Output for Frequency Parking
- Robust Design Keeps Vehicle System and Portable Device Safe in an Automotive Environment
  - Short-to-Battery Protection on VBUS, HVD± Pins
  - CC1 and CC2 Tolerant to 20V Transients
  - Advanced Diagnostics Through I<sup>2</sup>C Bus
  - ±25kV Air/±8kV Contact ISO 10605 (330pF, 2kΩ)\*
  - ±15kV Air/±8kV Contact ISO 10605 (330pF, 2kΩ)\*\*
  - ±15kV Air/±8kV Contact ISO 10605 (330pF, 330Ω)\*
  - ±15kV Air/±8kV Contact IEC 61000-4-2 (150pF, 330Ω)\*
  - Overtemperature Protection, Warning, and Intelligent Current Foldback
  - -40°C to +125°C Operating Temperature Range

\*Tested in [Typical Application Circuit](#) as used on the MAX20461 Evaluation Kit with 1m captive cable.

\*\*Tested in [Typical Application Circuit](#) as used on the MAX20461 Evaluation Kit without 1m captive cable.

Ordering Information appears at end of datasheet.  
Apple and CarPlay are registered trademarks of Apple Inc.

Simplified Block Diagram



---

**TABLE OF CONTENTS**


---

General Description . . . . .	1
Applications . . . . .	1
Benefits and Features . . . . .	1
Simplified Block Diagram . . . . .	2
Absolute Maximum Ratings . . . . .	8
Package Information . . . . .	8
32 Pin TQFN 5x5x0.75mm . . . . .	8
32 Pin SWTQFN 5x5x0.75mm . . . . .	8
Electrical Characteristics . . . . .	9
Typical Operating Characteristics . . . . .	15
Pin Configurations . . . . .	18
MAX20461 . . . . .	18
MAX20461A . . . . .	19
Pin Description . . . . .	19
Functional Diagrams . . . . .	21
On-Channel -3dB Bandwidth and Crosstalk . . . . .	21
On-Capacitance . . . . .	21
DCDC_ON Reset Behavior and Timing Diagram . . . . .	22
ADC Timing Diagram . . . . .	23
ATTACH Logic Diagram . . . . .	24
Cable Attach-Detach and SENSN Discharge Timing Diagram . . . . .	24
Detailed Block Diagram . . . . .	25
Detailed Description . . . . .	27
USB Type-C . . . . .	27
Configuration Channel (CC1 and CC2) . . . . .	27
CC Polarity Output Pin (CC_POL) . . . . .	29
V <sub>CONN</sub> (MAX20461 Only) . . . . .	29
V <sub>BUS</sub> . . . . .	29
External FET Gate Drive (G_DMOS Pin) . . . . .	29
Legacy Devices . . . . .	29
Power-Up and Enabling . . . . .	29
System Enable (HVEN) . . . . .	29
DC-DC Enable (ENBUCK) . . . . .	30
3.3V Input (IN) . . . . .	31
Linear Regulator Output (BIAS) . . . . .	31
Power-On Sequencing . . . . .	31
Step-Down DC-DC Regulator . . . . .	31
Step-Down Regulator . . . . .	31
Wide Input Voltage Range . . . . .	31

**TABLE OF CONTENTS (CONTINUED)**

Maximum Duty-Cycle Operation . . . . .	31
Output Voltage (SENSP). . . . .	31
Soft-Start . . . . .	32
Reset Behavior . . . . .	32
Reset Criteria . . . . .	32
Switching Frequency Configuration. . . . .	32
Switching Frequency Synchronization (SYNC Pin) . . . . .	32
Forced-PWM Operation . . . . .	32
Intelligent Skip-Mode Operation and Attach Detection . . . . .	32
Spread-Spectrum Option. . . . .	33
Current Limit . . . . .	33
Output Short-Circuit Protection . . . . .	33
Thermal Overload Protection . . . . .	34
Pre-Thermal Overload Warning . . . . .	34
Automatic Thermal Foldback. . . . .	34
USB Current Limit and Output Voltage Adjustment . . . . .	34
Current-Sense Amplifier (SENSP, SENSN) . . . . .	34
USB DC Current Limit Configuration . . . . .	34
Voltage Feedback Adjustment Configuration . . . . .	34
Remote Sense Feedback Adjustment. . . . .	34
High Voltage Modes Configuration . . . . .	35
USB Protection Switches and BC1.2 Host Charger Emulation . . . . .	35
USB Protection Switches . . . . .	35
USB Host Charger Emulator . . . . .	35
USB On-The-Go and Dual-Role Applications . . . . .	37
I <sup>2</sup> C, Control, and Diagnostics . . . . .	37
I <sup>2</sup> C Configuration (CONFIG1 and I <sup>2</sup> C) . . . . .	37
Standalone Configuration (CONFIG1–CONFIG3) . . . . .	38
I <sup>2</sup> C Diagnostics and Event Handling . . . . .	39
Interrupt and Attach Output (INT(ATTACH)). . . . .	39
I <sup>2</sup> C Output Voltage and Current Measurement . . . . .	40
I <sup>2</sup> C Interface . . . . .	40
Bit Transfer . . . . .	40
STOP and START Conditions. . . . .	41
Early STOP Condition . . . . .	41
Clock Stretching . . . . .	41
I <sup>2</sup> C General Call Address . . . . .	41
I <sup>2</sup> C Slave Addressing . . . . .	41
Acknowledge. . . . .	41

**TABLE OF CONTENTS (CONTINUED)**

Write Data Format . . . . .	42
Read Data Format . . . . .	42
Fault Detection and Diagnostics . . . . .	42
Fault Detection . . . . .	42
Fault Output Pin (FAULT) . . . . .	42
Register Map . . . . .	44
Summary Table . . . . .	44
Register Details . . . . .	44
Applications Information . . . . .	55
DC-DC Switching Frequency Selection . . . . .	55
DC-DC Input Capacitor Selection . . . . .	55
DC-DC Output Capacitor Selection . . . . .	55
DC-DC Output Inductor Selection . . . . .	56
Layout Considerations . . . . .	56
Determining USB System Requirements . . . . .	56
USB Loads . . . . .	56
USB Output Current Limit . . . . .	57
USB Voltage Adjustment . . . . .	57
Tuning of USB Data Lines . . . . .	58
USB Data Line Common-Mode Choke Placement . . . . .	59
ESD Protection . . . . .	59
ESD Test Conditions . . . . .	60
Human Body Model . . . . .	60
IEC 61000-4-2 . . . . .	60
Typical Application Circuits . . . . .	62
Typical Application Circuit . . . . .	62
Ordering Information . . . . .	63
Revision History . . . . .	64

---

**LIST OF FIGURES**

---

Figure 1. Type-C Pullup Model . . . . .	28
Figure 2. USB Type-C Block Diagram . . . . .	30
Figure 3. Remote Cable-Sense Diagram . . . . .	35
Figure 4. Data Switch and Charge-Detection Block Diagram . . . . .	37
Figure 5. I <sup>2</sup> C Timing Diagram . . . . .	40
Figure 6. START, STOP and REPEATED START Conditions . . . . .	41
Figure 7. Acknowledge Condition . . . . .	42
Figure 8. Data Format of I <sup>2</sup> C Interface . . . . .	42
Figure 9. DC Voltage Adjustment Model . . . . .	57
Figure 10. Increase in SENSP vs. USB Current . . . . .	58
Figure 11. Tuning of Data Lines . . . . .	58
Figure 12. Near-Eye Diagram (with No Switch) . . . . .	59
Figure 13. Untuned Near-Eye Diagram (with MAX20461) . . . . .	59
Figure 14. Human Body ESD Test Model . . . . .	60
Figure 15. IEC 61000-4-2 ESD Test Model . . . . .	60
Figure 16. Human Body Current Waveform . . . . .	61
Figure 17. IEC 61000-4-2 Current Waveform . . . . .	61

---

**LIST OF TABLES**

---

Table 1. Charge Detection Precedence .....	27
Table 2. CC Pulldown Response .....	28
Table 3. CC Pulldown Response (MAX20461A) .....	28
Table 4. Type-C Source $V_{CONN}$ Requirements .....	29
Table 5. DC-DC Converter Intelligent Skip Mode Truth Table .....	33
Table 6. Data Switch Mode Truth Table (I <sup>2</sup> C Variants) .....	35
Table 7. Data Switch Mode Truth Table (Standalone Variants) .....	36
Table 8. CONFIG1 Pin Table (I <sup>2</sup> C Version) .....	38
Table 9. CONFIG1 Pin Table (Standalone Variants) .....	38
Table 10. CONFIG2 and CONFIG3 Pin Table (Standalone Variants) .....	39
Table 11. I <sup>2</sup> C Slave Addresses .....	41
Table 12. Fault Conditions .....	43
Table 13. Recommended Output Filters For $I_{LOAD}$ of 3A .....	56

## Absolute Maximum Ratings

SUPSW to PGND .....	-0.3V to +40V	LX Continuous RMS Current .....	3.5A
HVEN to PGND .....	-0.3V to $V_{SUPSW}+0.3V$	Output Short-Circuit Duration.....	Continuous
LX to PGND (Note 1).....	-0.3V to $V_{SUPSW}+0.3V$	Thermal Characteristics	
SYNC to AGND .....	-0.3V to $V_{BIAS}+0.3V$	Continuous Power Dissipation - Single Layer Board ( $T_A = +70^\circ\text{C}$ , 32-TQFN (derate 21.3mW/°C above +70°C))....	1702.1 mW
SENSN, SENSE, VBMON to AGND .....	-0.3V to $V_{SUPSW}+0.3V$	Continuous Power Dissipation - Multi Layer Board ( $T_A = +70^\circ\text{C}$ , 32-TQFN (derate 34.5mW/°C above +70°C))....	2758.6 mW
AGND to PGND .....	-0.3V to +0.3V	Operating Temperature Range .....	-40°C to +125°C
BST to PGND .....	-0.3V to +46V	Junction Temperature .....	+150°C
BST to LX .....	-0.3V to +6V	Storage Temperature Range.....	-40°C to +150°C
IN, CONFIG1, ENBUCK, SDA (CONFIG2), SCL (CONFIG3), BIAS, BCMODE, FAULT, CC_POL (SHIELD), CC1, CC2, VCONN, INT(ATTACH) to AGND.....	-0.3V to +6V	Lead Temperature (soldering, 10s).....	+300°C
HVDP, HVDM to AGND.....	-0.3V to +18V	Soldering Temperature (reflow).....	+260°C
DP, DM to AGND.....	-0.3V to $V_{IN}+0.3V$		
G_DMOS to AGND.....	-0.3V to +16V		

**Note 1:** Self-protected from transient voltages exceeding these limits for  $\leq 50\text{ns}$  in circuit under normal operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 32 Pin TQFN 5x5x0.75mm

Package Code	T3255+4C
Outline Number	<a href="#">21-0140</a>
Land Pattern Number	<a href="#">90-0012</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	47 °C/W
Junction to Case ( $\theta_{JC}$ )	1.70 °C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	29 °C/W
Junction to Case ( $\theta_{JC}$ )	1.70 °C/W

### 32 Pin SWTQFN 5x5x0.75mm

Package Code	T3255Y+4C
Outline Number	<a href="#">21-100214</a>
Land Pattern Number	<a href="#">90-100082</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	47 °C/W
Junction to Case ( $\theta_{JC}$ )	1.70 °C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	29 °C/W
Junction to Case ( $\theta_{JC}$ )	1.70 °C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).



## Electrical Characteristics

( $V_{SUSPW} = 14V$ ,  $V_{IN} = 3.3V$ ,  $V_{ENBUCK} = 3.3V$ ,  $V_{VCONN} = 5V$ , Temperature =  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply and Enable</b>						
Supply Voltage Range	$V_{SUSPW}$	(Note 2)	4.5		28	V
Load Dump Event Supply Voltage Range	$V_{SUSPW\_LD}$	< 1s			40	V
Supply Current - Off State	$I_{SUSPW}$	$V_{SUSPW} = 18V$ ; $V_{HVEN} = 0V$ ; $V_{IN} = 0V$ ; $V_{CONN} = 0V$ , Off State		10	20	$\mu A$
Supply Current - Buck Off	$I_{SUSPW}$	$V_{HVEN} = 14V$ ; $V_{ENBUCK} = 0V$		1.1		mA
Supply Current - Skip Mode	$I_{SUSPW}$	$V_{HVEN} = 14V$ ; buck switching; no load		1.8		mA
Supply Current - FPWM	$I_{SUSPW}$	$V_{HVEN} = 14V$ ; buck switching; no load		28		mA
BIAS Voltage	$V_{BIAS}$	$5.75V \leq V_{SUSPW} \leq 28V$	4.5	4.7	5.25	V
BIAS Current Limit			50	150		mA
BIAS Undervoltage Lockout	$V_{UV\_BIAS}$	$V_{BIAS}$ rising	3.0	3.3	3.6	V
BIAS Undervoltage Lockout Hysteresis				0.2		V
SUSPW Undervoltage Lockout	$V_{UV\_SUSPW}$	$V_{SUSPW}$ rising	3.9		4.42	V
SUSPW Undervoltage Lockout Hysteresis				0.2		V
IN Voltage Range	$V_{IN}$		3		3.6	V
IN Overvoltage Lockout	$V_{IN\_OVLO}$	$V_{IN}$ rising	3.8	4	4.3	V
IN Input Current	$I_{IN}$				10	$\mu A$
HVEN Rising Threshold	$V_{HVEN\_R}$		0.6	1.5	2.4	V
HVEN Falling Threshold	$V_{HVEN\_F}$				0.4	V
HVEN Hysteresis	$V_{HVEN}$			0.2		V
HVEN Delay Rising	$t_{HVEN\_R}$		2.5		15	$\mu s$
HVEN Delay Falling	$t_{HVEN\_F}$		5	12	25	$\mu s$
HVEN Input Leakage		$V_{HVEN} = V_{SUSPW} = 18V$ , $V_{HVEN} = 0V$			10	$\mu A$
<b>G_DMOS Pin</b>						
G_DMOS Unloaded Output Voltage	$V_{G\_DMOS\_OC}$	$V_{G\_DMOS}$ to $V_{BIAS}$ , internal discharge path $2M\Omega$ to GND	7	10	13.0	V
G_DMOS Output Impedance	$R_{G\_DMOS\_OC}$			100	250	k $\Omega$
G_DMOS DC Output Current	$I_{G\_DMOS\_SC}$	G_DMOS to BIAS		20		$\mu A$
<b>USB Type C / Power Requirements (MAX20461 Only)</b>						
VCONN Source Voltage Input	$V_{VCONN\_IN}$	1W (3.3V/305mA, 5.5V/185mA) (Note 3)	3.3		5.5	V
VCONN On Resistance	$R_{ON\_VCONN}$	Resistance from $V_{CONN}$ to CC1 and CC2, $V_{CONN} = 5V$		600	1200	m $\Omega$

**Electrical Characteristics (continued)**

( $V_{SUPSW} = 14V$ ,  $V_{IN} = 3.3V$ ,  $V_{ENBUCK} = 3.3V$ ,  $V_{VCONN} = 5V$ , Temperature =  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCONN Current Limit	$I_{LIM\_VCONN}$	Measured on CC1 and CC2. $3.60V \leq V_{CONN} \leq 5.5V$	310	400		mA
VCONN UVLO Threshold	$V_{VCONN\_UVLO}$		2.2	2.45	2.65	V
VCONN to CC1/CC2 Discharge Resistance	$R_{DCH}$			3	6.2	k $\Omega$
<b>USB Type C / Current Level Characteristics</b>						
CC DFP 0.5A Current Source	$I_{DFP0.5\_CC}$	$4.0V < V_{BIAS} < 5.5V, \pm 20\%$	64	80	96	$\mu A$
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC}$	$4.0V < V_{BIAS} < 5.5V, \pm 8\%$	166	180	194	$\mu A$
CC DFP 3.0A Current Source	$I_{DFP3.0\_CC}$	$4.0V < V_{BIAS} < 5.5V, \pm 8\%$	304	330	356	$\mu A$
<b>USB Type C / Timing Characteristics</b>						
Type-C CC Pin Detection Debounce	$t_{CCDEBOUNCE}$	Final transition to Attached states		160		ms
<b>DP, DM Analog USB Switches</b>						
On-Channel -3dB Bandwidth	BW	$R_L = R_S = 50\Omega$		1000		MHz
Analog Signal Range			0		3.6	V
Protection Trip Threshold	$V_{OV\_D}$		3.65	3.85	4.1	V
Protection Response Time	$t_{FP\_D}$	$V_{IN} = 4.0V, V_{HVD\pm} = 3.3V$ to $4.3V$ step, $R_L = 15k\Omega$ on $D\pm$ , delay to $V_{D\pm} < 3V$		2		$\mu s$
On-Resistance Switch A	$R_{ON\_SA}$	$I_L = 10mA, V_{D\pm} = 0V$ to $V_{IN}, V_{IN} = 3.0V$ to $3.6V$		4	8	$\Omega$
On-Resistance Match between Channels Switch A	$\Delta R_{ON\_SA}$	$I_L = 10mA, V_{D\pm} = 1.5V$ or $3.0V$			0.2	$\Omega$
On-Resistance Flatness Switch A	$R_{FLAT(ON)A}$	$I_L = 10mA, V_{D\_} = 0V$ or $0.4V$		0.01		$\Omega$
On Resistance of HVD+/HVD- short	$R_{SHORT}$	$V_{DP} = 1V, I_{DM} = 500\mu A$		90	180	$\Omega$
HVD+/HVD- On-Leakage Current	$I_{HVD\_ON}$	$V_{HVD\pm} = 3.6V$ or $0V$	-7		7	$\mu A$
HVD+/HVD- Off-Leakage Current	$I_{HVD\_OFF}$	$V_{HVD\pm} = 18V, V_{D\pm} = 0V$			150	$\mu A$
D+/D- Off-Leakage Current	$I_{D\_OFF}$	$V_{HVD\pm} = 18V, V_{D\pm} = 0V$	-1		1	$\mu A$
<b>Current-Sense Amplifier (SENSP, SENSN) and Analog Inputs (VBMON)</b>						
Gain		$10mV < V_{SENSP} - V_{SENSN} < 110mV$ , $GAIN[4:0] = 0b11111$		19.4		V/V
Cable Compensation LSB	$R_{LSB}$			18		m $\Omega$

**Electrical Characteristics (continued)**

( $V_{SUSPW} = 14V$ ,  $V_{IN} = 3.3V$ ,  $V_{ENBUCK} = 3.3V$ ,  $V_{VCONN} = 5V$ , Temperature =  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overcurrent Threshold	ILIM_SET	ILIM[2:0] = 0b111, $R_{SENSE} = 33m\Omega$	3.04	3.14	3.30	A
		ILIM[2:0] = 0b110, $R_{SENSE} = 33m\Omega$	2.6	2.75	2.9	
		ILIM[2:0] = 0b101, $R_{SENSE} = 33m\Omega$	2.1	2.25	2.4	
		ILIM[2:0] = 0b100, $R_{SENSE} = 33m\Omega$	1.62	1.7	1.78	
		ILIM[2:0] = 0b011, $R_{SENSE} = 33m\Omega$	1.05	1.13	1.21	
		ILIM[2:0] = 0b010, $R_{SENSE} = 33m\Omega$	0.8	0.86	0.92	
		ILIM[2:0] = 0b001, $R_{SENSE} = 33m\Omega$	0.55	0.6	0.65	
		ILIM[2:0] = 0b000, $R_{SENSE} = 33m\Omega$	0.3	0.33	0.36	
SENSN / VBMON Discharge Current	$I_{SENSN\_DIS}$		11	18	32	mA
Startup Wait Time	$t_{BUCK\_WAIT}$			100		ms
SENSN / VBMON Discharge Time	$t_{DIS\_POR}$	Discharge after POR		1		s
	$t_{DIS\_CD}$	DCDC_ON toggle		2		
	$t_{DIS\_DET}$	Type-C detach		100		ms
Forced Buck Off-Time	$t_{BUCKOFF\_CD}$	DCDC_ON toggle; see reset criteria		2		s
	$t_{BUCKOFF\_DET}$	Type-C detach		100		ms
Attach Comparator Load Current Rising Threshold		Common mode input = 5.15V	5	16	28	mA
Attach Comparator Hysteresis		Common mode input = 5.15V		2.5		mA
SENSN Undervoltage Threshold (Falling)	$V_{UV\_SENSN}$		4	4.375	4.75	V
SENSN Overvoltage Threshold (Rising)	$V_{OV\_SENSN}$		7	7.46	7.9	V
SENSN Short Circuit Threshold (Falling)	$V_{SHT\_SENSN}$		1.75	2	2.25	V
SENSN Undervoltage Fault Blanking Time				16		ms
SENSN Overvoltage Fault Blanking Time	$t_{B,OV\_SENSN}$	From overvoltage condition to $\overline{FAULT}$ asserted		3	6	$\mu s$
SENSN Discharge Threshold Falling		$V_{SENSN}$ Falling	0.47	0.51	0.57	V
<b>Remote Feedback Adjustment</b>						
SHIELD Input Voltage Range			0.1		0.75	V
Gain			1.935	2	2.065	V/V
Input Referred Offset Voltage				$\pm 2.0$		mV
<b>Digital Inputs (SDA, SCL, ENBUCK, BCMODE)</b>						
Input Leakage Current		$V_{PIN} = 5.5V, 0V$	-5		5	$\mu A$

**Electrical Characteristics (continued)**

( $V_{SUPSW} = 14V$ ,  $V_{IN} = 3.3V$ ,  $V_{ENBUCK} = 3.3V$ ,  $V_{VCONN} = 5V$ , Temperature =  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic High	$V_{IH}$		1.6			V
Logic Low	$V_{IL}$				0.5	V
<b>USB 2.0 Host Charger Emulator (HVD+/HVD-, D+/D-)</b>						
Input Logic High	$V_{IH}$		2.0			V
Input Logic Low	$V_{IL}$				0.8	V
Data Sink Current	$I_{DAT\_SINK}$	$V_{DAT\_SINK} = 0.25V$ to $0.4V$	50	100	150	$\mu A$
Data Detect Voltage High	$V_{DAT\_REFH}$		0.4			V
Data Detect Voltage Low	$V_{DAT\_REFL}$				0.25	V
Data Detect Voltage Hysteresis	$V_{DAT\_HYST}$			60		mV
Data Source Voltage	$V_{DAT\_SRC}$	$I_{SRC} = 200\mu A$	0.5		0.7	V
<b>Synchronous Step-Down DC-DC Converter</b>						
PWM Output Voltage	$V_{SENSP}$	$7V \leq V_{SUPSW} \leq 28V$ , No Load		5.15		V
Skip Mode Output Voltage	$V_{SENSP\_SKIP}$	$7V \leq V_{SUPSW} \leq 18V$ , No Load (Note 2)		5.25		V
Load Regulation	$R_{LR}$	$7V \leq V_{SUPSW} \leq 18V$ , for 5V nominal output setting		51		m $\Omega$
Output Voltage Accuracy		$8V \leq V_{SUPSW} \leq 18V$ , 2.4A, $V_{SENSP} - V_{SENSN} = 79.2mV$ , GAIN[4:0] = 0b111111 cable compensation.	6.33		6.68	V
Spread Spectrum Range		SS Enabled		$\pm 3.4$		%
SYNC Switching Threshold High	$V_{SYNC\_HI}$	Rising	1.4			V
SYNC Switching Threshold Low	$V_{SYNC\_LO}$	Falling			0.4	V
SYNC Internal Pulldown				200		k $\Omega$
SYNC Input Clock Acquisition Time	$t_{SYNC}$	(Note 4)		1		Cycles
High-Side Switch On-Resistance	$R_{ONH}$	$I_{LX} = 1A$		54	95	m $\Omega$
Low-Side Switch On-Resistance	$R_{ONL}$	$I_{LX} = 1A$		72	135	m $\Omega$
BST Input Current	$I_{BST}$	$V_{BST} - V_{LX} = 5V$ , High-side on		2.2		mA
LX Current-Limit Threshold		All Other Variants		5		A
		MAX20461AATJM, MAX20461AATJP The min value is guaranteed by design at $T_A = T_J = 25^{\circ}C$ .	5	6		
Skip Mode Peak-Current Threshold	$I_{SKIP\_TH}$			1		A
Negative Current Limit				1.2		A

**Electrical Characteristics (continued)**

( $V_{SUPSW} = 14V$ ,  $V_{IN} = 3.3V$ ,  $V_{ENBUCK} = 3.3V$ ,  $V_{VCONN} = 5V$ , Temperature =  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Ramp Time	$t_{SS}$			8		ms
LX Rise Time		(Note 4)		3		ns
LX Fall Time		(Note 4)		4		ns
BST Refresh Algorithm Low-Side Minimum On-Time				60		ns
<b>CC_POL, FAULT, INT (ATTACH), SYNC Outputs</b>						
Output-High Leakage Current		$\overline{FAULT}$ , $\overline{INT(ATTACH)}$ , $CC\_POL = 5.5V$	-10		10	$\mu A$
Output Low Level		Sinking 1mA			0.4	V
SYNC Output High Level		Sourcing 1mA, SYNC configured as output	$V_{BIAS} - 0.4$			V
<b>Config Resistors Converter</b>						
CONFIG1-3 Current Leakage		$V_{CONFIG} = 0V$ to $4V$			$\pm 5$	$\mu A$
Minimum Window Amplitude			-4		4	%
<b>ADC</b>						
Resolution				8		Bits
ADC Gain Error				$\pm 2$		LSBs
Offset Error	Offset_ADC			$\pm 1$		LSB
<b>Oscillators</b>						
Internal High-Frequency Oscillator	HFOSC		7	8	9	MHz
Buck Oscillator Frequency	$f_{SW}$	$FSW[2:0] = 0b000$	1.95	2.2	2.45	MHz
Buck Oscillator Frequency	$f_{SW}$	$FSW[2:0] = 0b101$	340	410	480	kHz
<b>Thermal Overload</b>						
Thermal Warning Temperature				140		$^{\circ}C$
Thermal Warning Hysteresis				10		$^{\circ}C$
Thermal Shutdown Temperature				165		$^{\circ}C$
Thermal Shutdown Hysteresis				10		$^{\circ}C$
<b>I<sup>2</sup>C</b>						
Serial Clock Frequency	$f_{SCL}$				400	kHz
Bus Free Time Between STOP and START Condition	$t_{BUF}$		1.3			$\mu s$

**Electrical Characteristics (continued)**

( $V_{SUPSW} = 14V$ ,  $V_{IN} = 3.3V$ ,  $V_{ENBUCK} = 3.3V$ ,  $V_{VCONN} = 5V$ , Temperature =  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition Setup Time	$t_{SU:STA}$		0.6			$\mu s$
START Condition Hold Time	$t_{HD:STA}$		0.6			$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$		0.6			$\mu s$
Clock Low Period	$t_{LOW}$		1.3			$\mu s$
Clock High Period	$t_{HIGH}$		0.6			$\mu s$
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.6	$\mu s$
Pulse Width of Spike Suppressed	$t_{SP}$			50		ns
<b>ESD Protection (All Pins)</b>						
ESD Protection Level	$V_{ESD}$	Human Body Model		$\pm 2$		kV
<b>ESD Protection (HVDP, HVDM, CC1, CC2)</b>						
ESD Protection Level	$V_{ESD}$	ISO 10605 Air Gap (330pF, 2k $\Omega$ )		$\pm 25$		kV
		ISO 10605 Contact (330pF, 2k $\Omega$ )		$\pm 8$		
		IEC 61000-4-2 Air Gap (150pF, 330 $\Omega$ )		$\pm 15$		
		IEC 61000-4-2 Contact (150pF, 330 $\Omega$ )		$\pm 8$		
		ISO 10605 Air-Gap (330pF, 330 $\Omega$ )		$\pm 15$		
		ISO 10605 Contact (330pF, 330 $\Omega$ )		$\pm 8$		

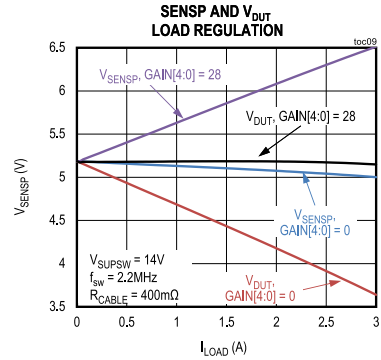
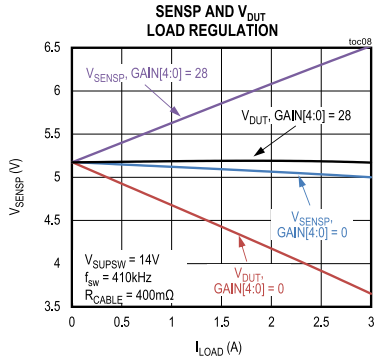
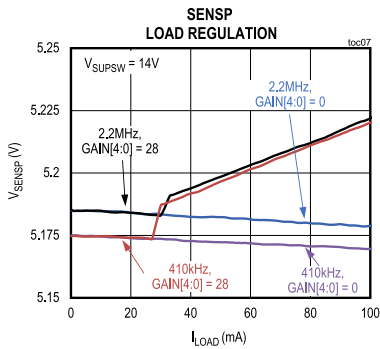
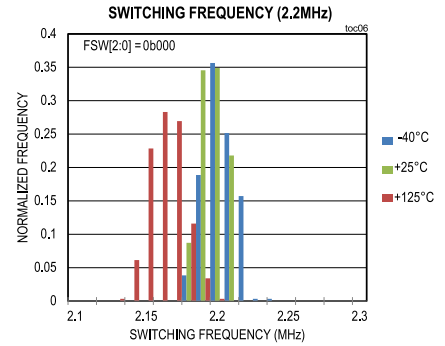
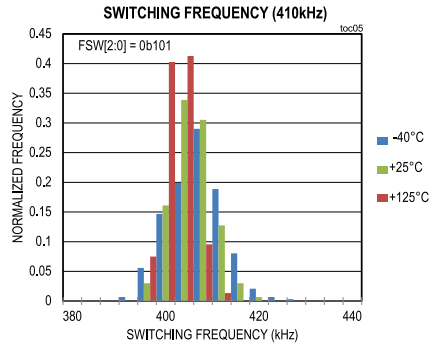
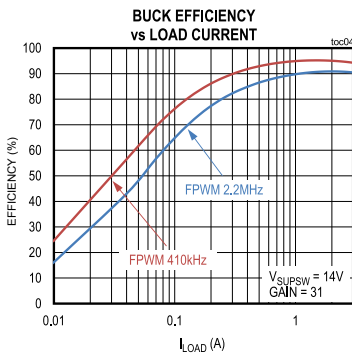
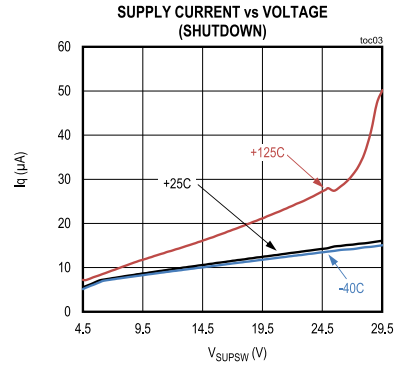
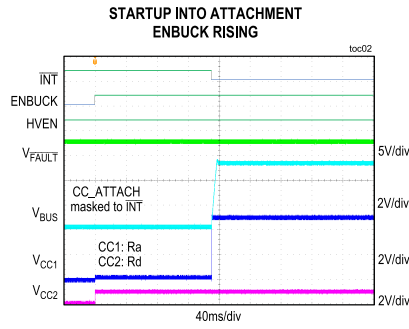
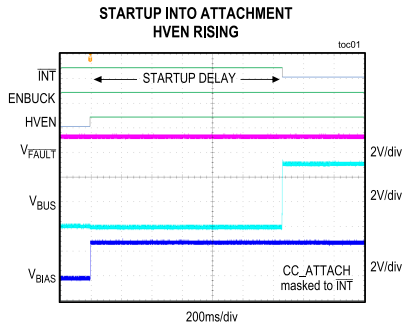
**Note 2:** Device is designed for use in applications with continuous operation of 14V. Device meets electrical table up to maximum supply voltage.

**Note 3:** The IR drop of the system must be considered when selecting the  $V_{CONN}$  pin source voltage.

**Note 4:** Guaranteed by design and bench characterization; not production tested.

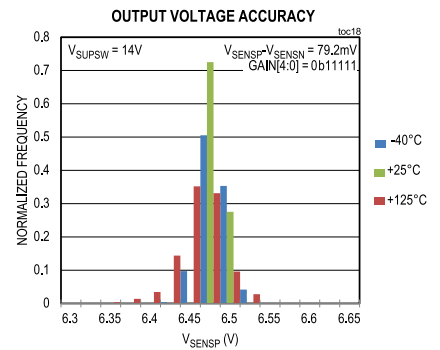
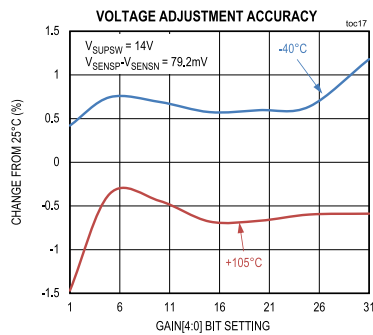
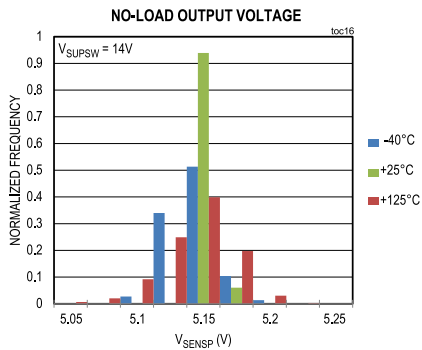
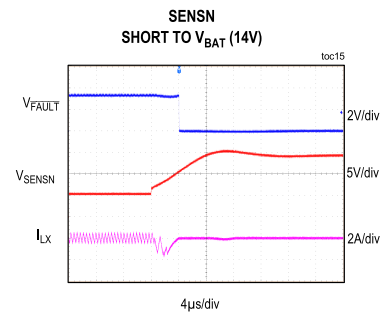
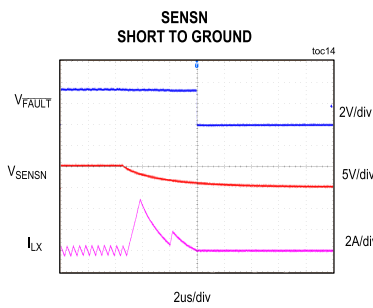
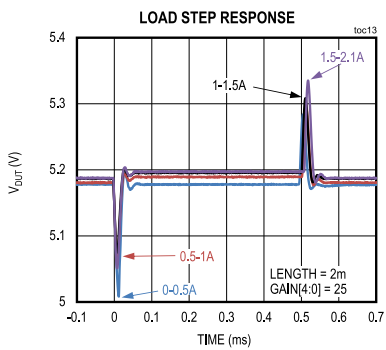
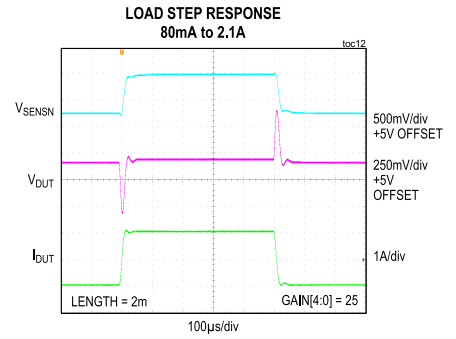
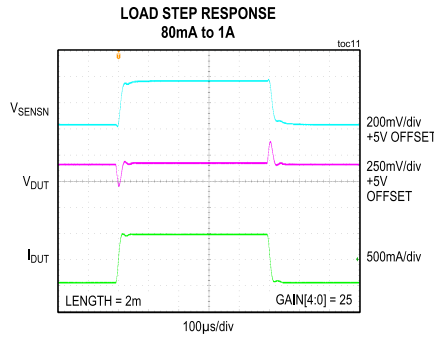
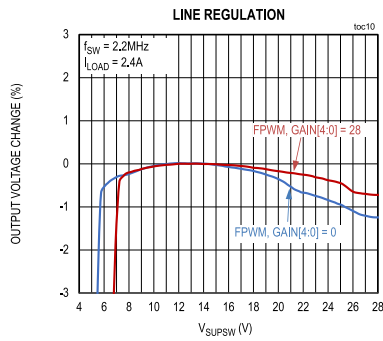
Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



Typical Operating Characteristics (continued)

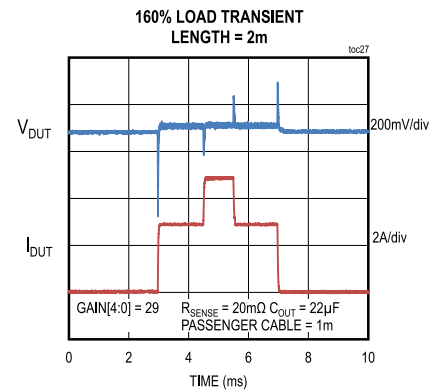
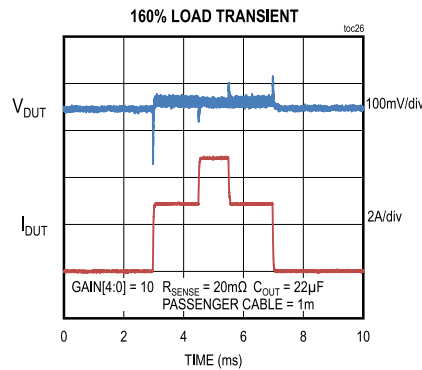
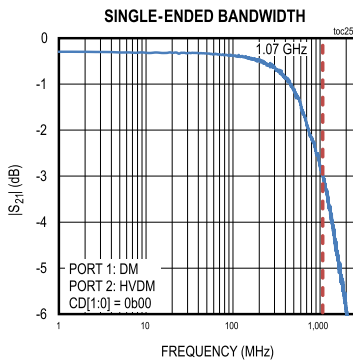
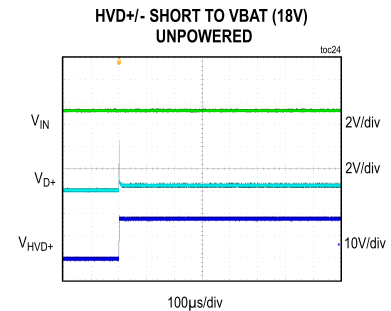
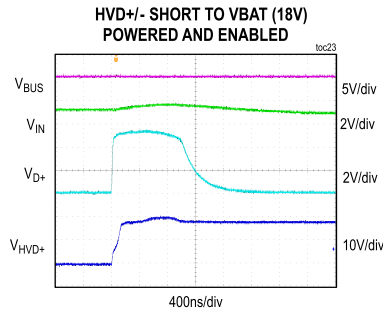
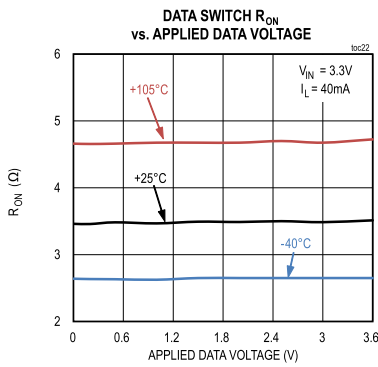
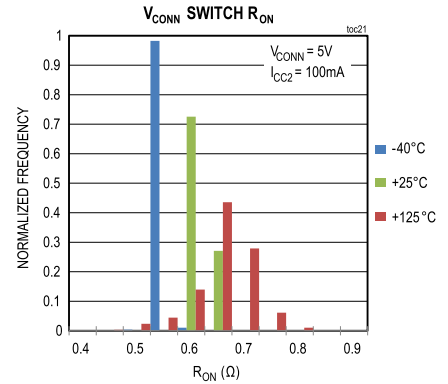
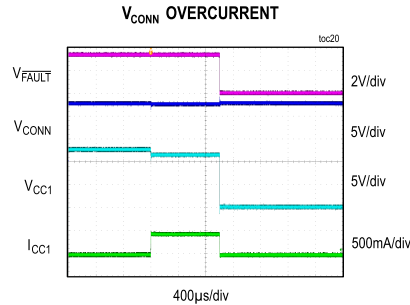
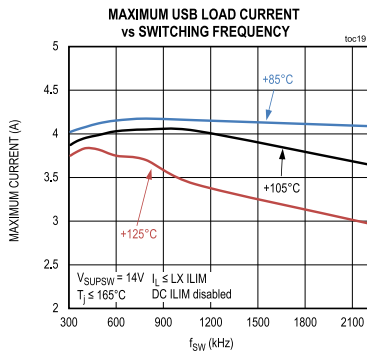
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)





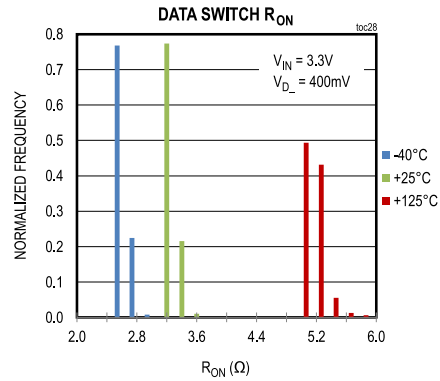
Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



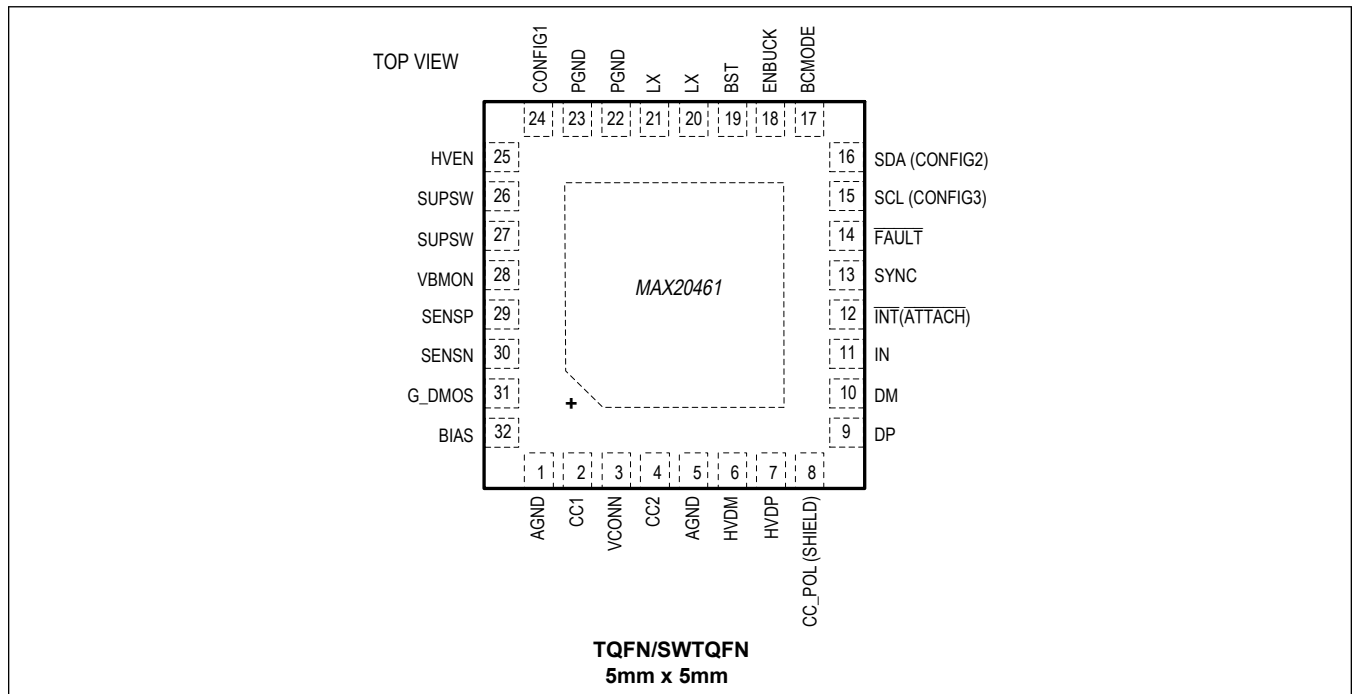
Typical Operating Characteristics (continued)

(T<sub>A</sub> = +25°C, unless otherwise noted.)

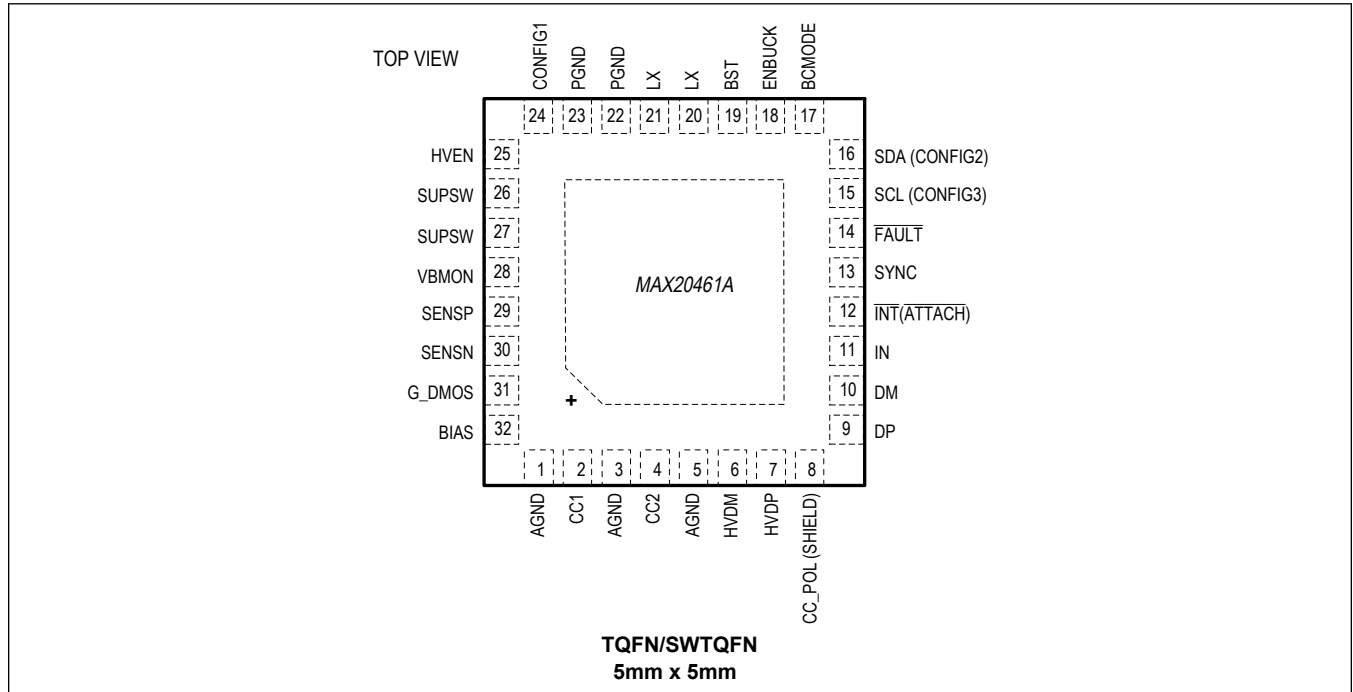


Pin Configurations

MAX20461



MAX20461A



Pin Description

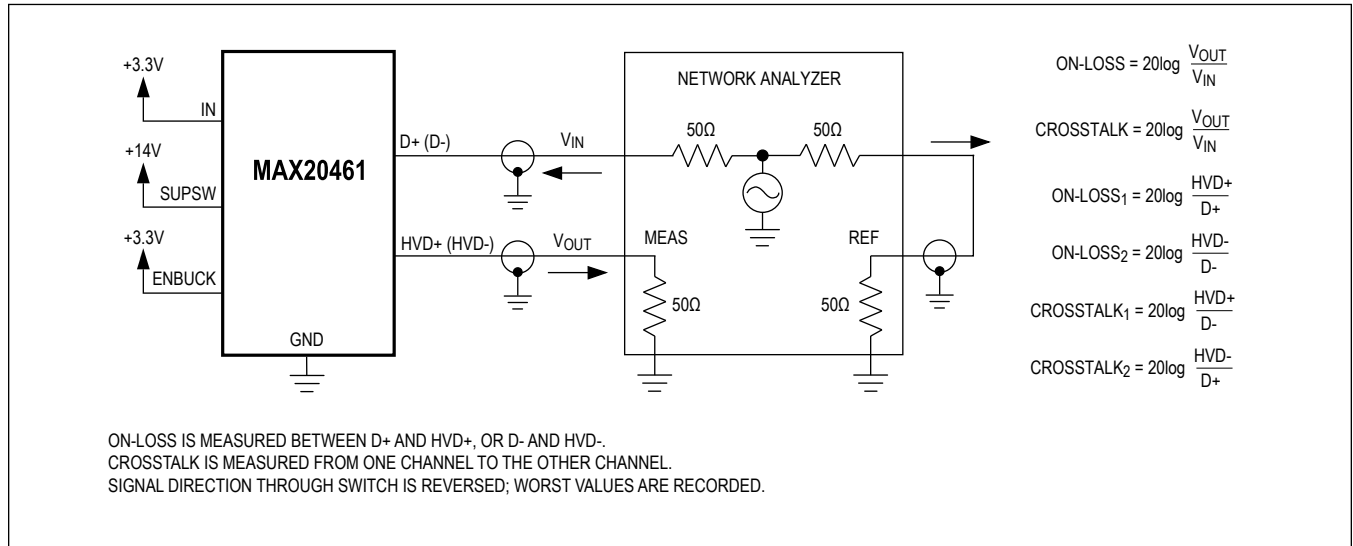
PIN		NAME	FUNCTION
MAX20461	MAX20461A		
1, 5	1, 3, 5	AGND	Analog Ground.
2	2	CC1	Type-C Configuration Channel (CC).
3	—	VCONN	Power Source. Supplies power to the unused CC pin if required.
4	4	CC2	Type-C Configuration Channel (CC).
6	6	HVDM	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- to the downstream USB connector D- pin.
7	7	HVDP	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ to the downstream USB connector D+ pin.
8	8	CC_POL (SHIELD)	In USB-C Configuration, CC_POL Output. In BC1.2 only variant, remote feedback input. See <a href="#">Figure 3</a> .
9	9	DP	USB Differential Data D+ Input. Connect D+ to the low-voltage USB transceiver D+ pin.
10	10	DM	USB Differential Data D- Input. Connect D- to the low-voltage USB transceiver D- pin.
11	11	IN	Logic Enable Input. Connect to I/O voltage of USB transceiver. IN is also used for clamping during overvoltage events on HVD+ or HVD-. Connect a 1µF-10µF ceramic capacitor from IN to GND.
12	12	$\overline{\text{INT}}$ (ATTACH)	In I <sup>2</sup> C variants, functions as an active-low INT pin. In standalone variants, functions as active-low Attach. Connect a 100kΩ pullup resistor to IN.
13	13	SYNC	Switching frequency Input/Output for synchronization with other supplies. See <a href="#">Applications Information</a> section.

## Pin Description (continued)

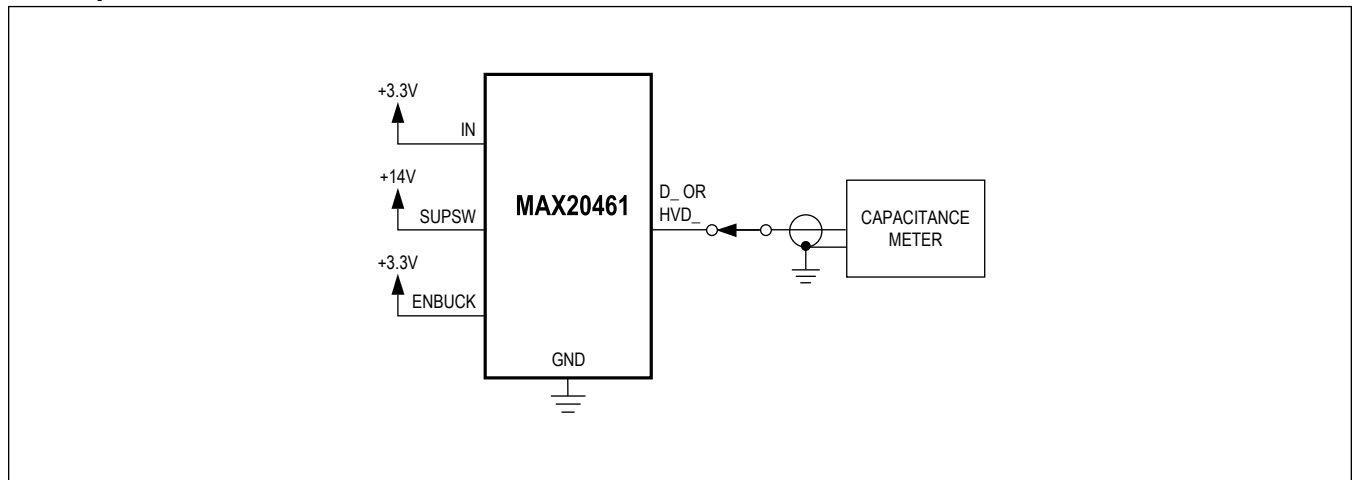
PIN		NAME	FUNCTION
MAX20461	MAX20461A		
14	14	$\overline{\text{FAULT}}$	Active-low, open-drain, fault indicator output. Connect a 100k $\Omega$ pullup resistor to the IN pin.
15	15	SCL (CONFIG3)	In I <sup>2</sup> C variants, this serves as the I <sup>2</sup> C SCL Pin. In standalone variants, this serves as CONFIG3 pin. See <a href="#">Table 10</a> .
16	16	SDA (CONFIG2)	In the I <sup>2</sup> C variants, this serves as the I <sup>2</sup> C SDA Pin. In standalone variants, this serves as CONFIG2 pin. See <a href="#">Table 10</a> .
17	17	BCMODE	This pin selects between the two modes of data switch operation. The modes are defined in the <a href="#">Data Switch Mode Truth Table</a> .
18	18	ENBUCK	DC-DC Enable Input. Drive high/low to enable/disable the buck converter.
19	19	BST	High-Side Driver Supply. Connect a 0.1 $\mu$ F capacitor from BST to LX.
20, 21	20, 21	LX	Inductor connection. Connect an inductor from LX to the DC-DC converter output (SENSP).
22, 23	22, 23	PGND	Power Ground.
24	24	CONFIG1	Configuration. Connect a resistor to GND to set default configuration. See <a href="#">Table 8</a> and <a href="#">Table 9</a> .
25	25	HVEN	Active-high system enable pin. HVEN is battery-voltage tolerant.
26, 27	26, 27	SUPSW	Internal High-Side Switch Supply Input. V <sub>SUPSW</sub> provides power to the internal switch and LDO. Connect a 10 $\mu$ F ceramic capacitor in parallel with a 47 $\mu$ F electrolytic capacitor from SUPSW to PGND. See the <a href="#">DC-DC Input Capacitor</a> section.
28	28	VBMON	USB VBUS monitor.
29	29	SENSP	DC-DC converter feedback input and current-sense amplifier positive input. DC-DC bulk capacitance placed here. Connect to positive terminal of current-sense resistor (R <sub>SENSE</sub> ) and the main output of the converter. Used for internal voltage regulation loop.
30	30	SENSN	Current-sense amplifier negative input. Connect to negative terminal of current-sense resistor (R <sub>SENSE</sub> ).
31	31	G_DMOS	Gate drive output. Optionally connect to the gate of an external N-channel FET, otherwise terminate with 10pF.
32	32	BIAS	5V linear regulator output. Connect a 2.2 $\mu$ F ceramic capacitor from BIAS to GND. BIAS powers the internal circuitry.
EP	EP	EP	Exposed pad. Connect EP to multiple GND planes with 3 x 3 via grid (minimum).

Functional Diagrams

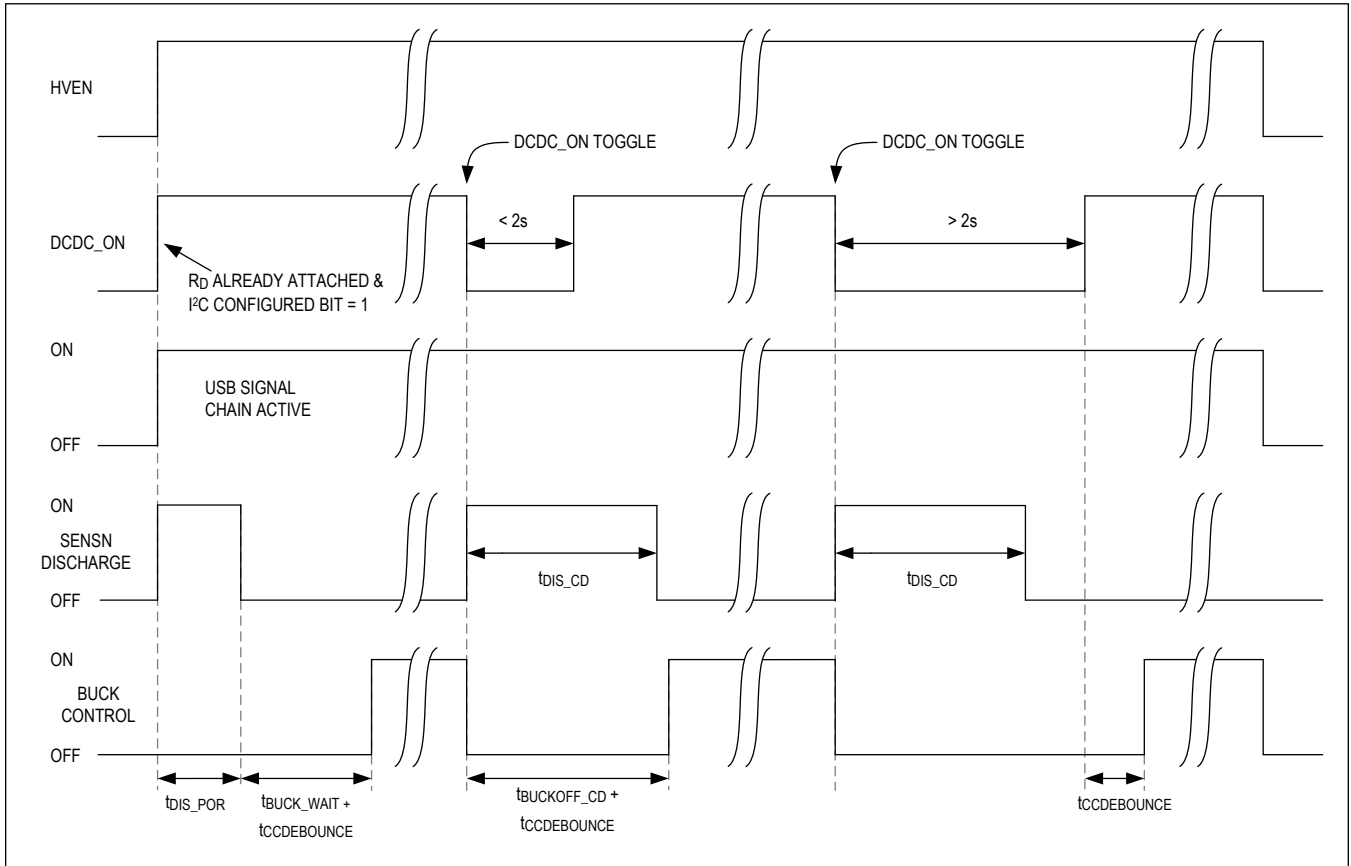
On-Channel -3dB Bandwidth and Crosstalk



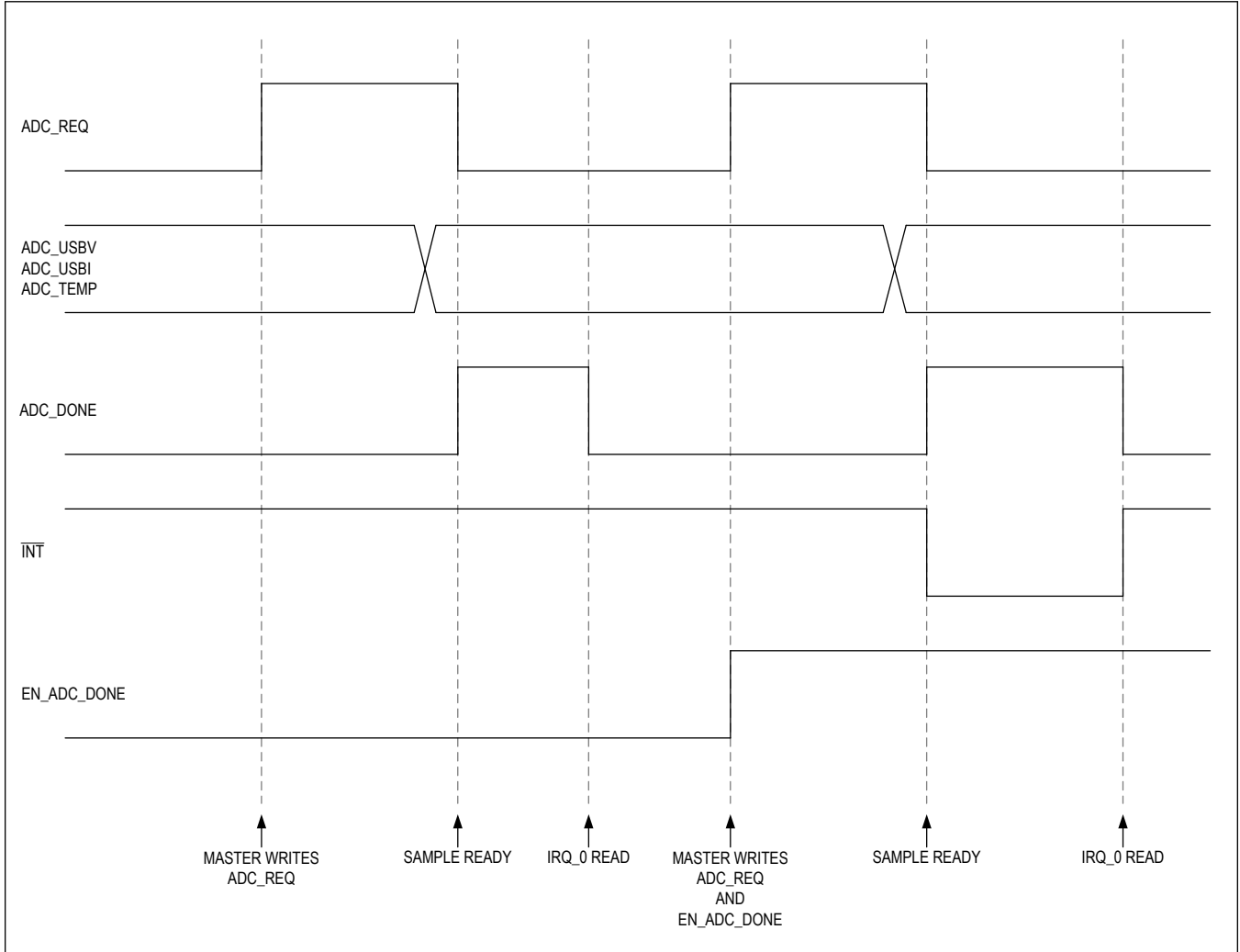
On-Capacitance



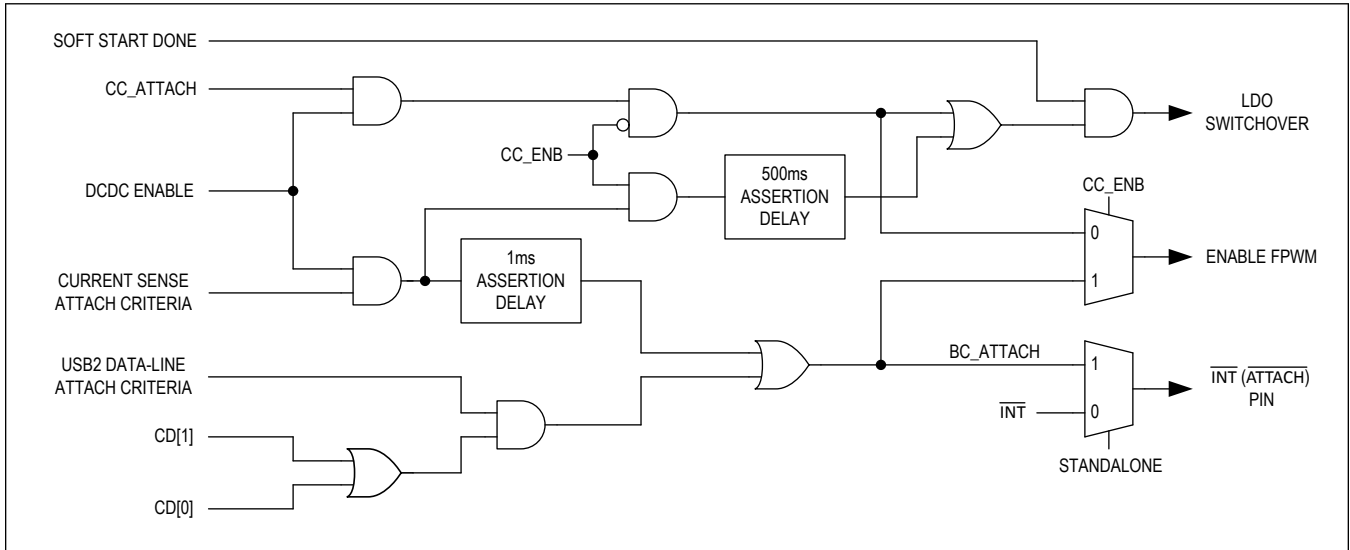
**DCDC\_ON Reset Behavior and Timing Diagram**



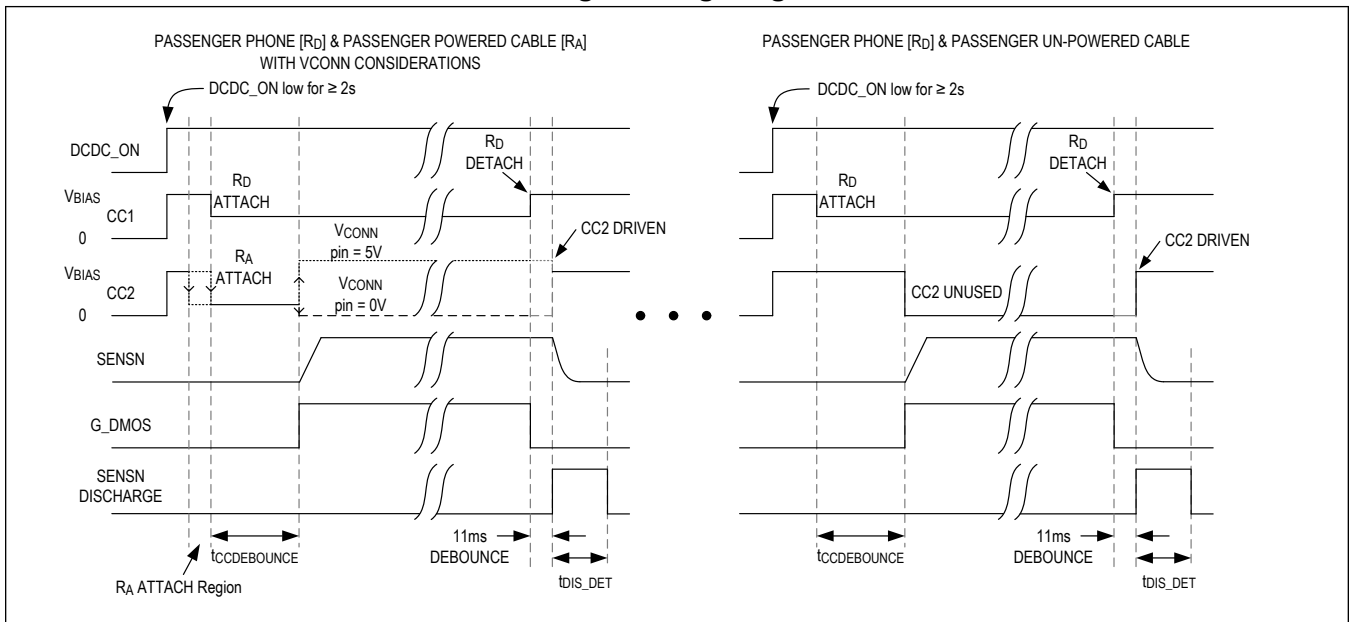
ADC Timing Diagram



**ATTACH Logic Diagram**

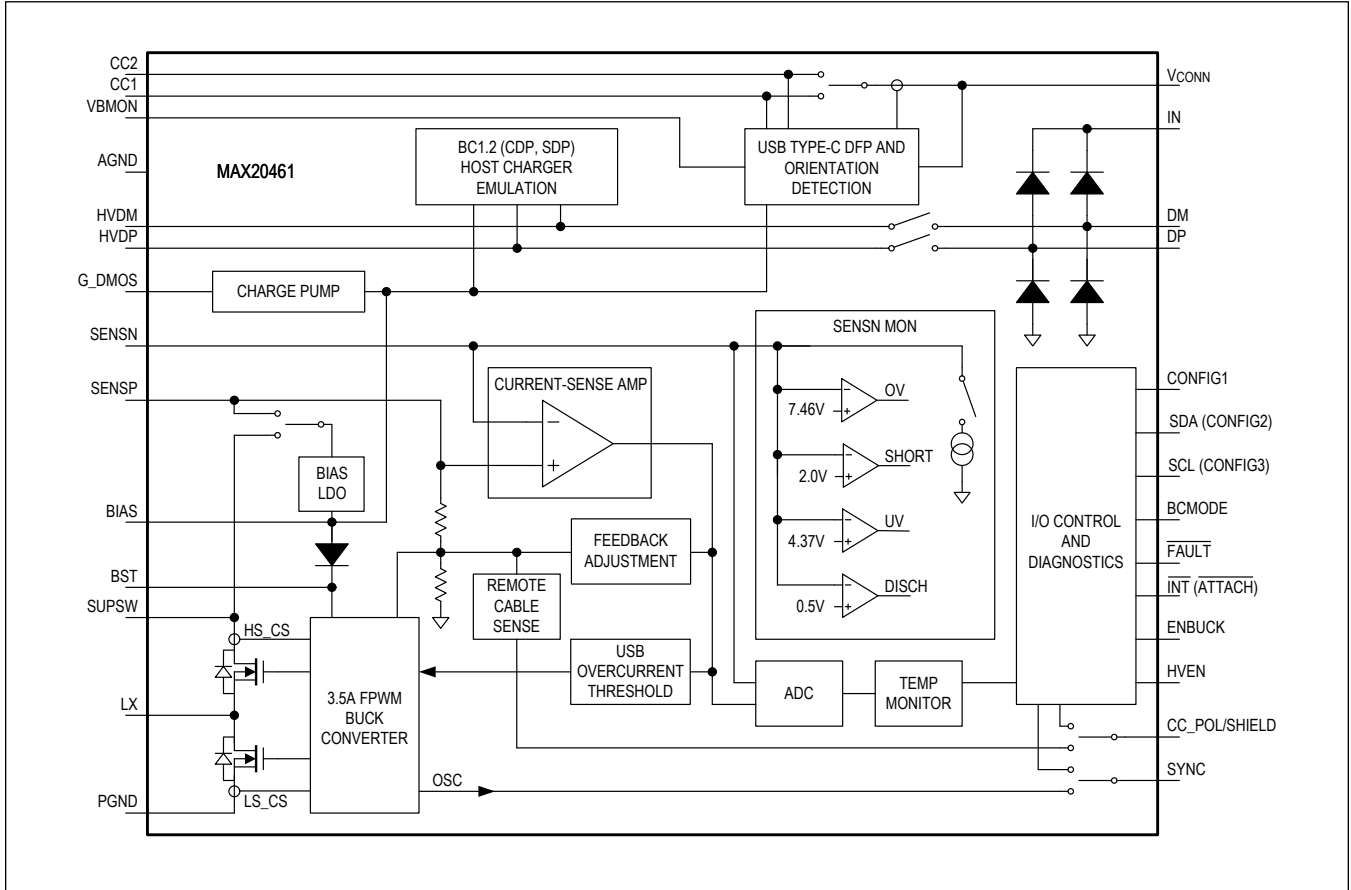


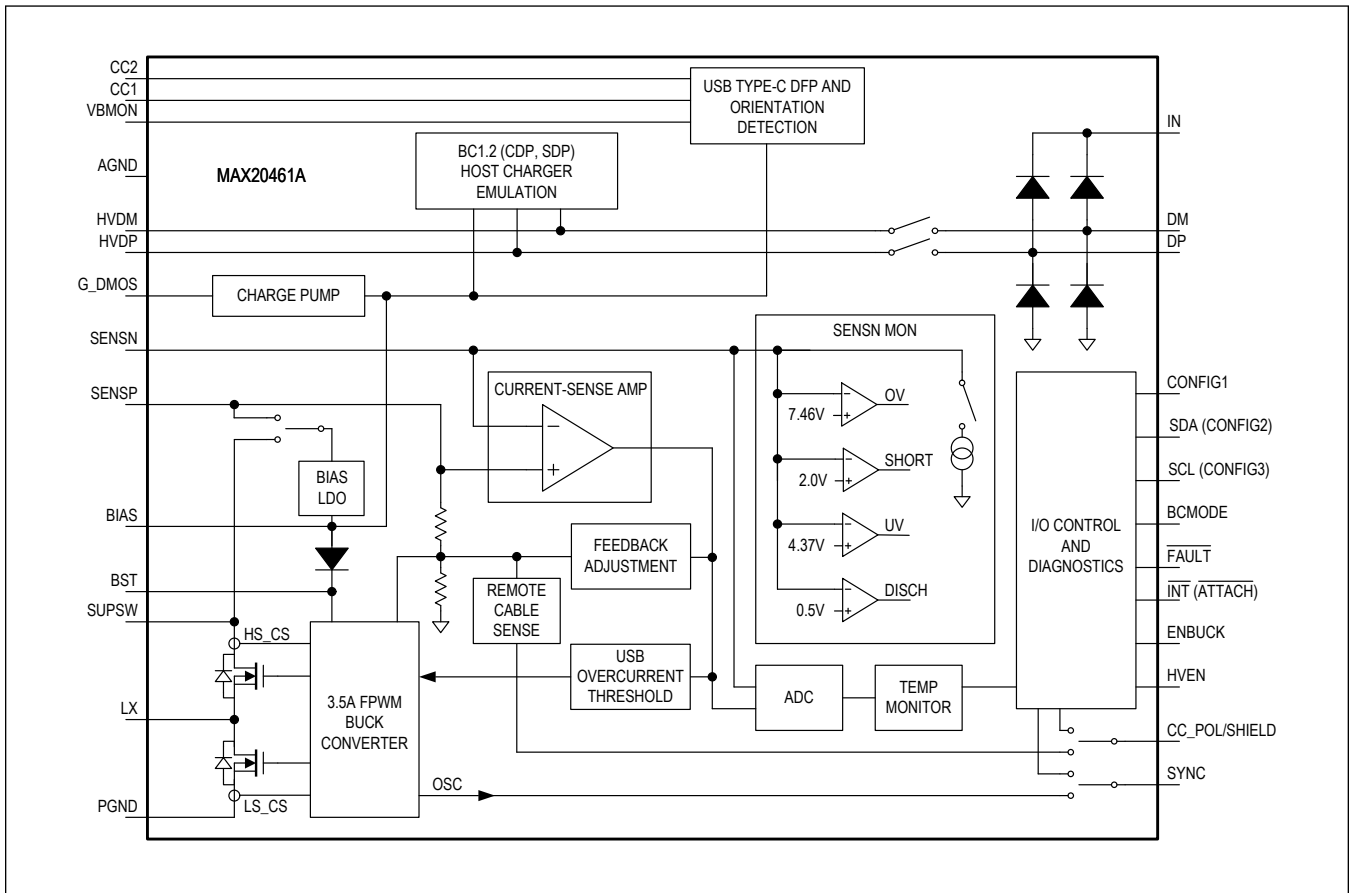
**Cable Attach-Detach and SENSN Discharge Timing Diagram**





Detailed Block Diagram





## Detailed Description

The MAX20461 combines a 5V/3A automotive-grade step-down converter, a USB host charger emulator, and USB protection switches. The device variants offer options for both standalone/GPIO and I<sup>2</sup>C configuration and control. This device family is designed for high-power USB ports in automotive radio, navigation, connectivity, USB hub, and dedicated charging applications.

The MAX20461 features high-voltage, high-ESD, 1GHz bandwidth data switches. MAX20461 protects up to 18V and includes internal ESD protection circuitry.

The data switches of all device variants protect the sensitive 3.3V pins of the USB transceiver and support USB Low-Speed (1.5Mbps), Full-Speed (12Mbps) and Hi-Speed (480Mbps) communication modes. The internal host charger port-detection circuitry offers automatic sensing and conformance to multiple standards, including USB Type-C 3.0A/1.5A/0.5A and USB-IF BC1.2 CDP/SDP modes. All variants enable USB-IF OTG, Apple CarPlay, and Android Auto conformance, while retaining industry-leading protection features and automotive-grade robustness.

The high-efficiency step-down DC-DC converter operates with an input voltage up to 28V, and is protected from load dump transients up to 40V. The DC-DC converter can be programmed from 310kHz to 2.2MHz switching frequency, or synced to 248kHz to 2.2MHz switching frequency. The converter can deliver 3A of continuous current at 125°C.

The MAX20461 features a high-side current-sense amplifier and a programmable feedback-adjustment circuit that provides automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications. The precision current sense allows for an accurate DC output current limit that minimizes the solution component size and cost.

## USB Type-C

USB Type-C introduces a new connector, cable, and detection mechanism while maintaining backwards compatibility with the existing USB ecosystem. The small-form-factor Type-C connector is reversible and bidirectional, which eliminates the Type A/Type B distinction. To maintain the USB host/device relationship, Type-C requires a configuration channel (CC). The CC pins are used to advertise and detect current capabilities and for the host to detect the cable orientation, which is required for USB3 and active cables.

A Type-C implementation supports, but does not require, USB Power Delivery, BC1.2, and USB3. For backwards compatibility, a USB3 implementation also requires an independent USB 2.0 channel. It is also advisable to implement BC1.2 detection, in addition to CC detection, on HVDP/HVDM. This ensures the highest possible charge current when a legacy adapter is used. [Table 1](#) shows the precedence of power negotiation as mandated by USB-IF. See USB Type-C 2.0 for details.

The MAX20461 provides an integrated Type-C 5V solution tailored to the automotive market. The device integrates all control and power circuitry necessary to maintain a 5V/3A downstream facing port (DFP) at the end of a captive-cable. It also provides BC1.2 charge detection, USB 2.0 data protection, and support for USB3 cable orientation detection and V<sub>CONN</sub> power.

**Table 1. Charge Detection Precedence**

PRECEDENCE	MODE OF OPERATION		NOMINAL VOLTAGE	MAXIMUM CURRENT
Highest ↓ Lowest	USB Type-C @ 3A Advertisement		5V	3A
	USB Type-C @ 1.5A Advertisement		5V	1.5A
	USB BC1.2		5V	≤ 1.5A
	Default USB Power	USB 3.1	5V	900 mA
		USB 2.0	5V	500 mA

## Configuration Channel (CC1 and CC2)

The CC pins utilize combinations of pullups and pulldowns to detect Type-C device attachment, advertise the current capabilities of the source, and detect the type and orientation of the cable and the device. There are three possible pullup resistors (R<sub>P</sub>) that represent the three source current capabilities: 0.5A, 1.5A, and 3A. There are also two possible device pulldown resistors (R<sub>A</sub> and R<sub>D</sub>) to provide device and cable information to the host. [Figure 1](#) shows how these are used

for Type-C detection on the CC pins. This configuration allows for simultaneous advertisement and detection. The Type-C specification also allows for dynamic  $R_P$  changes without any resets. [Table 2](#), [Table 3](#) and [Cable Attach-Detach and SENSEN Discharge Timing Diagram](#) detail how the MAX20461 responds to the various combinations of  $R_A$  and  $R_D$ .

**Table 2. CC Pulldown Response**

CC1	CC2	TYPE-C STATUS	MAX20461 ACTION TAKEN				
			VBUS	VCONN	CC_ATTACH	CC_POL	CC_PIN_STATE
Open	Open	Nothing attached	Off	Off	0	0	0b00
$R_D$	Open	Sink attached	On	Off	1	1	0b01
Open	$R_D$		On	Off	1	0	0b10
Open	$R_A$	Powered cable without Sink attached	Off	Off	0	0	0b00
$R_A$	Open		Off	Off	0	0	0b00
$R_D$	$R_A$	Powered cable with Sink attached	On	On CC2	1	1	0b01
$R_A$	$R_D$		On	On CC1	1	0	0b10
$R_D$	$R_D$	Debug Accessory attached	Off	Off	0	0	0b00
$R_A$	$R_A$	Audio Adapter Accessory attached	Off	Off	0	0	0b00

**Table 3. CC Pulldown Response (MAX20461A)**

CC1	CC2	TYPE-C STATUS	MAX20461A ACTION TAKEN			
			VBUS	CC_ATTACH	CC_POL	CC_PIN_STATE
Open	Open	Nothing attached	Off	0	0	0b00
$R_D$	Open	Sink attached	On	1	1	0b01
Open	$R_D$		On	1	0	0b10
Open	$R_A$	Powered cable without Sink attached	Off	0	0	0b00
$R_A$	Open		Off	0	0	0b00
$R_D$	$R_A$	Powered cable with Sink attached	On	1	1	0b01
$R_A$	$R_D$		On	1	0	0b10
$R_D$	$R_D$	Debug Accessory attached	Off	0	0	0b00
$R_A$	$R_A$	Audio Adapter Accessory attached	Off	0	0	0b00

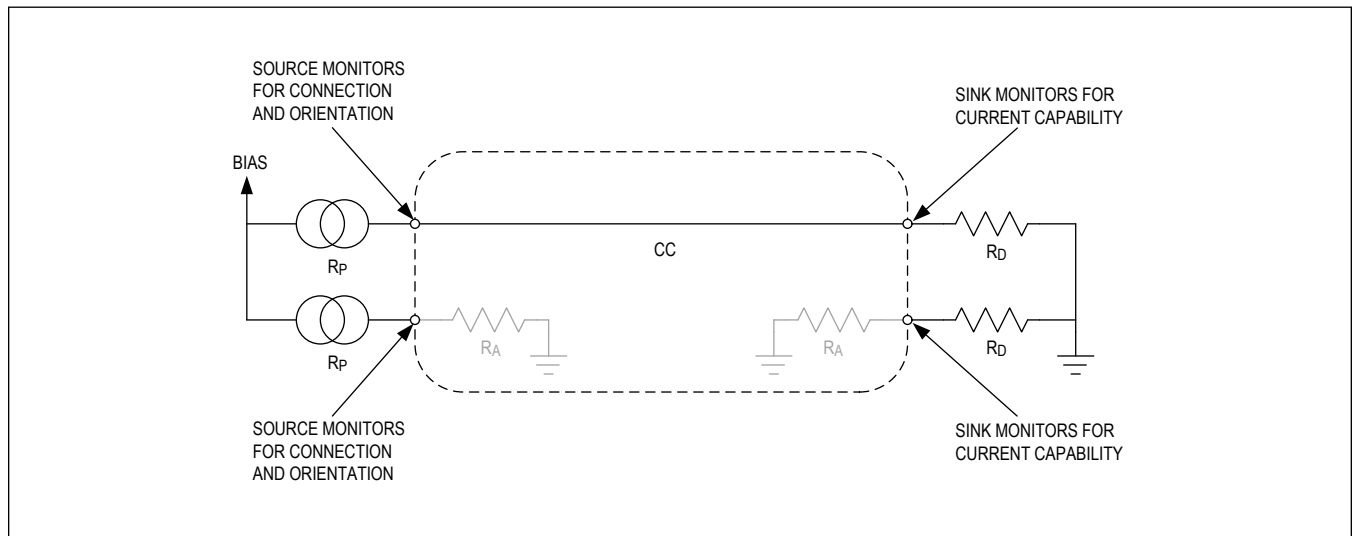


Figure 1. Type-C Pullup Model

**CC Polarity Output Pin (CC\_POL)**

The MAX20461 features an open-drain, active-low CC polarity output. The pin will assert low when  $R_D$  is detected on CC2. See [Table 2](#).

**V<sub>CONN</sub> (MAX20461 Only)**

While there are two CC pins that must be monitored on the host receptacle, there is only one CC wire running through the Type-C cable. This allows orientation to be determined, and leaves the second CC pin available for other uses. The Type-C specification allows the unused CC pin to operate as  $V_{CONN}$ , which is a low power source intended to power active cables that can include authentication ICs or superspeed muxes.

The MAX20461 includes complete support for  $V_{CONN}$  power control and protection. When a power source within the acceptable operating voltage is connected to the  $V_{CONN}$  pin, MAX20461 can connect the voltage source to the appropriate CC pin. Back-to-back  $V_{CONN}$  FETs provide overvoltage and overcurrent protection to the  $V_{CONN}$  source in addition to controlling the application of  $V_{CONN}$  per the Type-C specification.

**Table 4. Type-C Source  $V_{CONN}$  Requirements**

PORT FEATURES			$V_{CONN}$ REQUIREMENTS
D+/D-	SSTX/SSRX, VPD	>3A	
No	No	No	Not required
Yes	No	No	Not required
Yes	Yes	No	1W, 3V-5.5V

**V<sub>BUS</sub>**

Type-C includes new requirements for  $V_{BUS}$ , even when operating exclusively in 5V mode. When no device is attached to the CC pins, the host must switch the  $V_{BUS}$  source off so that near zero volts is present at the receptacle pin. To achieve this, the MAX20461 disables the external FET gate drive and turns off the buck converter when in a detached state, reducing quiescent current. The MAX20461 integrates control and discharge circuits to ensure all Type-C timing requirements are met. Throughout this document, the term  $V_{BUS}$  is used loosely to refer to voltage at SENSEP, SENSEN or VBMON. When more precision is required, the specific pin name is referenced.

**External FET Gate Drive (G\_DMOS Pin)**

The MAX20461 includes a gate drive for an optional external FET that can be used to isolate the bulk capacitance when  $V_{BUS}$  is not being sourced. If used, connect the G\_DMOS pin to the gate of the external FET. If not used, terminate G\_DMOS with a 10pF capacitor. G\_DMOS activates prior to soft-start, and turns off after discharge. If  $V_{BUS}$  short-to-battery is required, the FET should be appropriately rated. The external DMOS device must be a 20V  $V_{GS}$  type. The charge pump generates at least 7V.

**Legacy Devices**

The Type-C specification ensures interoperability with Type-A and Type-B devices by defining requirements for legacy adapters. As a DFP, relevant adapters connect from the Type-C receptacle to either a Type-B plug or to a Type-A receptacle, which can then be used with any legacy Type-A cable. A compliant legacy adapter of this type must include an  $R_D$  termination inside the adapter. In this case, the MAX20461 detects a Type-C attachment whenever the adapter is connected, regardless of whether a portable device is connected. The portable device sees the DFP as a BC1.2 port (when configured as such).

**Power-Up and Enabling****System Enable (HVEN)**

HVEN is used as the main enable to the device and initiates system start-up and configuration. If HVEN is at a logic-low level, SUPSW power consumption is reduced and the device enters a standby, low quiescent current level. HVEN is compatible with inputs from 3.3V logic up to automotive battery. After a system reset (e.g., HVEN toggle, BIAS UV), the I<sup>2</sup>C variant asserts the  $\overline{INT}$  pin to indicate that the IC has not been configured. The buck converter is forced off until the CONFIGURED bit of SETUP\_4 is written to a 1. This ensures that a portable device cannot attach before the IC registers

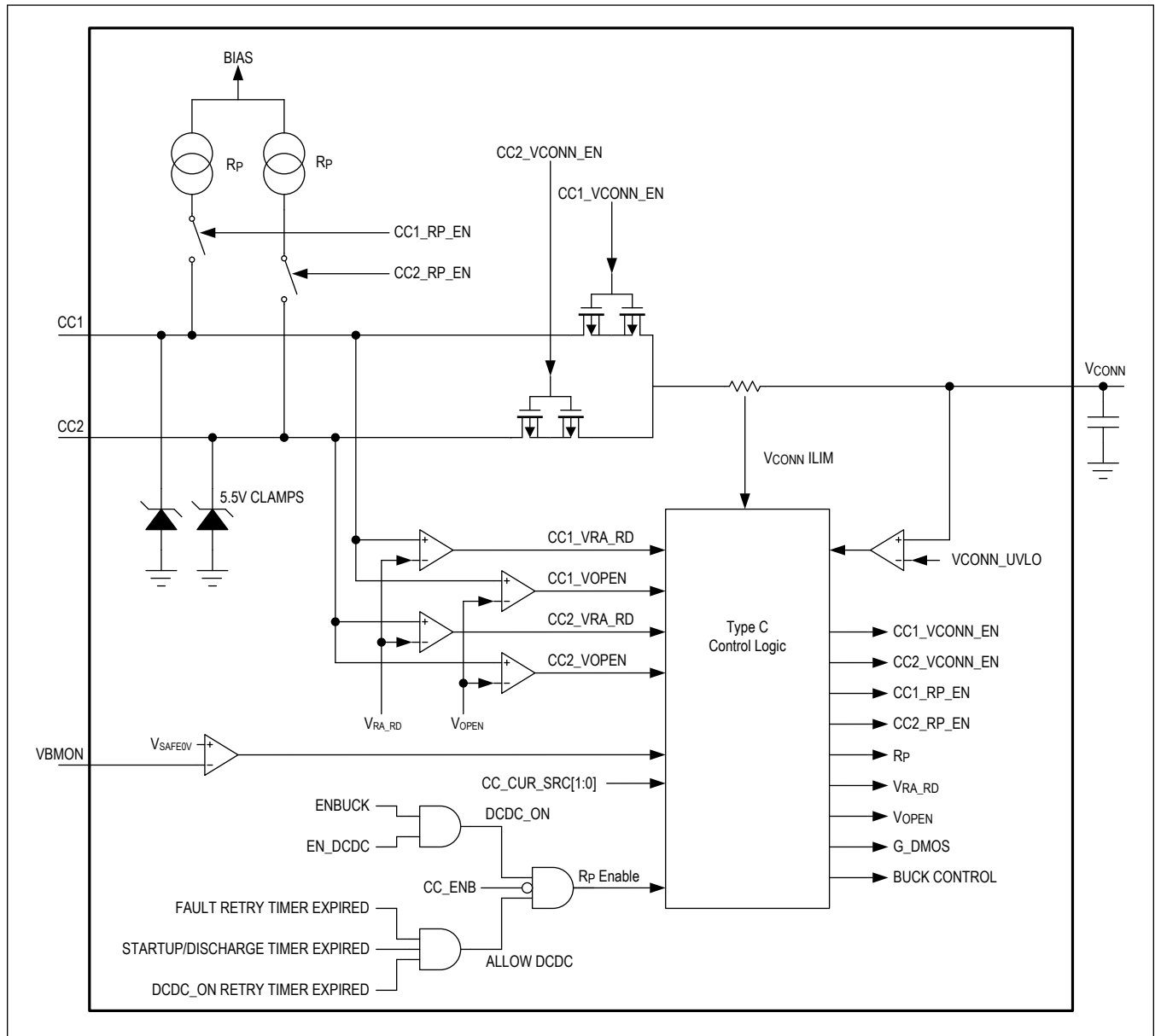


Figure 2. USB Type-C Block Diagram

are correctly set for the application.

**DC-DC Enable (ENBUCK)**

The buck regulator on the MAX20461 is controlled by the ENBUCK pin for standalone variants, and by both the ENBUCK pin and the I<sup>2</sup>C interface for I<sup>2</sup>C variants. DCDC\_ON, the logical AND of ENBUCK and EN\_DCDC, determines if the buck converter can be enabled by the Type-C control logic. On standalone variants, EN\_DCDC is always high and only ENBUCK can be used to enable the buck converter. On I<sup>2</sup>C variants, setting ENBUCK low overrides an I<sup>2</sup>C EN\_DCDC enable command, which allows compatibility with USB hub controllers. For a typical USB hub application, connect ENBUCK to the enable output of the USB hub controller. This allows the USB hub controller to enable and disable the USB power port using software commands. ENBUCK can be directly connected to the BIAS or IN pin for applications

that do not require GPIO control of the DC-DC converter enable.

### 3.3V Input (IN)

IN is used to clamp the D+ and D- pins during an ESD or overvoltage event on the HVD+ and HVD- pins. This clamping protects the downstream USB transceiver. The presence of these clamping diodes requires that IN remain set to 3.3V at all times for USB communication to occur. The IN pin features an overvoltage lockout that disables the data switches if IN is above  $V_{IN\_OVLO}$ . Bypass IN with a 1 $\mu$ F ceramic capacitor, place it close to the IN pin, and connect it to the same 3.3V supply that is shared with the multimedia processor or hub transceiver.

### Linear Regulator Output (BIAS)

BIAS is the output of a 5V linear regulator that powers the internal logic and control circuitry for the device. BIAS is internally powered from SUPSW or SENSP and automatically powers up when HVEN is high and SUPSW voltage exceeds  $V_{UV\_SUPSW}$ . The BIAS output contains an undervoltage lockout that keeps the internal circuitry disabled when BIAS is below  $V_{UV\_BIAS}$ . The linear regulator automatically powers down when HVEN is low, and a low shutdown current mode is entered. Bypass BIAS to GND with a 2.2 $\mu$ F ceramic capacitor.

### Power-On Sequencing

HVEN, ENBUCK and IN do not have a power-up sequence requirement by design. However, the desired system behavior should be considered for the state of these pins at startup. The D+ and D- pins are clamped to IN, therefore IN should be set to 3.3V before any USB communication is required. It is recommended that IN is set to 3.3V before HVEN is set high. ENBUCK acts as the master disable for the DC-DC converter. If ENBUCK is low when HVEN is set high, all variants keep the buck converter in the disabled state until ENBUCK is set high.

## Step-Down DC-DC Regulator

### Step-Down Regulator

The MAX20461 features a current-mode, step-down converter with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency, forced-PWM operation under light loads. The DC-DC regulator features a cycle-by-cycle current limit and intelligent transition from skip mode to forced-PWM mode that makes the device ideal for automotive applications.

### Wide Input Voltage Range

The device is specified for a wide 4.5V to 28V input voltage range. SUPSW provides power to the internal BIAS linear regulator and internal power switch. Certain conditions such as cold cranking can cause the voltage at the output to drop below the programmed output voltage. Under such conditions, the device operates in a high duty-cycle mode to facilitate minimum dropout from input to output.

### Maximum Duty-Cycle Operation

The MAX20461 has a maximum duty cycle of 98% (typ). The IC monitors the off-time (time for which the low-side FET is on) in both PWM and skip modes for every switching cycle. Once the off-time of 150ns (typ) is detected continuously for 7.5 $\mu$ s, the low-side FET is forced on for 60ns (typ) every 7.5 $\mu$ s. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and design efficiency. The input voltage at which the devices enter dropout can be approximated as:

$$V_{SUPSW} = \frac{V_{OUT} + (I_{LOAD} \times R_{ONH})}{0.98}$$

Note: The equation above does not take into account the efficiency and switching frequency but will provide a good first-order approximation. Use the  $R_{ONH}$  (max) in the [Electrical Characteristics](#) table.

### Output Voltage (SENSP)

The device features a precision internal feedback network that is connected to SENSP and that is used to set the output voltage of the DC-DC converter. The network nominally sets the average DC-DC converter output voltage to the voltage that corresponds to the  $V_{OUT}$  configuration register, with a default value of 5.15V.

### Soft-Start

When the DC-DC converter is enabled, the regulator soft-starts by gradually ramping up the output voltage from 0V to 5.15V over approximately 8ms. This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads (see the [USB Loads](#) section).

### Reset Behavior

The MAX20461 implements a discharge function on SENS\_N any time that the DC-DC regulator is disabled for any reason. When the discharge function is activated, current ( $I_{\text{SENS\_DIS}}$ ) is drained through a current-limited FET, and a reset timer is also started. This timer prevents the DC-DC regulator from starting up again until the timer has expired. This allows for easy compatibility with USB specifications and removes the need for long discharge algorithms to be implemented in system software. See the relevant [Functional Diagrams](#) and [Figure 2](#) for reset timer details.

### Reset Criteria

The MAX20461 DC-DC converter automatically resets for all undervoltage, overvoltage, overcurrent and overtemperature fault conditions. See [Table 12](#) for details. The fault retry timer is configurable in the SETUP\_3 register. This timer is activated after a fault condition is removed and prevents the buck converter from switching on until the timer expires.

Another internal retry timer is enabled after DCDC\_ON is set low or a Type-C detach event. DCDC\_ON toggle causes buck shutdown and prevent the buck from switching on until  $t_{\text{BUCKOFF\_CD}}$  expires. A Type-C detach event will cause buck shutdown and prevent the buck from switching on until  $t_{\text{BUCKOFF\_DET}}$  expires.

### Switching Frequency Configuration

The DC-DC switching frequency can be referenced to an internal oscillator or from an external clock signal on the SYNC pin. The internal oscillator frequency is set by the FSW[2:0] bits of the SETUP\_1 register, which has a POR value corresponding to 2.2MHz. The internal oscillator can be programmed via I<sup>2</sup>C to eight discrete values from 310kHz to 2.2MHz. For standalone variants, FSW configuration value is loaded from the CONFIG1 pin at startup with four discrete values from 310kHz to 2.2MHz available.

### Switching Frequency Synchronization (SYNC Pin)

When the SYNC pin is configured to operate as an output, skip mode operation is disallowed, and the internal oscillator drives the SYNC pin. This allows other devices to synchronize with the MAX20461 180 degrees out of phase for EMI reduction.

When SYNC is configured as an input, the SYNC pin becomes a logic-level input that can be used for both operating-mode selection and frequency control. Connecting SYNC to GND or an external clock enables fixed-frequency, forced-PWM mode. Connecting SYNC to a logic-high signal allows intelligent skip-mode operation (Type-A mode, i.e. CC\_ENB = 1) or FPWM mode (default Type-C mode, i.e. CC\_ENB = 0). The device can be externally synchronized to frequencies within  $\pm 20\%$  of the programmed internal oscillator frequency.

### Forced-PWM Operation

In forced-PWM mode, the device maintains fixed-frequency PWM operation over all load conditions, including no-load conditions.

### Intelligent Skip-Mode Operation and Attach Detection

When the SYNC pin is configured as an input and CC\_ENB = 1 (via I<sup>2</sup>C only), but neither a clocked signal nor a logic-low level exists on the SYNC pin, the MAX20461 operates in skip mode at very light load/no load conditions. Intelligent device attach detection is used to determine when a device is attached to the USB port. The device intelligently exits skip mode and enters forced-PWM mode when a device is attached and remains in forced-PWM mode as long as the attach signal persists. This minimizes the EMI concerns caused by automotive captive USB cables and poorly shielded consumer USB cables. The device attach event is also signaled by the ATTACH pin (standalone variants) or ATTACH bits (I<sup>2</sup>C variants). The criteria for device attach detection and intelligent skip-mode operation are shown in [Table 5](#). Note that when operating in Type-C mode, the buck only switches on when a Type-C device is attached. This means skip mode cannot be entered if CC\_ENB = 0.



**Table 5. DC-DC Converter Intelligent Skip Mode Truth Table**

CC_ENB	SYNC PIN	SYNC DIR BIT	DATA SWITCH CHARGE DETECTION MODE	CDP ATTACH DETECTION	CURRENT SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
0	x	x	x	x	x	Forced-PWM Mode: Type-C Device Attached
1	x	1	x	x	x	Forced-PWM Mode: Continuous
1	0	0	x	x	x	Forced-PWM Mode: Continuous
1	Clocked	0	x	x	x	Forced-PWM Mode: Continuous
1	1	0	High-Speed Pass Thru (SDP) Mode	x	0	Intelligent Skip Mode: No Device Attached
1	1	0	High-Speed Pass Thru (SDP) Mode	x	1	Forced-PWM Mode: Device Attached
1	1	0	BC1.2 Auto CDP Mode	0	0	Intelligent Skip Mode: No Device Attached
1	1	0	BC1.2 Auto CDP Mode	1	x	Forced-PWM Mode: Device Attached
1	1	0	BC1.2 Auto CDP Mode	x	1	Forced-PWM Mode: Device Attached

### Spread-Spectrum Option

Spread-spectrum operation is offered to improve the EMI performance of the MAX20461. Spread-spectrum operation is enabled by the SS\_EN bit of the SETUP\_0 register, which is preloaded on startup from the CONFIG1 pin for both standalone and I<sup>2</sup>C variants. The internal operating frequency modulates the switching frequency by up to  $\pm 3.4\%$  relative to the internally generated operating frequency. This results in a total spread-spectrum range of 6.8%. Spread-spectrum mode is only active when operating from the internal oscillator. Spread-spectrum clock dithering is not possible when operating from an external clock.

### Current Limit

The MAX20461 limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter, as well as a user-programmable external DC load current-sense amplifier threshold. This allows the current limit to be adjusted between 300mA to 3A depending on the application requirements, while protecting the system in the event of a fault. Upon exceeding either the DC-DC peak or user-programmable current thresholds, the high-side FET is immediately switched off and current-limit algorithms are initiated. When the external current limit lasts for longer than 16ms, the FAULT pin asserts and the VBUS\_ILIM bit of the IRQ\_1 register is set. Once the load current exceeds the programmed threshold, the DC-DC converter acts as a constant-current source. This may cause the output voltage to droop. The ILIM\_ITRIP bit of the SETUP\_2 register determines the output voltage droop required to initiate a DC-DC converter reset during VBUS\_ILIM. When ILIM\_ITRIP = 0, the USB current limit is detected for 16ms and the output voltage falls below  $V_{UV\_SENSN}$ ; the DC-DC converter resets. The DC-DC converter also resets if the internal LX peak current threshold is exceeded for four consecutive switching cycles and the output voltage droops to less than 2.0V.

In some cases, the designer may want to increase the load to 160%, refer to [USB Output Current Limit](#) for details.

### Output Short-Circuit Protection

The DC-DC converter output (SENSP, SENSN) is protected against both short-to-ground and short-to-battery conditions. If a short-to-ground or undervoltage condition is encountered, the DC-DC converter immediately resets, asserts the FAULT pin, flags the fault in the IRQ\_1 register, and then reattempts soft-start after the reset delay. This pattern repeats until the short circuit has been removed.

If a short-to-battery is encountered ( $V_{SENSN} > V_{OV\_SENSN}$ ), the buck converter shuts down, G\_DMOS is disabled, the FAULT pin is asserted, and the fault is flagged in the IRQ\_1 register. The buck converter stays shut down until the fault

condition resolves and the 2s timer expires.

### Thermal Overload Protection

Thermal overload protection limits the total power dissipated by the device. A thermal-protection circuit monitors the die temperature. If the die temperature exceeds +165°C, the device shuts down, so it can cool. Once the device has cooled by 10°C, the device is enabled again. This results in a pulsed output during continuous thermal overload conditions, protecting the device during fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. See the Thermal Considerations section for more information.

### Pre-Thermal Overload Warning

The MAX20461 I<sup>2</sup>C variant features a thermal overload warning flag which sets the THM\_WARN bit of the IRQ\_2 register when the die temperature crosses +140°C. This allows a system software implementation of thermal foldback or load shedding algorithms to prevent a thermal overload condition.

### Automatic Thermal Foldback

All MAX20461 variants implement a thermal foldback feature which, when enabled, reduces the Type-C current advertised on the CC pins by R<sub>P</sub>. When THM\_WARN = 1, the R<sub>P</sub> current advertisement reduces to the setting immediately below what is set in CC\_CUR\_SRC[1:0]. When the die temperature drops below the thermal warning threshold, R<sub>P</sub> returns to its original setting based on CC\_SRC\_CUR[1:0].

Note that Type-C allows for dynamic R<sub>P</sub> changes in the Attached.SRC state without reinitializing detection. The MAX20461 thermal foldback does not: force BUS to reset, change the BC1.2 mode, or reduce the USB current limit. Alternative thermal foldback algorithms are available and can be performed in system software. Contact Maxim Applications for support.

## USB Current Limit and Output Voltage Adjustment

### Current-Sense Amplifier (SENSP, SENSN)

MAX20461 features an internal USB load current-sense amplifier to monitor the DC load current delivered to the USB port. The V<sub>SENSE</sub> voltage (V<sub>SENSP</sub> - V<sub>SENSN</sub>) is used internally to provide precision DC current-limit and voltage-compensation functionality. A 33mΩ sense resistor (R<sub>SENSE</sub>) should be placed between SENSP and SENSN.

In some cases, the designer may want to increase the load to 160%, refer to [USB Output Current Limit](#) for details.

### USB DC Current Limit Configuration

The MAX20461 allows configuration of the precision DC current limit by the ILIM[2:0] bits of the SETUP\_2 register. I<sup>2</sup>C configuration enables selection of eight discrete DC current limit values. See SETUP\_2 for current limit configuration values.

Standalone variants of the device allow selection of a subset of the eight available current limit options by reading the CONFIG3 resistor. See [Table 10](#) and the [Applications Information](#) section for more information.

In some cases, the designer may want to increase the load to 160%, refer to [USB Output Current Limit](#) for details.

### Voltage Feedback Adjustment Configuration

The MAX20461 compensates voltage drop for up to 474mΩ of USB cable in typical USB charging applications. I<sup>2</sup>C variants of the device allow this configuration by the GAIN[4:0] bits of the SETUP\_1 register. See GAIN[4:0] for voltage gain configuration. Standalone variants of the device allow configuration by the CONFIG2 resistor, which sets GAIN[3:0], and the CONFIG3 resistor, which sets GAIN[4]. See the SETUP\_1 register map and the [Applications Information](#) section for more information.

In some cases, the designer may want to increase the load to 160%, refer to [USB Output Current Limit](#) for details.

### Remote Sense Feedback Adjustment

The remote-sense feature (available by custom order only) provides another option to adjust the output voltage by sensing the ground node on the USB port at the far-end of the captive cable; either with the cable shield or with an additional sensing wire. This feature automatically senses the cable resistance and adjusts the voltage compensation

without changing the GAIN[4:0] setting.

The user needs to compensate the voltage drop because of the sense resistor, the load line behavior of the buck, and any difference between the V<sub>BUS</sub> and GND conductors. See [Figure 3](#) and contact the factory for support and how to order.

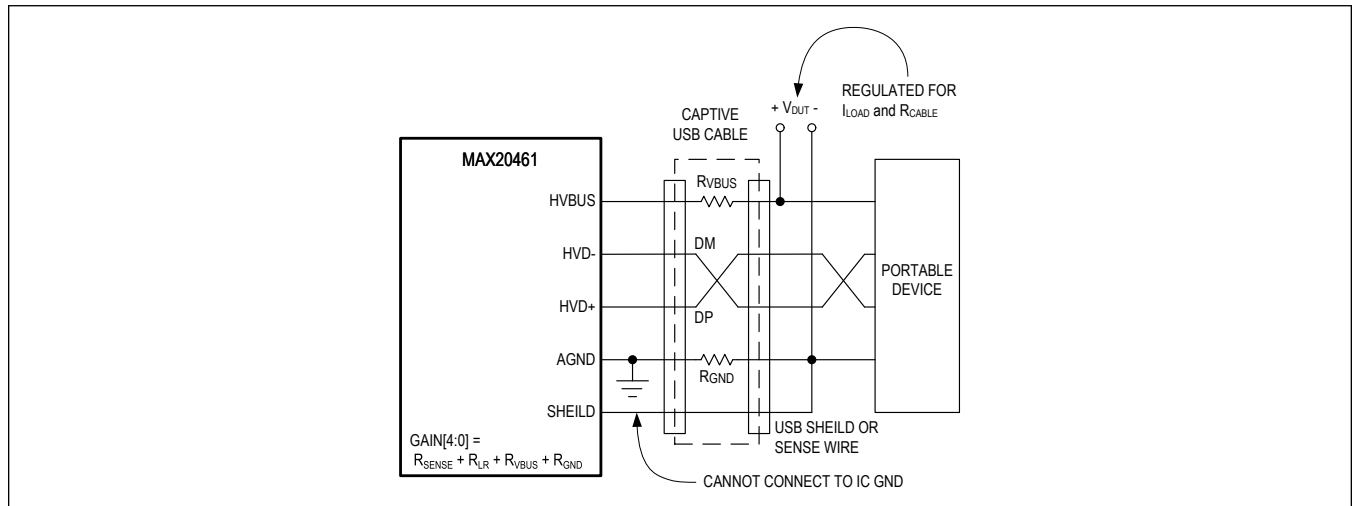


Figure 3. Remote Cable-Sense Diagram

**High Voltage Modes Configuration**

I<sup>2</sup>C variants of the MAX20461 allow high output voltage mode configurations for flexible use in higher power charging applications, and for load-dump protected battery pass-through output to automotive modules. Contact factory for support.

**USB Protection Switches and BC1.2 Host Charger Emulation**

**USB Protection Switches**

MAX20461 provides automotive-grade ESD and short-circuit protection for the low-voltage USB data lines of high-integration multimedia processors. HVDP/HVDM protection consists of ESD and OVP (overvoltage protection) for 1.5Mbps, 12Mbps, and 480Mbps USB transceiver applications. This is accomplished with a very low-capacitance FET in series with the D+ and D- data path.

The MAX20461 does not require an external ESD array, and protects the HVD+ and HVD- pins to ±15kV Air-Gap/±8kV Contact Discharge with the 150pF/330Ω IEC 61000-4-2 model and the 330pF/330Ω model, as well as protecting up to ±25kV Air-Gap/±8kV Contact Discharge with the 330pF/2kΩ ISO 10605 model. The MAX20461 provides robust, automotive-grade protection while maintaining a 1GHz -3dB insertion loss. This ensures optimum eye diagram at the end of a captive cable.

The HVD+ and HVD- short-circuit protection features include protection for a short to the USB +5V BUS and a short to the +18V car battery. These protection features prevent damage to the low-voltage USB transceiver when shorts occur in the vehicle harness or customer USB connector/cable. Short-to-GND protection is provided by the upstream USB transceiver.

**USB Host Charger Emulator**

The USB protection switches integrate the latest USB-IF Battery Charging Specification Revision 1.2 CDP and SDP circuitry.

**Table 6. Data Switch Mode Truth Table (I<sup>2</sup>C Variants)**

PART NUMBER	DEVICE INPUTS	SA	SB	DATA SWITCH MODE
-------------	---------------	----	----	------------------

**Table 6. Data Switch Mode Truth Table (I<sup>2</sup>C Variants) (continued)**

	HVEN	IN	CD[1]	CD[0]	BCMODE			
MAX20461ATJA, MAX20461AATJA, MAX20461AATJM	0	X	X	X	X	0	0	Off
	1	0	X	X	1	Invalid Mode (IN = 3.3V required for all modes)		
	1	0	0	X	0	Invalid Mode (IN = 3.3V required for all modes)		
	1	1	0	0	0	1	0	Hi-Speed Pass-Through (SDP)
	1	1	0	1	0	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)
	1	1	X	X	1	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)

**Table 7. Data Switch Mode Truth Table (Standalone Variants)**

PART NUMBER	DEVICE INPUTS			SA	SB	DATA SWITCH MODE
	HVEN	IN	BCMODE			
MAX20461ATJD, MAX20461AATJD, MAX20461AATJP	0	X	X	0	0	Off
	1	0	X	Invalid Mode (IN = 3.3V required for all modes)		
	1	1	0	1	0	Hi-Speed Pass-Through (SDP)
	1	1	1	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)

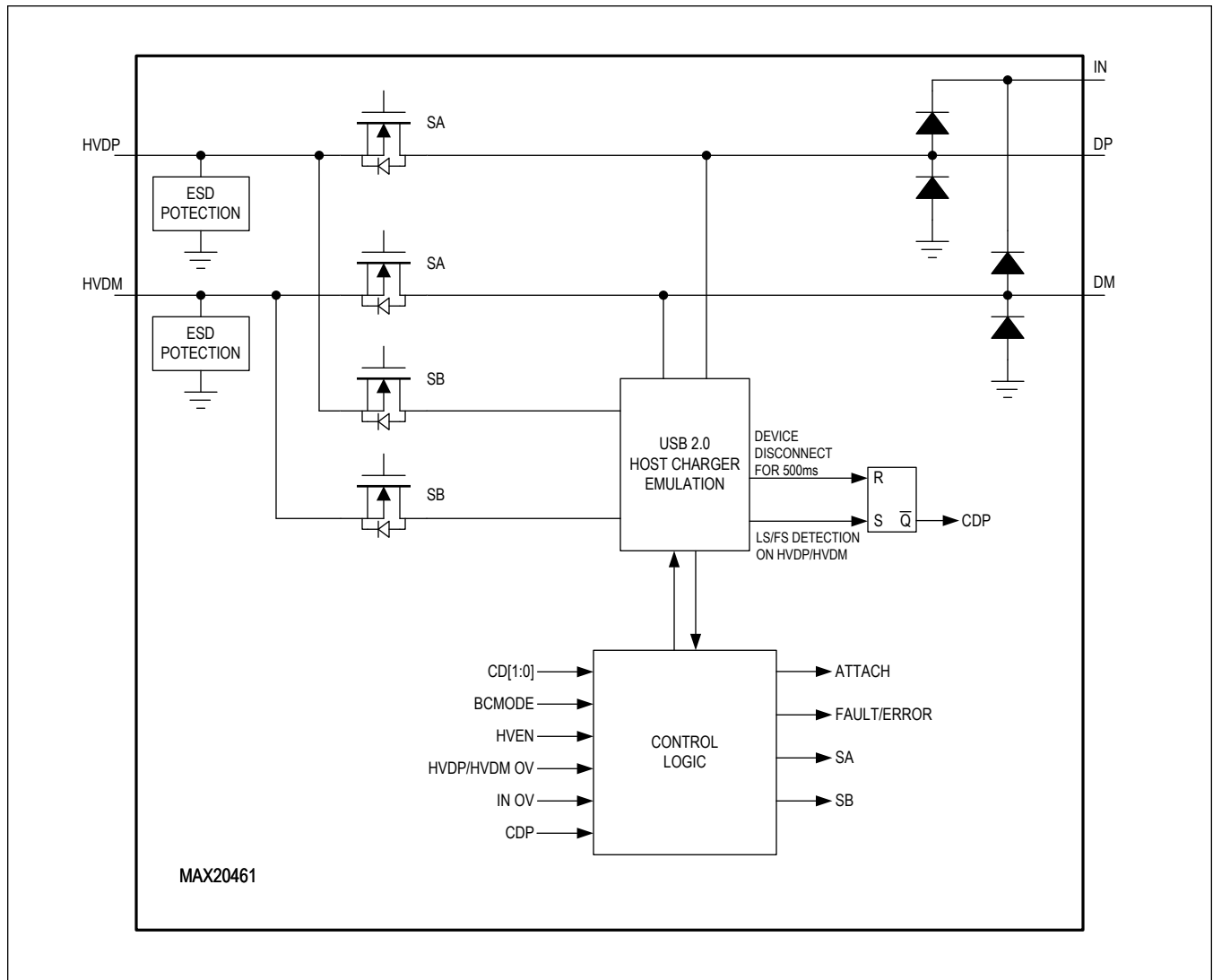


Figure 4. Data Switch and Charge-Detection Block Diagram

**USB On-The-Go and Dual-Role Applications**

The MAX20461 is fully compatible with USB on-the-go (OTG) and dual-role applications. A negotiated role swap (HNP or Apple CarPlay) requires no software interaction with the IC. When there is no negotiation before the SOC enters peripheral mode, the MAX20461 must be in Hi-Speed pass-through (SDP mode) before and during the role swap. All variants default to SDP mode on startup if the BCMODE pin is logic-low. This configuration allows a role swap immediately on startup without microcontroller interaction.

**I<sup>2</sup>C, Control, and Diagnostics**

**I<sup>2</sup>C Configuration (CONFIG1 and I<sup>2</sup>C)**

The MAX20461 I<sup>2</sup>C variants allow basic device configuration through a resistor placed to GND on the CONFIG1 pin. The configuration parameters correlating to the chosen resistor are pre-loaded into their respective I<sup>2</sup>C registers on startup when HVEN is toggled high. After startup, the user is free to change the affected I<sup>2</sup>C registers as desired.

For I<sup>2</sup>C variants, CONFIG1 sets the startup value of the DC-DC spread-spectrum enable bit SS\_EN and the SYNC

direction control bit SYNC\_DIR. CONFIG1 also sets the LSBs of the I<sup>2</sup>C slave address. The configuration table for the I<sup>2</sup>C variant CONFIG table is shown in [Table 8](#).

**Table 8. CONFIG1 Pin Table (I<sup>2</sup>C Version)**

RESISTANCE (Ω, typ)	STEP	SS_EN	SYNC_DIR	I <sup>2</sup> C_ADDR LSBs
Short to GND	0	1 (ON)	1 (IN)	00
619	1	1 (ON)	1 (IN)	01
976	2	1 (ON)	1 (IN)	10
1370	3	1 (ON)	1 (IN)	11
1820	4	1 (ON)	0 (OUT)	00
2370	5	1 (ON)	0 (OUT)	01
3090	6	1 (ON)	0 (OUT)	10
3920	7	1 (ON)	0 (OUT)	11
4990	8	0 (OFF)	1 (IN)	00
6340	9	0 (OFF)	1 (IN)	01
8250	10	0 (OFF)	1 (IN)	10
11000	11	0 (OFF)	1 (IN)	11
15400	12	0 (OFF)	0 (OUT)	00
23700	13	0 (OFF)	0 (OUT)	01
44200	14	0 (OFF)	0 (OUT)	10
Short to BIAS (or R > 71.5kΩ)	15	0 (OFF)	0 (OUT)	11

### Standalone Configuration (CONFIG1–CONFIG3)

The MAX20461 standalone variants allow full device configuration from three resistors placed among the three CONFIG pins and GND. For standalone variants, SDA and SCL serve as CONFIG2 and CONFIG3, respectively.

CONFIG1 sets the internal oscillator switching frequency, SYNC pin direction, and DC-DC spread spectrum mode. CONFIG2 sets the 4 LSBs of the voltage adjustment gain (GAIN[3:0]). CONFIG3 sets the USB DC current limit, type-C current advertisement, automatic thermal foldback, and MSB of voltage adjustment gain (GAIN[4]). See tables below for standalone variant CONFIG options. See the [Applications Information](#) section for setting selection and [Ordering Information](#) for variant part number information.

In some cases, the designer may want to increase the load to 160%, refer to [USB Output Current Limit](#) for details.

**Table 9. CONFIG1 Pin Table (Standalone Variants)**

RESISTANCE (Ω, typ)	STEP	SS_EN	SYNC_DIR	FSW (kHz)
Short to GND	0	ON	IN	2200
619	1	ON	IN	488
976	2	ON	IN	350
1370	3	ON	IN	310
1820	4	ON	OUT	2200
2370	5	ON	OUT	488
3090	6	ON	OUT	350
3920	7	ON	OUT	310
4990	8	OFF	IN	2200
6340	9	OFF	IN	488
8250	10	OFF	IN	350

**Table 9. CONFIG1 Pin Table (Standalone Variants) (continued)**

RESISTANCE ( $\Omega$ , typ)	STEP	SS_EN	SYNC_DIR	FSW (kHz)
11000	11	OFF	IN	310
15400	12	OFF	OUT	2200
23700	13	OFF	OUT	488
44200	14	OFF	OUT	350
Short to BIAS (or $R > 71.5k\Omega$ )	15	OFF	OUT	310

**Table 10. CONFIG2 and CONFIG3 Pin Table (Standalone Variants)**

RESISTANCE ( $\Omega$ , typ)	STEP	CONFIG2		CONFIG3		
		GAIN[3:0]	THM_FLDBK_EN	GAIN[4]	CURRENT LIMIT ILIM_SET (A)	TYPE-C MODE CC_SRC_CUR (A)
Short to GND	0	0b0000	ON	0	0.55	0.5
619	1	0b0001	ON	0	1.62	1.5
976	2	0b0010	ON	0	2.60	1.5
1370	3	0b0011	ON	0	3.04	3.0
1820	4	0b0100	ON	1	0.55	0.5
2370	5	0b0101	ON	1	1.62	1.5
3090	6	0b0110	ON	1	2.60	1.5
3920	7	0b0111	ON	1	3.04	3.0
4990	8	0b1000	OFF	0	0.55	0.5
6340	9	0b1001	OFF	0	1.62	1.5
8250	10	0b1010	OFF	0	2.60	1.5
11000	11	0b1011	OFF	0	3.04	3.0
15400	12	0b1100	OFF	1	0.55	0.5
23700	13	0b1101	OFF	1	1.62	1.5
44200	14	0b1110	OFF	1	2.60	1.5
Short to BIAS (or $R > 71.5k\Omega$ )	15	0b1111	OFF	1	3.04	3.0

### I<sup>2</sup>C Diagnostics and Event Handling

The I<sup>2</sup>C-based diagnostic functionality is independent of the  $\overline{\text{FAULT}}$  pin. Setting the IRQMASK bit for a specific fault condition does not mask the  $\overline{\text{FAULT}}$  pin for the respective fault. IRQMASK register functionality affects only the behavior of the  $\overline{\text{INT}}$  pin. This allows the  $\overline{\text{FAULT}}$  pin to be tied to over-current fault input of a hub controller or SoC, while the I<sup>2</sup>C interface is simultaneously used by the system software for advanced diagnostic functionality.

### Interrupt and Attach Output ( $\overline{\text{INT}}(\overline{\text{ATTACH}})$ )

The MAX20461  $\overline{\text{INT}}(\overline{\text{ATTACH}})$  pin functions as an interrupt ( $\overline{\text{INT}}$ ) for I<sup>2</sup>C variants. The  $\overline{\text{INT}}$  pin asserts an interrupt based on the configuration of the IRQ\_MASK\_0, IRQ\_MASK\_1, and IRQ\_MASK\_2 registers. Interrupt configuration allows the  $\overline{\text{INT}}$  pin to assert any of the featured fault detection, as well as on device attachment, and USB voltage/current ADC conversion completion. The  $\overline{\text{INT}}$  pin only asserts while a masked IRQ bit is asserted, which means its behavior is also dependent on the AUTOCLR bit.

Standalone variants of the MAX20461 feature an open-drain, active-low,  $\overline{\text{ATTACH}}$  output that serves as the attach detection pin. For standalone variants, the  $\overline{\text{ATTACH}}$  pin can be used for GPIO input to a microprocessor, or to drive an LED for attach/charge indication.

The  $\overline{\text{INT}}(\overline{\text{ATTACH}})$  assertion logic is shown in [ATTACH Logic Diagram](#).

### I<sup>2</sup>C Output Voltage and Current Measurement

The MAX20461 I<sup>2</sup>C variant allows measurement of the instantaneous SENSE voltage, DC output current, and die temperature using an integrated ADC. To initiate a measurement, set the ADC\_REQ bit of the ADC\_REQUEST register. The ADC\_REQ bit is cleared by the IC once the measurement is complete and the ADC samples are available. Additionally, the ADC\_DONE bit of the IRQ\_0 register will be set when the sample is available. ADC\_DONE can be masked to assert an interrupt when the sample is ready.

The sampled measurements can be read from the ADC\_USBV, ADC\_USBI, and ADC\_TEMP registers. The new sample persists in the register until another sample request is initiated by setting the ADC\_REQ bit.

All measurements provide 8 bits of resolution. The measured SENSE voltage has a range of 0V to 19.8V. Convert the sample to a voltage as follows

$$V_{SENSE} = \frac{19.8V}{255} \cdot \text{ADC\_USBV (Volts)}.$$

The measured SENSE voltage has a range from 0 to 128.5mV. Convert the sample to a current as follows

$$I_{LOAD} = \frac{128.5mV}{255} \cdot \frac{\text{ADC\_USBI}}{R_{SENSE}} \text{ (Amps)}.$$

The measured die temp has a range from -40°C to 170°C and a temperature resolution of 3.5°C. Convert the sample to a die temperature by  $T_J = 3.5^\circ\text{C} \cdot \text{ADC\_TEMP} - 270$  (°C).

### I<sup>2</sup>C Interface

The MAX20461 features an I<sup>2</sup>C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX20461 and the master at clock rates up to 400kHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. [Figure 5](#) shows the 2-wire interface timing diagram.

A master device communicates to the MAX20461 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse. The MAX20461 SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus.

The MAX20461 SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

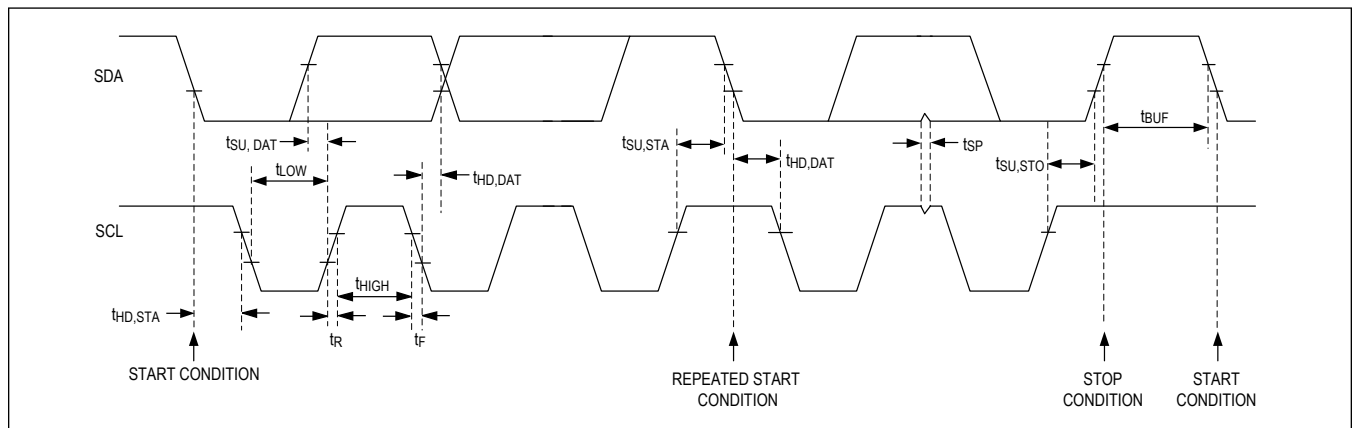


Figure 5. I<sup>2</sup>C Timing Diagram

### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the



SCL pulse. Changes in SDA while SCL is high are considered control signals (see the STOP and START Conditions section). SDA and SCL idle high when the I<sup>2</sup>C bus is not busy.

### STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 6). A START (S) condition from the master signals the beginning of a transmission to the MAX20461. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

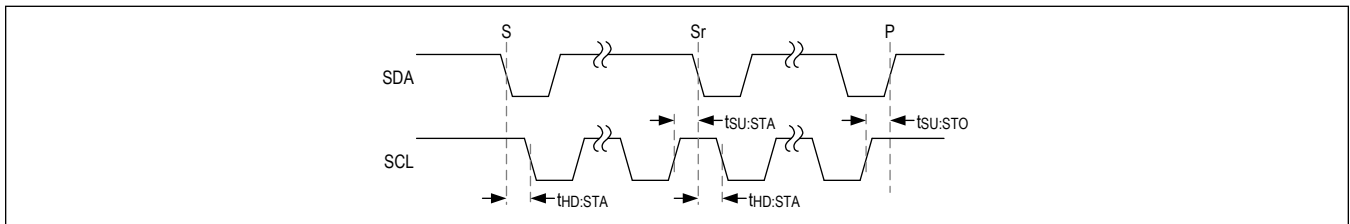


Figure 6. START, STOP and REPEATED START Conditions

### Early STOP Condition

The MAX20461 recognizes a STOP condition at any point during data transmission, unless the STOP condition occurs in the same high pulse as a START condition.

### Clock Stretching

In general the clock signal generation for the I<sup>2</sup>C bus is the responsibility of the master device. The I<sup>2</sup>C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX20461 does not use any form of clock stretching to hold down the clock line.

### I<sup>2</sup>C General Call Address

The MAX20461 does not implement the I<sup>2</sup>C specifications general call address. If the MAX20461 sees the general call address (0b0000\_0000), it does not issue an acknowledge.

### I<sup>2</sup>C Slave Addressing

Once the device is enabled, the I<sup>2</sup>C slave address is set by the CONFIG1 pin.

The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to 1 to configure the device to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Table 11. I<sup>2</sup>C Slave Addresses

CONFIG1 CODE	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
0b00	0	1	1	0	0	0	0	0x30	0x60	0x61
0b01	0	1	1	0	0	0	1	0x31	0x62	0x63
0b10	0	1	1	0	0	1	0	0x32	0x64	0x65
0b11	0	1	1	0	0	1	1	0x33	0x66	0x67

### Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 7). The device pulls down SDA during the master generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event

of an unsuccessful data transfer, the bus master can reattempt communication.

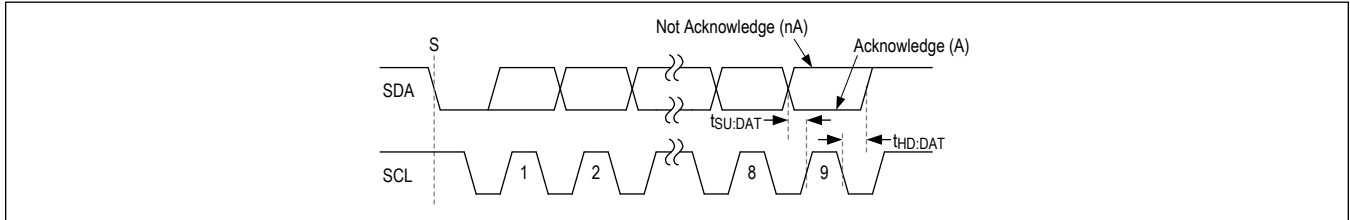


Figure 7. Acknowledge Condition

**Write Data Format**

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to a register address, one byte of data to the command register, and a STOP condition. [Figure 8](#) illustrates the proper format for one frame.

**Read Data Format**

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data from a register address, restart condition, the slave address with read bit set to 1, one byte of data to the command register, and a STOP condition. [Figure 8](#) illustrates the proper format for one frame.

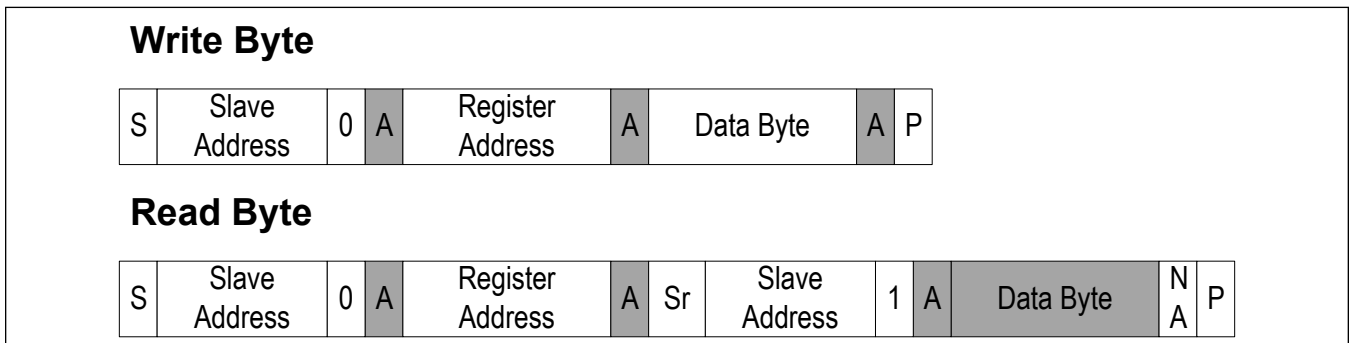


Figure 8. Data Format of I<sup>2</sup>C Interface

**Fault Detection and Diagnostics**

**Fault Detection**

The MAX20461 features advanced device protection features with automatic fault handling and recovery. [Table 12](#) summarizes the conditions that generate a fault, and the actions taken by the device. For all variants, the  $\overline{\text{FAULT}}$  output remains asserted as long as a fault condition persists.

For I<sup>2</sup>C variants, the IRQ registers provide detailed information on the source of the fault condition, and the IRQMASK registers allow selection of the criteria for assertion of the I<sup>2</sup>C Interrupt pin,  $\overline{\text{INT}}$ . The IRQ register bits clear when read. However, the IRQ bits that represent a present fault condition continue to reassert after they are cleared, so long as the fault condition persists. If the IRQMASK registers are configured to assert  $\overline{\text{INT}}$  for a present fault, the  $\overline{\text{INT}}$  pin deasserts when the IRQ register that asserted the interrupt is read. The  $\overline{\text{INT}}$  pin subsequently reasserts if the fault condition persists.

**Fault Output Pin ( $\overline{\text{FAULT}}$ )**

The MAX20461 features an open-drain, active-low  $\overline{\text{FAULT}}$  output. The MAX20461 is designed to eliminate false  $\overline{\text{FAULT}}$  reporting by using an internal deglitch and fault blanking timer. This ensures  $\overline{\text{FAULT}}$  is not incorrectly asserted during normal operation such as starting into high-capacitance loads. The  $\overline{\text{FAULT}}$  pin can be tied directly to the over-current

fault input of a hub controller or SoC.

**Table 12. Fault Conditions**

EVENT	IRQ REGISTER BITS (I <sup>2</sup> C ONLY)	DEBOUNCE PRIOR TO ACTION	ACTION TAKEN
Thermal Shutdown	THM_SHD	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and disable $R_P$ . When fault resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin, enable $R_P$ and the DC-DC converter.
Thermal Warning/ Foldback	THM_WARN	20 ms	Assert associated IRQ bit and reduce Type-C $R_P$ by one step. When fault resolves and REPLY_TMR expires, reset Type-C to CC_SRC_CUR.
IN Overvoltage	IN_OV	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, disable $R_P$ , and reset BC1.2. When fault resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin, close data switches, enable $R_P$ and the DC-DC converter.
HVDP/ HVDM Overvoltage	DATA_OV	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, disable $R_P$ , and reset BC1.2. When fault resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin, close data switches, enable $R_P$ and the DC-DC converter.
USB DC Overcurrent	VBUS_ILIM	16 ms	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit after overcurrent condition persists for 16ms. When overcurrent resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin.
USB DC Overcurrent and SENSN < 4.38V	VBUS_ILIM_UV	16 ms	ILIM_ITRIP = 0: Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, and disable $R_P$ after overcurrent and undervoltage condition persists for 16ms. Release $\overline{\text{FAULT}}$ pin, enable $R_P$ and DC-DC converter once REPLY_TMR expires after shutdown.  I <sup>2</sup> C variant and ILIM_ITRIP = 1: Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit after overcurrent condition persists for 16ms. When overcurrent resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin.
SENSN < 4.38V	VBUS_UV	16 ms	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit after undervoltage condition persists for 16ms. When undervoltage resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin.
USB DC Overcurrent and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and disable $R_P$ . Release $\overline{\text{FAULT}}$ pin, enable $R_P$ and DC-DC converter once REPLY_TMR expires after shutdown.
LX Overcurrent for 4 Consecutive Cycles and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and disable $R_P$ . Release $\overline{\text{FAULT}}$ pin, enable $R_P$ and DC-DC converter once REPLY_TMR expires after shutdown.
SENSN Overvoltage	VBUS_OV	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and disable $R_P$ . When fault resolves and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin, enable $R_P$ , DC-DC converter, and data switches.
V <sub>CONN</sub> Overcurrent	VCONN_ILIM	1 ms	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, open V <sub>CONN</sub> FET. After overcurrent no longer exists and REPLY_TMR expires, release $\overline{\text{FAULT}}$ pin. V <sub>CONN</sub> can only be re-enabled by passing through the unattached state.
V <sub>BUS</sub> Pre-on Overvoltage	VBUS_PRE_OV	16 ms	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit after overvoltage condition persists for 16ms. After overvoltage no longer exists and REPLY_TMR has expired, release $\overline{\text{FAULT}}$ pin.

## Register Map

## Summary Table

ADDRESS	NAME	MSB							LSB
<b>USER_CMDS</b>									
0x00	<a href="#">SETUP_0[7:0]</a>	-	THM_FL DBK_EN	EN_DCD C	VOUT[2:0]			SYNC_D IR	SS_EN
0x01	<a href="#">SETUP_1[7:0]</a>	FSW[2:0]			GAIN[4:0]				
0x02	<a href="#">SETUP_2[7:0]</a>	-	-	-	ILIM_ITR IP	-	ILIM[2:0]		
0x03	<a href="#">SETUP_3[7:0]</a>	RETRY_TMR[1:0]		CD[1:0]		CC_ENB	CC_VCO NN_EN	CC_SRC_CUR[1:0]	
0x04	<a href="#">SETUP_4[7:0]</a>	-	-	-	-	-	-	-	CONFIG URED
0x05	<a href="#">ADC_REQUEST[7:0]</a>	-	-	-	-	-	-	-	ADC_RE Q
0x06	<a href="#">CC_REQUEST[7:0]</a>	-	-	-	-	-	-	CC_FOR CE_ERR	CC_SRC _RST
0x07	<a href="#">IRQ_MASK_0[7:0]</a>	IRQ_AU TOCLR	-	EN_CC_ STATE_ EV	EN_CC_ ATTACH_ IRQ	EN_BC_ ATTACH_ IRQ	EN_CC_ ATTACH_ EV	EN_BC_ ATTACH_ EV	EN_ADC_ DONE
0x08	<a href="#">IRQ_MASK_1[7:0]</a>	-	EN_VBU S_PRE_ OV	EN_VBU S_ILIM_ UV	EN_VBU S_ILIM	EN_VBU S_OV	EN_VBU S_UV	EN_VBU S_SHT_ GND	EN_THM_ SHD
0x09	<a href="#">IRQ_MASK_2[7:0]</a>	-	-	EN_VBU S_PREB IAS	EN_VCO NN_ERR	EN_THM_ _WARN	EN_IN_ OV	EN_DAT A_OV	EN_VCO NN_ILIM
0x0A	<a href="#">IRQ_0[7:0]</a>	UNCON FIGURE D	-	CC_STA TE_EV	CC_ATT ACH_IR Q	BC_ATT ACH_IR Q	CC_ATT ACH_EV	BC_ATT ACH_EV	ADC_DO NE
0x0B	<a href="#">IRQ_1[7:0]</a>	-	VBUS_P RE_OV	VBUS_IL IM_UV	VBUS_IL IM	VBUS_O V	VBUS_U V	VBUS_S HT_GND	THM_SH D
0x0C	<a href="#">IRQ_2[7:0]</a>	-	-	VBUS_P REBIAS	VCONN_ ERR	THM_W ARN	IN_OV	DATA_O V	VCONN_ ILIM
0x0D	<a href="#">STATUS_0[7:0]</a>	-	-	-	CC_ATT ACH	BC_ATT ACH	VBMON _SAFE	VCONN_ READY	VBUS_S TAT
0x0E	<a href="#">STATUS_1[7:0]</a>	-	-	CC_PIN_STATE[1:0]		CC_STATE[3:0]			
0x10	<a href="#">ADC_0[7:0]</a>	ADC_USBI[7:0]							
0x11	<a href="#">ADC_1[7:0]</a>	ADC_USBV[7:0]							
0x12	<a href="#">ADC_2[7:0]</a>	ADC_TEMP[7:0]							

## Register Details

[SETUP\\_0 \(0x0\)](#)

BIT	7	6	5	4	3	2	1	0
Field	–	THM_FLDBK K_EN	EN_DCDC	VOUT[2:0]			SYNC_DIR	SS_EN
Reset	–	0b0	0b1	0b000				
Access Type	–	Write, Read	Write, Read	Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
THM_FLDBK _EN	6	Lowers the Type-C advertised current capability when thermal warning is tripped.	0 = Disable Thermal Foldback 1 = Enable Thermal Foldback
EN_DCDC	5	DC/DC Converter Enable. Internally AND'ed with the ENBUCK pin.	0 = Disable V <sub>BUS</sub> Buck Converter 1 = Enable V <sub>BUS</sub> Buck Converter
VOUT	4:2	V <sub>BUS</sub> Output Level Selection	0b000 = 5V 0b001 = 9V 0b010 = 12V 0b011 = 15V 0b100 = 18V (protected battery pass-through) 0b101 = 5V 0b110 = 5V 0b111 = 5V
SYNC_DIR	1	SYNC Pin Direction Selection Initial value set by CONFIG1 resistor.	0 = Output 1 = Input
SS_EN	0	Spread Spectrum Enable Initial value set by CONFIG1 resistor.	0 = Disable Spread Spectrum Function 1 = Enable Spread Spectrum Function

**SETUP\_1 (0x1)**

BIT	7	6	5	4	3	2	1	0
Field	FSW[2:0]			GAIN[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FSW	7:5	DC/DC Converter Switching Frequency Selection	0b000 = 2200 kHz 0b001 = 1200 kHz 0b010 = 790 kHz 0b011 = 600 kHz 0b100 = 488 kHz 0b101 = 410 kHz 0b110 = 350 kHz 0b111 = 310 kHz

BITFIELD	BITS	DESCRIPTION	DECODE
GAIN	4:0	The gain of the voltage correction applied to the buck converter output (based on DC load sensed by current sense amp). $R_{SENSE} = 33m\Omega$ .	0: 0m $\Omega$ 1: 18m $\Omega$ 2: 36m $\Omega$ 3: 54m $\Omega$ 4: 72m $\Omega$ 5: 90m $\Omega$ 6: 108m $\Omega$ 7: 126m $\Omega$ 8: 144m $\Omega$ 9: 162m $\Omega$ 10: 180m $\Omega$ 11: 198m $\Omega$ 12: 216m $\Omega$ 13: 234m $\Omega$ 14: 252m $\Omega$ 15: 270m $\Omega$ 16: 288m $\Omega$ 17: 306m $\Omega$ 18: 324m $\Omega$ 19: 342m $\Omega$ 20: 360m $\Omega$ 21: 378m $\Omega$ 22: 396m $\Omega$ 23: 414m $\Omega$ 24: 432m $\Omega$ 25: 450m $\Omega$ 26: 468m $\Omega$ 27: 486m $\Omega$ 28: 504m $\Omega$ 29: 522m $\Omega$ 30: 540m $\Omega$ 31: 558m $\Omega$

**SETUP 2 (0x2)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	ILIM_ITRIP	-	ILIM[2:0]		
Reset	-	-	-	0b0	-	0b111		
Access Type	-	-	-	Write, Read	-	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM_ITRIP	4	Determines the buck's retry behavior under USB DC current limit conditions.	0 = VBUS_ILIM_UV fault enabled. 1 = VBUS_ILIM_UV fault disabled.
ILIM	2:0	USB DC Current-Limit Threshold, $R_{SENSE} = 33m\Omega$ .	USB DC Current-Limit Threshold (min in Amps) 0b000 = 0.3 0b001 = 0.55 0b010 = 0.8 0b011 = 1.05 0b100 = 1.62 0b101 = 2.1 0b110 = 2.6 0b111 = 3.04

**SETUP 3 (0x3)**

BIT	7	6	5	4	3	2	1	0
Field	RETRY_TMR[1:0]		CD[1:0]		CC_ENB	CC_VCONN_EN	CC_SRC_CUR[1:0]	
Reset	0b00				0b0	0b1	0b01	
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_TMR	7:6	Determines the length of the RETRY timer after a fault condition.	0b00 = 2.0s 0b01 = 1.0s 0b10 = 0.5s 0b11 = 16ms
CD	5:4	BC1.2 Charge Detection Configuration Selection.  This register is pre-loaded based on the part number variant and the status of the BCMODE pin.	0b00 = High Speed Pass Through (SDP) 0b01 = Auto-CDP 0b10 = Reserved 0b11 = Reserved
CC_ENB	3	Disable Type-C Detection	0 = Enable 1 = Disable
CC_VCONN_EN	2	MAX20461A: Not Used  MAX20461: Enable V <sub>CONN</sub> pass-through	0 = Disable V <sub>CONN</sub> pass-through. 1 = Enable V <sub>CONN</sub> pass-through.
CC_SRC_CUR	1:0	Type-C DFP source pullup current advertisement (R <sub>p</sub> )	00 = 0.5A 01 = 1.5A 10 = 3.0A 11 = 0.5A

**SETUP 4 (0x4)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CONFIGURED
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONFIGURED	0	I <sup>2</sup> C configuration complete indicator  Upon power-up, the buck converter is prevented from turning on until this bit is written to a one, indicating the part is fully configured for its intended mode of operation.	0 = I <sup>2</sup> C Configuration Pending 1 = I <sup>2</sup> C Configuration Complete

**ADC\_REQUEST (0x5)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ADC_REQ
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_REQ	0	ADC V/I Sample Request  When a one is written, ADC V/I sampling is initiated. This bit is cleared once the requested sampling is complete and the ADC results are updated. The status of the ADC conversion (data ready) can be monitored in the IRQ0 register.	0 = No ADC Sample Requested 1 = ADC Sample Requested

**CC\_REQUEST (0x6)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	CC_FORCE_ERR	CC_SRC_RST
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_FORCE_ERR	1	Type-C Force Error Request  This is a request bit (write-only). Forces the Type-C state machine to go through error recovery. This bit will always read back zero.	0 = No change to current operating state. 1 = Force transition to error recovery state.
CC_SRC_RST	0	Type-C Force Source Reset Request  This is a request bit (write-only). The Type-C state machine will be forced back to the UnAttached.SRC state, restarting Type-C detection. This bit will always read back zero.	0 = No change to current operating state 1 = Force transition to UnAttached.SRC state

**IRQ\_MASK\_0 (0x7)**

A Read-Write register that configures which of the conditions in the IRQ\_0 register will assert an Interrupt. See the IRQ\_0 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	IRQ_AUTO CLR	–	EN_CC_STATE_EV	EN_CC_ATTACH_IRQ	EN_BC_ATTACH_IRQ	EN_CC_ATTACH_EV	EN_BC_ATTACH_EV	EN_ADC_DONE
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_AUTOC CLR	7	IRQ Auto Clear	0 = IRQ register flags are latched on until read. 1 = IRQ register flags are automatically cleared when the error condition is removed.
EN_CC_STATE_EV	5	CC_STATE Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_CC_ATTACH_IRQ	4	Type-C ATTACH STATUS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_BC_ATTACH_IRQ	3	BC1.2 ATTACH STATUS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt



BITFIELD	BITS	DESCRIPTION	DECODE
EN_CC_ATT ACH_EV	2	Type-C ATTACH EVENT Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_BC_ATT ACH_EV	1	BC1.2 ATTACH EVENT Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_ADC_D ONE	0	ADC_DONE Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

**IRQ\_MASK\_1 (0x8)**

A Read-Write register that configures which of the conditions in the IRQ\_1 register will assert an Interrupt. See the IRQ\_1 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	EN_VBUS_ PRE_OV	EN_VBUS_I LIM_UV	EN_VBUS_I LIM	EN_VBUS_ OV	EN_VBUS_ UV	EN_VBUS_ SHT_GND	EN_THM_S HD
Reset	–	0x0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBUS_P RE_OV	6	VBUS_PRE_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_IL IM_UV	5	VBUS_ILIM_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_IL IM	4	VBUS_ILIM Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_O V	3	VBUS_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_U V	2	VBUS_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_S HT_GND	1	VBUS_SHT_GND Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_THM_SH D	0	THM_SHD Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

**IRQ\_MASK\_2 (0x9)**

A Read-Write register that configures which of the conditions in the IRQ\_2 register will assert an Interrupt. See the IRQ\_2 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_VBUS_ PREBIAS	EN_VCON N_ERR	EN_THM_ WARN	EN_IN_OV	EN_DATA_ OV	EN_VCON N_ILIM
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBUS_P REBIAS	5	VBUS_PREBIAS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VCONN_ERR	4	MAX20461A: Not Used MAX20461: VCONN_ERR Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_THM_WARN	3	THM_WARN Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_IN_OV	2	IN_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_DATA_OV	1	DATA_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VCONN_ILIM	0	MAX20461A: Not Used MAX20461: VCONN_ILIM Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

**IRQ\_0 (0xA)**

A read only register that includes flags which indicate a number of operating conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

IRQ\_0 holds notifications of expected operations rather than error/fault conditions.

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	UNCONFIGURED	–	CC_STATE_EV	CC_ATTACH_IRQ	BC_ATTACH_IRQ	CC_ATTACH_EV	BC_ATTACH_EV	ADC_DONE
<b>Reset</b>	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Clears All	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
UNCONFIGURED	7	I <sup>2</sup> C Unconfigured Indicator Bit	0 = Device is fully configured (CONFIGURED written to 1) 1 = Device is not fully configured (CONFIGURED has not been written to 1)
CC_STATE_EV	5	Type-C State Change Indicator Clear on Read. Not affected by IRQ_AUTOCLR.	0 = No change in Type-C state since last read 1 = Type-C state has changed since last read
CC_ATTACH_IRQ	4	Type-C ATTACH Indicator This bit indicates a Type-C device attach is observed via the CC Pins. Applies to Attached.SRC states. Further attach details can be read in the STATUS registers.	0 = No Type-C device attached 1 = Type-C device attached
BC_ATTACH_IRQ	3	BC1.2 ATTACH Indicator This bit indicates a BC1.2 device attach is observed via the HVDP/HVDM pins.	0 = No device attached 1 = Device attached

BITFIELD	BITS	DESCRIPTION	DECODE
CC_ATTACH_EV	2	Type-C ATTACH Event Detected  This bit indicates a Type-C device attach was initiated and/or terminated as observed via the CC Pins. This bit differs from CC_ATTACH (which indicates the current Type-C attach status in real time) in that it is issued only when the status changes from unattached to attached or vice-versa.  Clear on Read. Not affected by IRQ_AUTOCLR.	0 = No attach or detach event detected since least read 1 = New attach and/or detach event detected
BC_ATTACH_EV	1	BC1.2 ATTACH Event Detected  This bit indicates a BC1.2 device attach was initiated and/or terminated as observed via the HVDP/HVDM pins. This bit differs from BC_ATTACH (which indicates the current BC1.2 attach status in real time) in that it is issued only when the status changes from unattached to attached or vice-versa.  Clear on Read. Not affected by IRQ_AUTOCLR.	0 = No attach or detach event detected since least read 1 = New attach and/or detach event detected
ADC_DONE	0	ADC Measurement Complete Indicator. Clear on Read.	0 = No new data available since least read 1 = New data available

**IRQ\_1 (0xB)**

A read only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	VBUS_PRE_OV	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_PRE_OV	6	VBUS Pre-Overvoltage Fault Detected  Asserts if overvoltage exists on VBMON when Type-C is enabled and no Type-C device is attached.  Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_ILIM_UV	5	VBUS Current Limit and SENSN UV Fault Detected Disabled when ILIM_ITRIP = 1. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_ILIM	4	VBUS Current Limit Condition Detected Disabled when ILIM_ITRIP = 0. Clear on Read if condition is resolved.	0 = No event 1 = Event detected

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_OV	3	VBUS Overvoltage Fault Detected Detected on SENS pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_UV	2	VBUS Under Voltage Fault Detected Detected on SENS pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_SHT_GND	1	VBUS Short to Ground Fault Detected Detected on SENS pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
THM_SHD	0	Over Temperature Fault Detected Asserts when the die temperature exceeds 165°C (typ). Clear on Read if condition is resolved.	0 = No event 1 = Event detected

**IRQ\_2 (0xC)**

A read only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	VBUS_PRE BIAS	VCONN_E RR	THM_WAR N	IN_OV	DATA_OV	VCONN_ILI M
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_PREBIAS	5	VBUS Pre-Bias  Asserts if Type-C is enabled and VBMON > VSAFE0V when no Type-C device is attached.	0 = No event 1 = Event detected
VCONN_ERROR	4	MAX20461A: Not Used  MAX20461: VCONN input requested and the VCONN source is not within operating range.	0 = No event 1 = Event detected
THM_WARN	3	Thermal Warning Condition Detected Asserts when the temperature has reached 140°C (typ). If thermal foldback is enabled, the Type-C current advertisement is lowered one step while this bit is asserted. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
IN_OV	2	IN Pin Overvoltage Fault Detected Clear on Read if condition is resolved.	0 = No event 1 = Event detected
DATA_OV	1	DATA Pin Overvoltage Fault Detected Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VCONN_ILIM	0	MAX20461A: Not Used  MAX20461: VCONN Overcurrent Fault Detected The VCONN overcurrent monitor is only active when VCONN is being sourced to a CC pin. It is not active on the opposite CC pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected

**STATUS\_0 (0xD)**

A read only register that includes information on the current status of the IC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CC_ATTAC H	BC_ATTAC H	VBMON_S AFE	VCONN_R EADY	VBUS_STA T
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CC_ATTACH	4	Type-C ATTACH Status Indicator This bit indicates the current Type-C attach status via the CC pins. More details can be read in the STATUS_1 register.	0 = No Type-C device currently attached 1 = Type-C device currently attached
BC_ATTACH	3	BC1.2 ATTACH Status Indicator This bit indicates the current device attach status via the HVDP/HVDM pins. More details can be read in the STATUS_1 register.	0 = No device currently attached 1 = Device currently attached
VBMON_SAFE	2	VBMON (V <sub>BUS</sub> ) Safe Status Indicator Determines if the DC-DC converter can be turned on after a Type-C attach. Only applicable with Type-C enabled.	0 = V <sub>BUS</sub> > V <sub>SAFE0V</sub> 1 = V <sub>BUS</sub> < V <sub>SAFE0V</sub>
VCONN_READY	1	MAX20461A: Not Used  MAX20461: V <sub>CONN</sub> Detect Status Indicator Asserts when Type-C is enabled and a V <sub>CONN</sub> source is detected on the V <sub>CONN</sub> pin.	0 = V <sub>CONN</sub> not observed 1 = V <sub>CONN</sub> > V <sub>VCONN_DET</sub>
VBUS_STAT	0	Type-C V <sub>BUS</sub> Status Indicator	0 = V <sub>BUS</sub> not applied to receptacle 1 = V <sub>BUS</sub> applied to receptacle (Attached.SRC)

**STATUS\_1 (0xE)**

A read only register that includes information on the current status of the IC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	CC_PIN_STATE[1:0]		CC_STATE[3:0]			
Reset	–	–	0b00		0b0000			
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
CC_PIN_STATE	5:4	Type-C Active CC Pin/Orientation Indicator	0b00 = No Attach 0b01 = R <sub>D</sub> detected on CC1 0b10 = R <sub>D</sub> detected on CC2 0b11 = Not used
CC_STATE	3:0	Type-C Functional Status/State Indicator	0b0000 = Disabled 0b0010 = ErrorRecovery 0b0011 = Unattached.SRC 0b0110 = AttachWait.SRC 0b1000 = Attached.SRC (CC2) 0b1100 = Attached.SRC (CC1)

[ADC\\_0 \(0x10\)](#)

BIT	7	6	5	4	3	2	1	0
Field	ADC_USBI[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
ADC_USBI	7:0	USB Load Current ADC Measurement Result			$I_{LOAD} = ((128.5\text{mV}/255) * \text{ADC\_USBI})/R_{SENSE}$ (amperes)			

[ADC\\_1 \(0x11\)](#)

BIT	7	6	5	4	3	2	1	0
Field	ADC_USBV[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
ADC_USBV	7:0	USB Voltage ADC Measurement Result			$V_{SENSN} = (19.8\text{V}/255) * \text{ADC\_USBV}$ (volts), when $V_{OUT}[2:0] = 0b000$			

[ADC\\_2 \(0x12\)](#)

BIT	7	6	5	4	3	2	1	0
Field	ADC_TEMP[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
ADC_TEMP	7:0	Die Temp ADC Measurement Result			Die Temp = $3.5^{\circ}\text{C} * \text{ADC\_TEMP} - 270$ ( $^{\circ}\text{C}$ )			

## Applications Information

### DC-DC Switching Frequency Selection

The switching frequency ( $f_{SW}$ ) for MAX20461 is programmable via the CONFIG1 resistor (on standalone variants) or by I<sup>2</sup>C register writes.

Higher switching frequencies allow for smaller PCB area designs with lower inductor values and less output capacitance. Consequently, peak currents and I<sup>2</sup>R losses are lower at higher switching frequencies, but core losses, gate charge currents, and switching losses increase.

To avoid AM band interference, operation between 500kHz and 1.8MHz is not recommended.

### DC-DC Input Capacitor Selection

The input capacitor supplies the instantaneous current needs of the buck converter and reduces the peak currents drawn from the upstream power source. The input bypass capacitor is a determining factor in the input voltage ripple.

The input capacitor RMS current rating requirement ( $I_{IN(RMS)}$ ) is defined by the following equation:

$$I_{IN(RMS)} = I_{LOAD} \frac{\sqrt{V_{SENSP} \times (V_{SUPSW} - V_{SENSP})}}{V_{SUPSW}}$$

$I_{IN(RMS)}$  has a maximum value when the input voltage equals twice the output voltage ( $V_{SUPSW} = 2 \cdot V_{SENSP}$ ), so

$I_{IN(MAX)} = \frac{1}{2} \cdot I_{LOAD(MAX)}$ .  $I_{LOAD}$  is the measured operating load current, while  $I_{LOAD(MAX)}$  refers to the maximum load current.

Choose an input capacitor that exhibits less than 10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of  $V_Q$  (caused by the capacitor discharge) and  $V_{ESR}$  (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUPSW} - V_{SENSP}) \times V_{SENSP}}{V_{SUPSW} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ where } D = \frac{V_{SENSP}}{V_{SUPSW}}$$

Where D is the buck converter duty cycle.

Bypass SUPSW with 0.1µF parallel to 10µF of ceramic capacitance close to the SUPSW and PGND pins. The ceramic input capacitor of a buck converter has a high  $\frac{di}{dt}$ , minimize the PCB current-loop area to reduce EMI. Bypass SUPSW with 47µF of bulk electrolytic capacitance to dampen line transients.

### DC-DC Output Capacitor Selection

To ensure stability and compliance with the USB and Apple specifications, follow the recommended output filters listed in [Table 13](#). For proper functionality, a minimum amount of ceramic capacitance must be used regardless of  $f_{SW}$ . Additional capacitance for lower switching frequencies can be low-ESR electrolytic types (< 0.25Ω).

### DC-DC Output Inductor Selection

Three key inductor parameters must be considered when selecting an inductor: inductance value (L), inductor saturation current ( $I_{SAT}$ ), and DC resistance ( $R_{DCR}$ ). To select the proper inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected. A small LIR will reduce the RMS current in the output capacitor and results in small output ripple voltage, but this requires a larger inductor. A good compromise between size and loss is  $LIR = 0.35$  (35%). Determine the inductor value using the equation below,

$$L = \frac{V_{SENSP} \times (V_{SUPSW} - V_{SENSP})}{V_{SUPSW} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where  $V_{SUPSW}$  and  $V_{SENSP}$  are typical values (such that efficiency is optimum for nominal operating conditions). Ensure the inductor  $I_{SAT}$  is above the buck converter's cycle-by-cycle peak current limit.

**Table 13. Recommended Output Filters For  $I_{LOAD}$  of 3A**

f <sub>sw</sub> (kHz)	L <sub>OUT</sub> (μH)	RECOMMENDED C <sub>OUT</sub>
2200	1.5	22μF ceramic
488	8.2	3 x 22μF ceramic
488	8.2	22μF ceramic + low-ESR 68μF electrolytic (< 0.25Ω)
248	20	22μF ceramic + low-ESR 68μF electrolytic (< 0.25Ω)

### Layout Considerations

Proper PCB layout is critical for robust system performance. See the MAX20461 EV kit datasheet for a recommended layout. Minimize the current-loop area and the parasitics of the DC-DC conversion circuitry to reduce EMI. The input capacitor placement should be prioritized because in a buck converter, the ceramic input capacitor has high  $\frac{di}{dt}$ . Place the input capacitor, power inductor, and output capacitor as close as possible to the IC SUPSW and PGND pins. Shorter traces should be prioritized over wider traces.

A low-impedance ground connection between the input and output capacitor is required (route through the ground pour on the exposed pad). Connect the exposed pad to ground. Place multiple vias in the pad to connect to all other ground layers for proper heat dissipation. Failure to do so can result in the IC repeatedly reaching thermal shutdown. Do not use separate power and analog ground planes. Instead, use a single common ground and manage currents through component placement. High-frequency return current flows through the path of least impedance (through the ground pour directly underneath the corresponding traces).

USB traces must be routed as a 90Ω differential pair with an appropriate keep-out area. Avoid routing USB traces near clocks and high-frequency switching nodes. The length of the routing should be minimized and avoid 90° turns, excessive vias, and RF stubs.

### Determining USB System Requirements

The nominal cable resistance (with tolerance) for both the USB power wire (BUS) and return GND should be determined from the cable manufacturer. In addition, be sure to include the resistance from any inline or PCB connectors. Determine the desired operating temperature range for the application, and consider the change in resistance over temperature.

A typical application presents a 200mΩ BUS resistance with a matching 200mΩ resistance in the ground path. In this application, the voltage drop at the far end of the captive cable is 800mV when the load current is 2A. This voltage drop requires the voltage-adjustment circuitry of the IC to increase the output voltage to comply with the USB and Apple specifications.

### USB Loads

MAX20461 is compatible with both USB-compliant and non-compliant loads. A compliant USB device is not allowed to sink more than 30mA and must not present more than 10μF of capacitance when initially attached to the port. The device then begins its HVD+/HVD- connection and enumeration process. After completion of the connect process, the device can pull 100mA/150mA and must not present a capacitance greater than 10μF. This is considered the hot-inserted, USB-compliant load of 44Ω in parallel with 10μF.



For non-compliant USB loads, the ICs can also support both a hot insertion and soft-start into a USB load of 2Ω in parallel with 330μF.

### USB Output Current Limit

The USB load current is monitored by an internal current-sense amplifier through the voltage created across  $R_{SENSE}$ . MAX20461 offers a digitally adjustable USB current-limit threshold. See SETUP\_2 or [Table 10](#) to select an appropriate register or resistor value for the desired current limit.

Some systems require the need to supply up to 160% of  $I_{LOAD(MAX)}$  for brief periods. It is possible to increase the MAX20461 current limit beyond 3.04A (min) by decreasing  $R_{SENSE}$  using this scaling factor:

$$R_{SENSE} = 33m\Omega \cdot \frac{3.04A}{1.6 \cdot I_{LOAD(MAX)}}$$

### USB Voltage Adjustment

[Figure 9](#) shows a DC model of the voltage-correction function of MAX20461. Without voltage adjustment ( $V_{ADJ} = 0$ ,  $GAIN[4:0] = 0$ ), the voltage seen by the device at the end of the cable will decrease linearly as load current increases. To compensate for this, the output voltage of the buck converter should increase linearly with load current. The slope of

SENSP is called  $R_{COMP}$  such that  $V_{ADJ} = R_{COMP} \cdot I_{LOAD}$  and  $R_{COMP} = GAIN[4:0] \cdot R_{LSB} \cdot \frac{R_{SENSE}}{33m\Omega}$  (see [Figure 10](#)). The  $R_{COMP}$  adjustment values available on MAX20461 are listed in the GAIN[4:0] register description and are based on a 33mΩ sense resistor.

For  $V_{DUT} = V_{NO\_LOAD}$ ;  $0 \leq I_{LOAD}$ ,  $R_{COMP}$  must equal the sum of the system resistances. Calculate the minimum  $R_{COMP}$  for the system so that  $V_{DUT}$  stays constant:

$$R_{COMP\_SYS} = R_{LR} + R_{SENSE} + R_{PCB} + R_{CABLE\_VBUS} + R_{CABLE\_GND}$$

Where  $R_{CABLE\_VBUS} + R_{CABLE\_GND}$  is the round-trip resistance of the USB cable (including the effect from the cable shield, if it conducts current),  $R_{LR}$  is the buck converter's load regulation expressed in mΩ (51mΩ typ.), and  $R_{PCB}$  is the resistance of any additional  $V_{BUS}$  parasitics (the  $V_{BUS}$  FET, PCB trace, ferrites, and the USB connectors). Find the setting for GAIN[4:0] using the minimum  $R_{COMP}$ .

$$GAIN[4:0] = \text{ceiling}\left(\frac{R_{COMP\_SYS}}{R_{LSB}} \cdot \frac{33m\Omega}{R_{SENSE}}\right)$$

The nominal DUT voltage can then be estimated at any load current by:

$$V_{DUT} = V_{NO\_LOAD} + R_{LSB} \cdot GAIN[4:0] \cdot \frac{R_{SENSE}}{33m\Omega} \cdot I_{LOAD} - R_{COMP\_SYS} \cdot I_{LOAD}$$

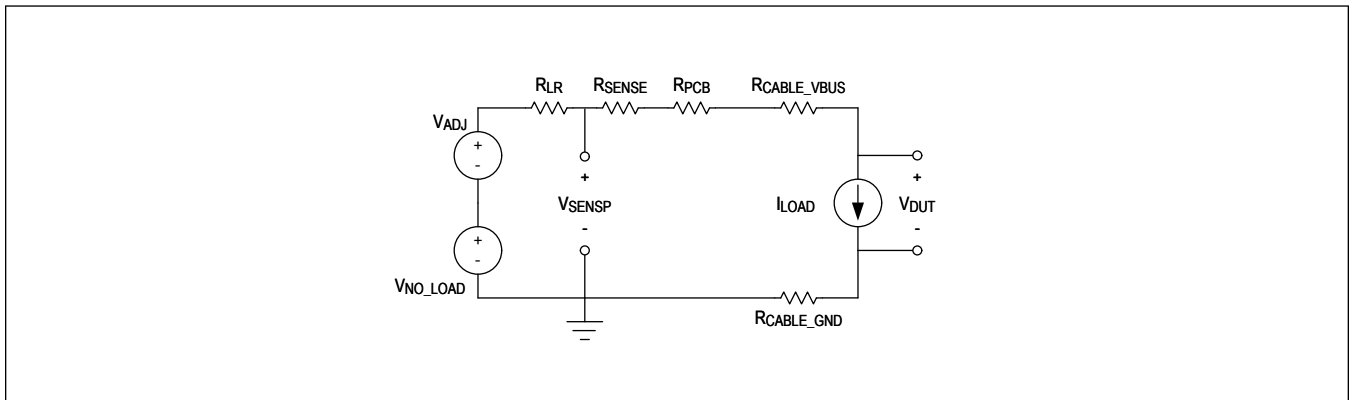


Figure 9. DC Voltage Adjustment Model

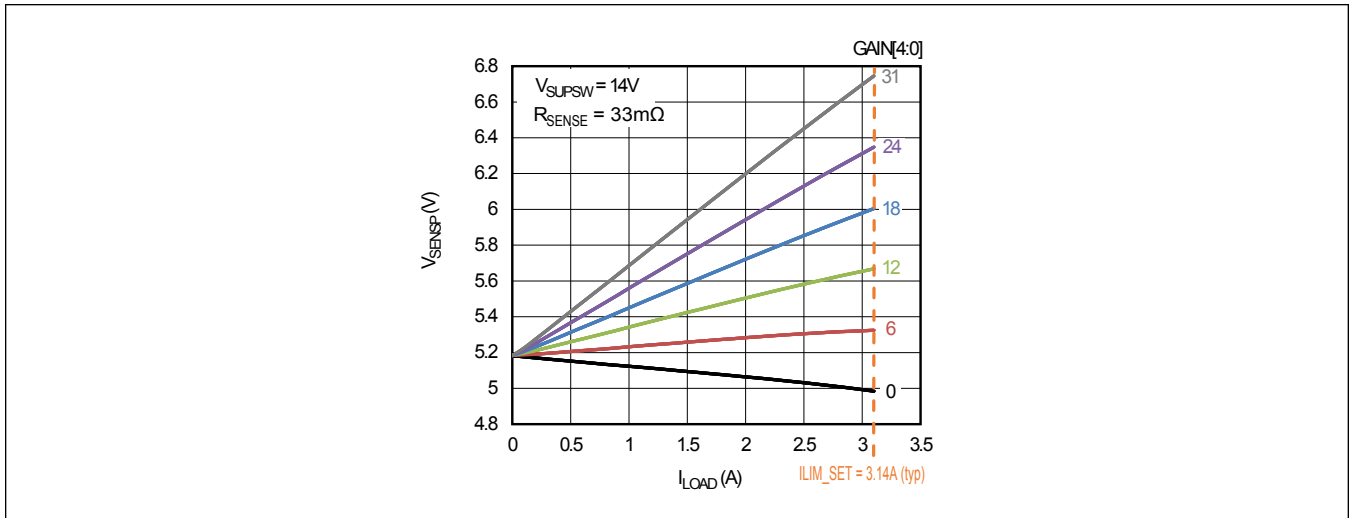


Figure 10. Increase in SENSE vs. USB Current

### Tuning of USB Data Lines

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance, with matched traces of equal length and with no stubs or test points. MAX20461 includes high-bandwidth USB data switches (>1GHz). This means data-line tuning is generally not required. However, all designs are recommended to include pads that would allow LC components to be mounted on the data lines so that tuning can easily be performed later, if necessary. Tuning components should be placed as close as possible to the IC data pins, on the same layer of the PCB as the IC. The proper configuration of the tuning components is shown in Figure 11. Figure 12 shows the reference eye diagram used in the test setup. Figure 13 shows the MAX20461 high-voltage eye diagram on the standard EVKIT with no tuning components. Tuning inductors should be high-Q wire-wound inductors. Contact Maxim’s application team for assistance with the tuning process for your specific application.

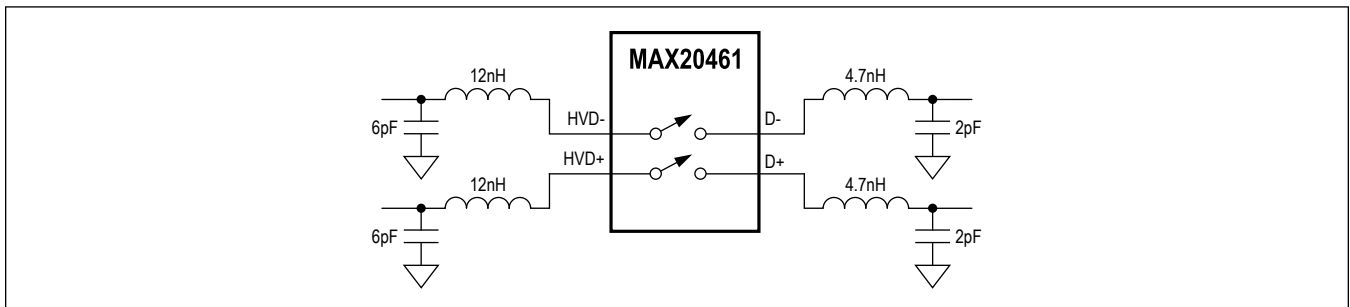


Figure 11. Tuning of Data Lines

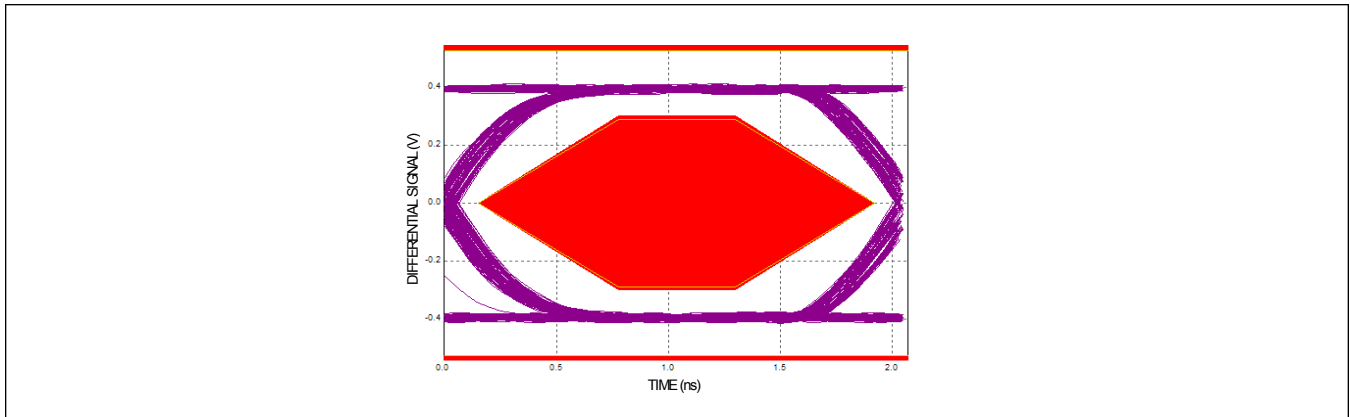


Figure 12. Near-Eye Diagram (with No Switch)

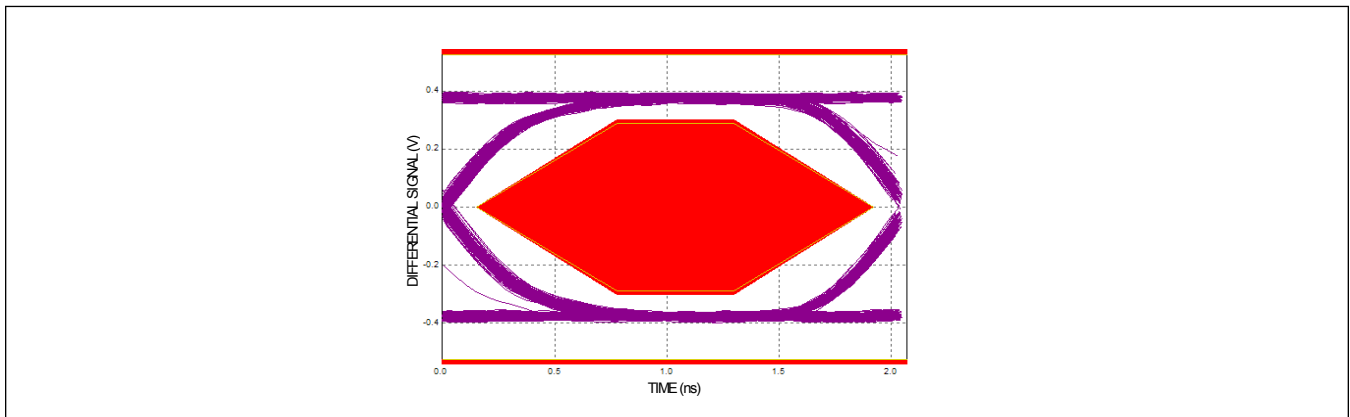


Figure 13. Untuned Near-Eye Diagram (with MAX20461)

### USB Data Line Common-Mode Choke Placement

Most automotive applications use a USB-optimized common-mode choke to mitigate EMI signals from both leaving and entering the module. Optimal placement for this EMI choke is at the module's USB connector. This common-mode choke does not replace the need for the tuning inductors previously mentioned.

### ESD Protection

The high-voltage MAX20461 requires no external ESD protection. All Maxim devices incorporate ESD protection structures to protect against electrostatic discharges encountered during handling and assembly. While competing solutions can latch-up and require the power to be cycled after an ESD event, the MAX20461 continues to work without latch-up. When used with the configuration shown in the [Typical Application Circuit](#), the MAX20461 is characterized for protection to the following limits:

- $\pm 25\text{kV}$  ISO 10605 (330pF, 2k $\Omega$ ) Air Gap
- $\pm 8\text{kV}$  ISO 10605 (330pF, 2k $\Omega$ ) Contact
- $\pm 15\text{kV}$  IEC 61000-4-2 (150pF, 330 $\Omega$ ) Air Gap
- $\pm 8\text{kV}$  IEC 61000-4-2 (150pF, 330 $\Omega$ ) Contact
- $\pm 15\text{kV}$  ISO 10605 (330pF, 330 $\Omega$ ) Air Gap
- $\pm 8\text{kV}$  ISO 10605 (330pF, 330 $\Omega$ ) Contact

Note: All application-level ESD testing is performed on the standard evaluation kit with 1m captive cable.

## ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

## Human Body Model

[Figure 14](#) shows the Human Body Model, and [Figure 16](#) shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

## IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. MAX20461 helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Because the series resistance is lower in the IEC 61000-4-2 ESD test model [Figure 15](#), the ESD withstand-voltage measured to this standard is generally lower than that measured using the Human Body Model. [Figure 17](#) shows the current waveform for the 8kV, IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

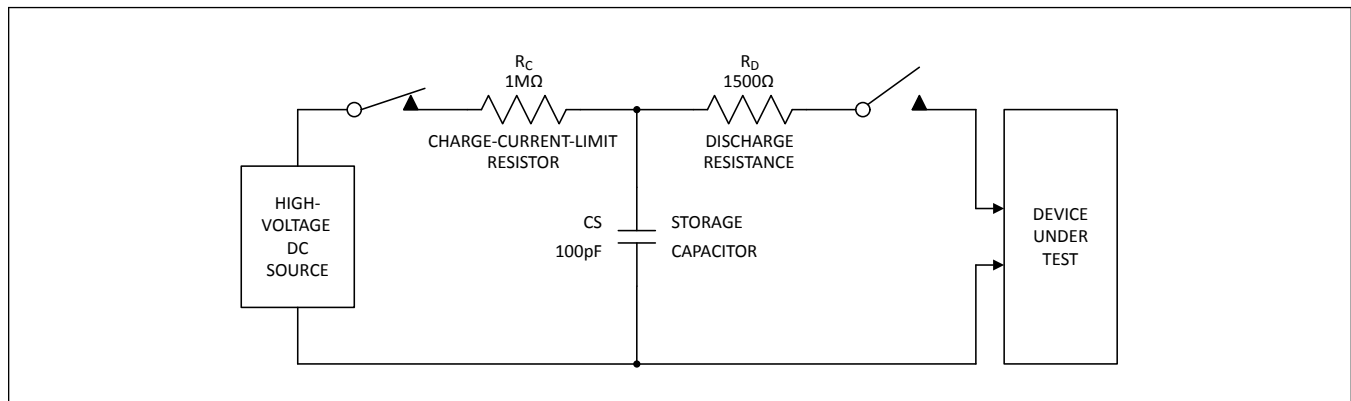


Figure 14. Human Body ESD Test Model

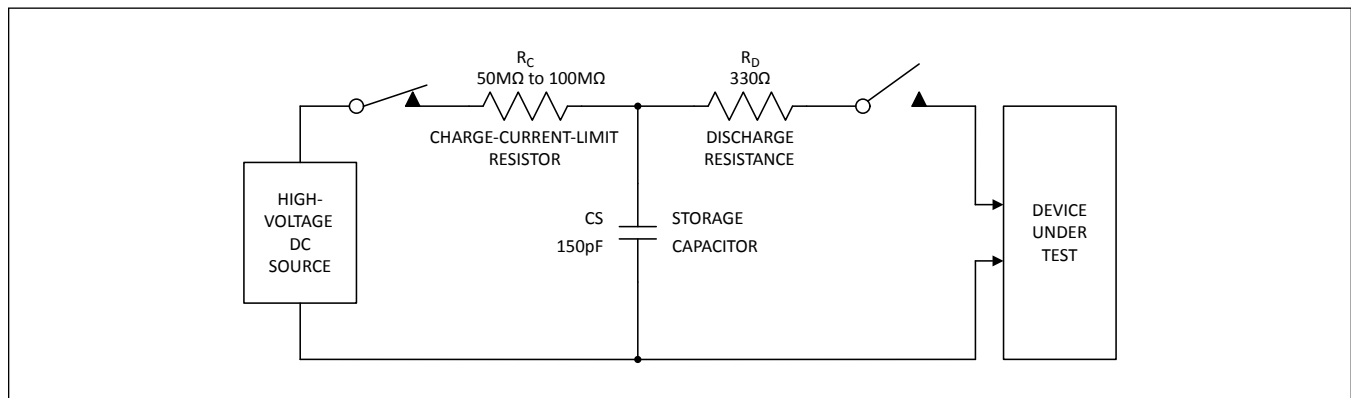


Figure 15. IEC 61000-4-2 ESD Test Model

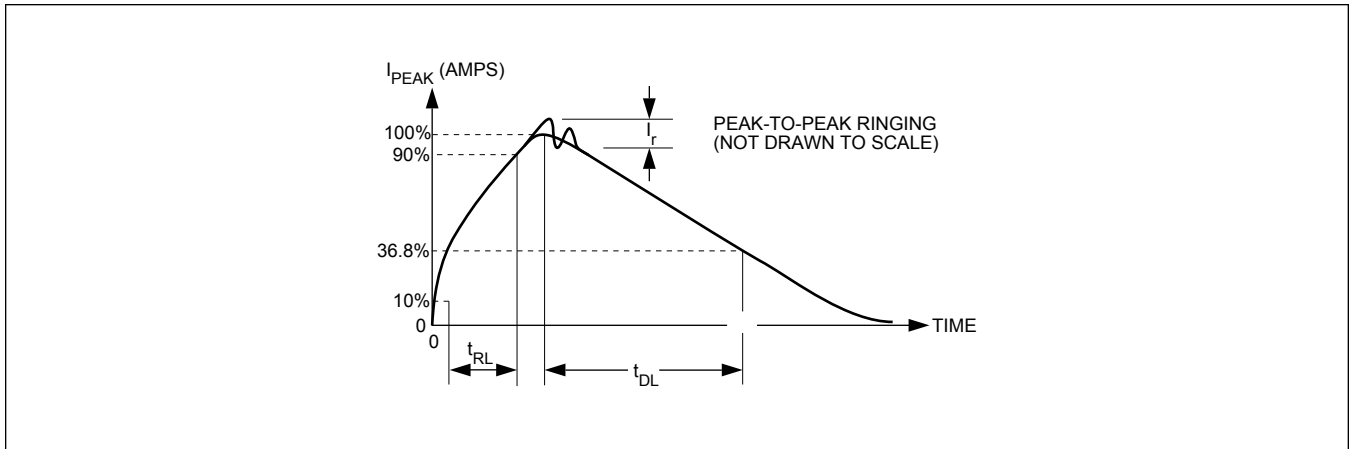


Figure 16. Human Body Current Waveform

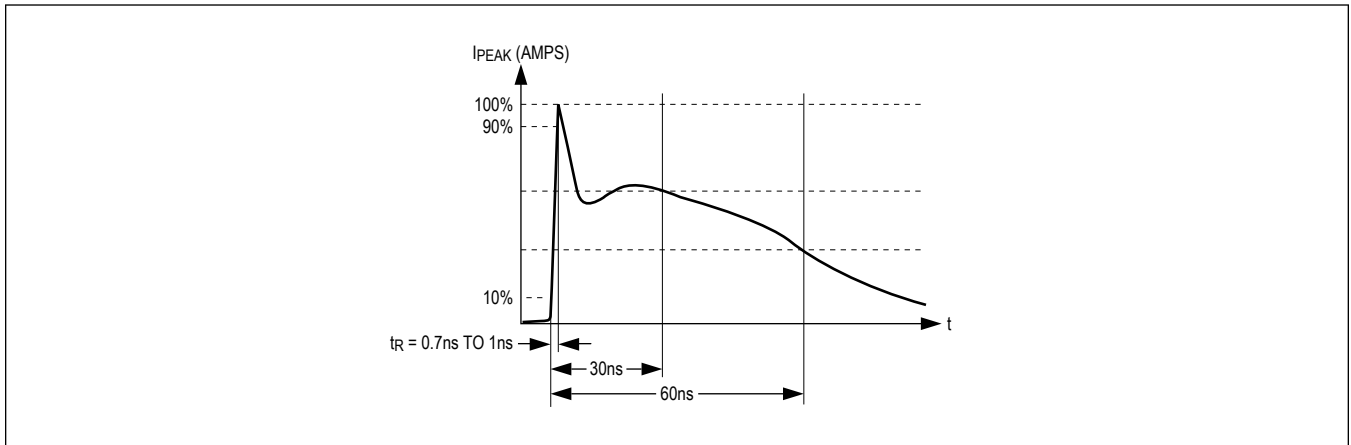
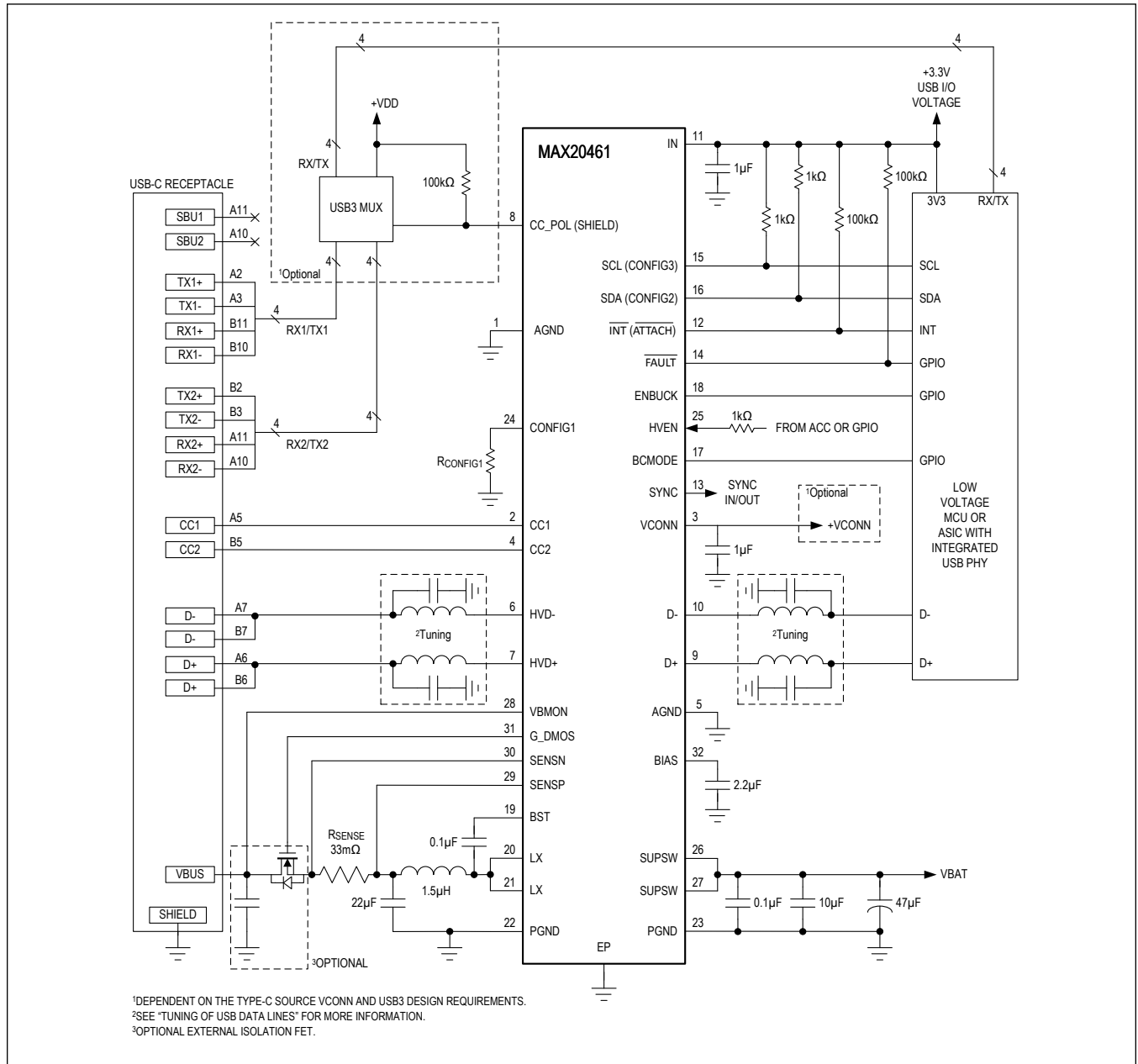


Figure 17. IEC 61000-4-2 Current Waveform

Typical Application Circuits

Typical Application Circuit



## Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	STARTUP MODE (BCMODE PIN = 0)	I <sup>2</sup> C	V <sub>CONN</sub>	NOMINAL OUTPUT CURRENT FOR APPLE R30+ SPECIFICATIONS
MAX20461ATJA/V+	-40°C to +125°C	32 TQFN-EP	SDP Mode	Yes	Yes	2.4 Amp
MAX20461ATJD/V+				No		
MAX20461AATJA/V+				Yes		
MAX20461AATJD/V+				No		
MAX20461AATJM/V+		32 SWTQFN-EP		Yes	No	3.0 Amp
MAX20461AATJM/VY+				No		
MAX20461AATJP/V+				No		

/V Denotes Automotive Qualified Parts

+ Denotes a lead(Pb)-free/RoHS-compliant package.

EP = Exposed pad.

Y = Side-wettable (SW) package.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/18	Initial release	—
1	8/18	Updated <i>General Description, Simplified Block Diagram, Absolute Maximum Ratings, Package Information, TOCs 4, 7–10, 13, 17, 18, 25, Pin Configuration, Pin Description, Figure 1, CC Attachment and VBUS Discharge diagram, Detailed Description, USB Type-C, VCONN, Figure 2, VBUS, External FET Gate Drive (G_DMOS Pin), System Enable (HVEN), Linear Regulator Output (BIAS), Maximum Duty-Cycle Operation, Reset Behavior, Output Short-Circuit Protection, Figure 3, USB Host Adapter Emulator, I2C Configuration (CONFIG1 and I2C), I2C Diagnostics and Event Handling, Interrupt and Attach Output (INT(ATTACH)), Fault Output Pin (FAULT), Table 11, Register Map, SETUP_3 (0x3), SETUP_4 (0x04), CC_REQUEST (0x06), IRQ_MASK_0 (0x07), IRQ_0 (0xA), STATUS_0 (0xD), STATUS_1 (0xE), DC-DC Input Capacitor Selection, DC-DC Output Capacitor Selection, USB Voltage Adjustment, Tuning of USB Data Lines, Figure 9, Figure 10, Typical Application Circuit, and Ordering Information.</i>	1, 21, 23, 25, 26, 27, 29–31, 33, 35, 38–41, 44, 45, 46, 48, 49, 52, 53, 55, 57, 60, 61
2	4/20	Updated <i>General Description, Benefits and Features, Absolute Maximum Ratings, Package Information, Electrical Characteristics, Typical Operating Characteristics, Functional Diagrams, Detailed Description, Register Details, and Applications Information.</i>	1, 6, 7, 9, 10, 12, 14, 15, 19, 21, 27–30, 38, 41, 44, 51, 57
3	6/20	Added MAX20461A. Updated <i>Benefits and Features, Simplified Block Diagram, Absolute Maximum Ratings, Electrical Characteristics, Pin Configuration, Pin Description, DCP Reset Behavior and Timing Diagram, ENBUCK Reset Behavior and Timing Diagram, ATTACH Logic Diagram, CC Attachment and VBUS Discharge, Detailed Block Diagram, CC Pulldown Response, VCONN, External FET Gate Drive (G_DMOS Pin), Power-On Sequencing, Switching Frequency Configuration, Switching Frequency Synchronization (SYNC Pin), CONFIG2 and CONFIG3 Pin Table (Standalone Variants), Fault Conditions, SYNC_DIR bit, SS_EN bit, CD bit, Ordering Information.</i>	1–63
4	12/20	Updated USB Type-C functionality to meet latest specifications (search for $t_{DIS\_DET}$ ). Improved SYNC pin logic for multi-port applications (search for SYNC). Expanded design methods for overcurrent flexibility (search for $I_{LOAD(MAX)}$ ).	1–65
5	5/21	Added MAX20461AATJM and MAX20461AATJP. Updated <i>Electrical Characteristics, ToCs 26–27, USB On-The-Go and Dual-Role Applications, Data Switch Mode Truth Table, Typical Application Circuit and Ordering Information.</i>	13, 17, 35, 36, 37, 63, 64, 65
6	7/22	Added side-wettable MAX20461AATJM/VY. Updated <i>Package Information, Electrical Characteristics, Pin Configurations, Data Format of I2C Interface, ADC_1 (0x11) and Ordering Information.</i>	8, 12, 18, 41, 53, 62, 63
7	9/23	Added TOC28, updated <i>ADC_0 (0x10), ADC_1 (0x11), and I<sup>2</sup>C Output Voltage and Current Measurement.</i>	18, 40, 54