EVALUATION KIT AVAILABLE

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MAX25601A/MAX25601B/ MAX25601C/MAX25601D

Synchronous Boost and Synchronous Buck LED Controllers

General Description

The MAX25601A/B/C/D is a synchronous boost controller followed by a synchronous buck LED controller. The 4.5V to 40V input voltage range of the boost controller is ideal for automotive applications, and acts as a pre-boost power supply for the second-stage buck LED controller.

The synchronous boost is a current-mode controller that can be be paralleled with another device to provide higher output power. A SYNCOUT pin provides the clock to drive the RT/SYNCIN pin of the other device, enabling two-phase 180-degree out-of-phase operation. The boost converter can be programmed with a switching frequency of 200kHz to 2.2MHz. Spread spectrum is included to reduce EMI. An internal digital soft-start feature is provided to enable a smooth power up of the boost output. Protection features like hiccup mode, overvoltage protection, and thermal shutdown are provided.

The synchronous buck LED controller uses Maxim's F^3 Architecture, a proprietary average-current-mode control scheme to regulate the inductor current at a constant switching frequency without any control-loop compensation. Inductor current is sensed in the bottom synchronous n-channel MOSFET. The device operates over a wide 4.5V to 65V input range at switching frequencies as high as 1MHz. Both analog and PWM dimming are included. LED current can be monitored on the IOUTV pin.

Both controllers have high- and low-side gate drivers with at least 1A peak source and sink-current capability. Adaptive non-overlap control logic prevents shoot-through currents during transition. Both the boost and the buck faults are monitored on the $\overline{FLT}$ pin.

The MAX25601A/C is available in a 32-pin SWTQFN package and the MAX25601B/D is available in a 28-pin TSSOP package. The 32-pin package features an additional switch control that can be used in high-beam/low-beam and heads-up display applications.

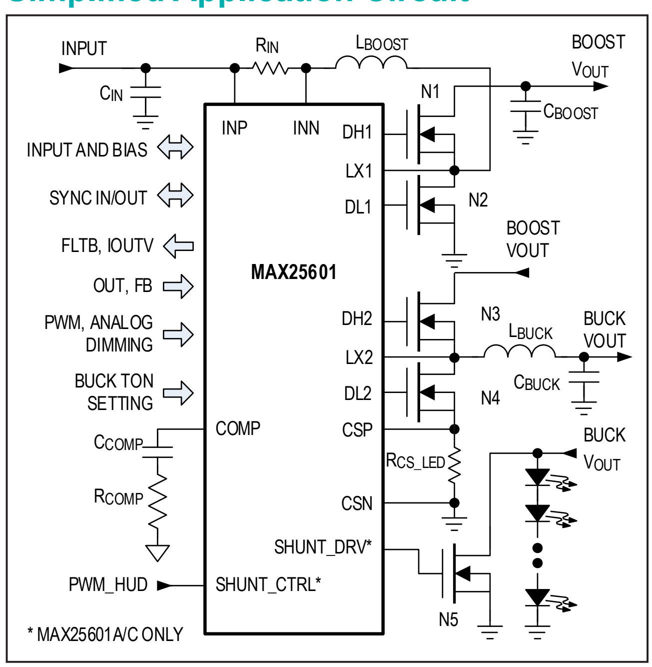
Applications

- Automotive Exterior Lighting: High-Beam/Low-Beam/ Signal/Position Lights, Daytime Running Lights (DRLs), Matrix Light, Pixel Light, and Other Adaptive Front-Light Assemblies
- Commercial, Industrial, and Architectural Lighting

Benefits and Features

- Integration Minimizes BOM for High-Brightness LED Driver, Saving Space and Cost
  - Wide Input-Voltage Range from 4.5V to 40V
  - Wide Boost-Output Range up to 65V
  - Programmable Switching Frequency Optimizes Component Size
  - External MOSFETs Can be Sized for Appropriate Current
  - Synchronous Rectification Provides High Efficiency and Fast Transient Response
  - Average Current-Mode Control for Buck Eliminates Compensation Components
- Wide Dimming Ratio Allows High Contrast Ratio
  - Analog Dimming and PWM Dimming
  - Analog Voltage-Controlled PWM Dimming
- Protection Features and Wide Temperature Range Increase System Reliability
  - Short Circuit, Overvoltage, and Thermal Protection
  - -40°C to +125°C Operating Temperature Range

Simplified Application Circuit



Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

IN, UVEN, INP, INN to AGND
(MAX25601A, MAX25601B)..............................-0.3V to +40V
IN, UVEN, INP, INN to AGND
(MAX25601C, MAX25601D) ....-0.3V to +52V
LX1, TON to PGND ....-0.3V to +70V
LX2 to PGND...-1V to +70V
BST_ to LX_...-0.3V to +6V
DH_ to LX_.. -0.3V to $V_{BST\_}$ +0.3V
DL_, SHUNT_DRV to PGND ....-0.3V to V_{DRV}+0.3V
CSP, CSN to PGND ....-2.5V to +6V
CSP to CSN, INP to INN.....................................-0.3V to +0.3V
V_{CC} to SGND...-0.3V to V_{DRV}+0.3V
REFI, IOUTV, SYNCOUT to AGND............-0.3V to V_{DRV}+0.3V
FB, OUT, COMP to AGND ....-0.3V to V_{DRV}+0.3V
$\overline{FLT}$, SHUNT_CTRL, PWMDIM,
RT/SYNCIN to AGND..-0.3V to +6V

VDRV to PGND..-0.3V to +6V
PGND to AGND...-0.3V to +0.3V
Continous Power Dissipation (Single-Layer Board),
32 pin SW TQFN T3255Y+6C
(T_A = +70°C, derate 21.3mW/°C above +70°C.).......1702mW
Continuous Power Dissipation (Multilayer Board),
32 pin SW TQFN T3255Y+6C
(T_A = +70°C, derate 34.5mW/°C above +70°C.).......2759mW
Continuous Power Dissipation (Single-Layer Board),
28 pin TSSOP U28E+1C
(T_A = +70°C, derate 22.2mW/°C above +70°C.).......1777mW
Continuous Power Dissipation (Multilayer Board),
28 pin TSSOP U28E+1C (T_A = +70°C,
derate 29.7mW/°C above +70°C.)................. mW to 2380mW
Operating Temperature Range............................-40°C to 125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 pin TQFN

Package Code	T3255Y+6C
Outline Number	**21-100041**
Land Pattern Number	**90-100066**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

28 pin TSSOP

Package Code	U28E+1C
Outline Number	**21-100182**
Land Pattern Number	**90-100069**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33.6°C/W
Junction to Case (θ_{JC})	3.3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 12V, V_{UVEN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE						
Input Voltage Range	V_{IN}	MAX25601A/MAX25601B	5		36	V
		MAX25601C/MAX25601D	5		48	
		IN connected to V_{DRV} and V_{CC} (external bias)	4.5		5.5	
Quiescent Current	I_Q	V_{DIM} = 5V, V_{IN} = 12V, V_{OUT_BOOST} = 48V, boost and buck not switching		5	10	mA
Shutdown Current	I_{SHDN}	V_{DIM} = 0V, V_{IN} = 12V, V_{UVEN} = 0V			12	µA
V_{CC} and V_{DRV}						
V_{DRV} Output Voltage	V_{DRV}	I_{VDRV} = 30mA, 5.5V ≤ V_{IN} ≤ 36V	4.95	5.0	5.05	V
		I_{VDRV} = 10mA to 60mA, 6V ≤ V_{IN} ≤ 25V	4.90	5.0	5.10	
V_{DRV} Dropout Voltage		I_{VDRV} = 5mA, V_{IN} = 4.5V		35	100	mV
V_{DRV} Short-Circuit Current	$VDRV_{IMAX}$	V_{DRV} = 4.5V, V_{IN} = 6V	90			mA
V_{DRV} Undervoltage Lockout Rising	$VDRV_{UVLOR}$	Rising voltage		3.92		V
V_{DRV} Undervoltage Lockout Falling	$VDRV_{UVLOF}$	Falling voltage		3.45		V
UV ENABLE						
UVEN Threshold	V_{TH_UVEN}		1.12	1.24	1.37	V
Hysteresis				100		mV
$\overline{FLT}$						
$\overline{FLT}$Low Voltage		Any boost or buck fault present			0.4	V
$\overline{FLT}$Leakage Current	$\overline{FLT}_{LK}$	$V_{\overline{FLT}}$ = 5.5V, 100kΩ pullup			1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		Rising		165		°C
Thermal Shutdown Hysteresis				10		°C
BUCK / OFF-TIME CONTROL						
Minimum Off-Time	$t_{OFF\_MIN\_BUCK}$	V_{CSP} - V_{CSN} = 0V		125	200	ns
Maximum Off-Time				42		µs
CS Comparator Propagation Delay	t_{CS_DLY}			65		ns
Linear Range of Pulse Doubler			0		5	µs

Electrical Characteristics (continued)

(V_{IN} = 12V, V_{UVEN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BUCK / ON-TIME CONTROL/OVERVOLTAGE PROTECTION/SHORT FAULT INDICATOR						
Minimum On-Time	$t_{ON\_MIN\_BUCK}$			110		ns
Maximum On-Time	$t_{ON\_MAX\_BUCK}$	T_{ON} = GND, V_{OUT} = 1V		24		µs
t_{ON} Pulldown Resistance		V_{IN} = 65V, R_{TON} > 20kΩ		15	30	Ω
t_{ON}Threshold to DH Falling Delay	$t_{ON\_DLY\_BUCK}$			65		ns
OUT Overvoltage Threshold	$V_{TH\_OVP\_BUCK}$	OUT rising	2.38	2.5	2.62	V
OUT Overvoltage Hysteresis		OUT falling		20		mV
Short Fault Threshold	OUT_{V_SHF}	Output falling, V_{OUT} is lower than threshold		50		mV
Programmed On-Time		V_{OUT_BUCK} = 1V, R_{TON} = 50kΩ, C_{TON} = 1nF		4.55		µs
BUCK / ANALOG DIMMING INPUT						
REFI Input Voltage Range	V_{REFI_RNG}		0.2		1.2	V
REFI Zero Current Threshold	V_{REFI_ZC}	V_{CSP} - V_{CSN} < 5mV	0.16	0.18	0.20	V
Internal REFI Clamp Voltage	V_{REFI_CLMP}	I_{REFI} sink = 1µA	1.254	1.3	1.326	V
REFI Input Bias Current	I_{REFI}	V_{REFI} = 0 to V_{CC}		20	200	nA
BUCK / BUCK FAULTS						
LED Open-Fault Enable Threshold	LOF_{REFI_VTH}	V_{REFI} greater than this threshold, 50mV (typ) hysteresis	300	325	350	mV
LED Open-Fault Detection Threshold	LOF_{IOUTV_TH}	V_{IOUTV} lower than the threshold when DIM is high	10	25	40	%
BUCK / CURRENT-SENSE AMPLIFIER						
Buck Current-Sense Gain	CSA_{BUCK}			5		V/V
Buck Current-Sense Amplifier Offset	$V_{CS\_OFS\_BUCK}$		0.182	0.2	0.208	V
BUCK / PWM AND ANALOG-TO-PWM DIMMING						
DIM Input High	V_{DIM_IH}	DIM Rising	2.0			V
DIM Input Low	V_{DIM_IL}	DIM Falling			0.8	V
DIM Rising to DL2 Rising Delay	t_{DIM_RIS}	DIM Rising		100		ns
External DIM Frequency Range	f_{DIM_EXT}		10		2000	Hz
Internal Ramp Frequency	f_{DIM_INT}		180	200	220	Hz
DIM Comparator Offset Voltage	V_{DIM_OFS}		170	200	230	mV
DIM Voltage for 100% Duty Cycle			3.2			V

Electrical Characteristics (continued)

(V_{IN} = 12V, V_{UVEN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BUCK / GATE DRIVERS							
DH2 Gate Driver On-Resistance	R_{DH2_SRC}	T_A = -40°C to +125°C, BST2-LX2 forced to 5V	DH2 = high		2.5	5.0	Ω
	R_{DH2_SINK}		DH2 = low		1.0	2.0	
DH2 Gate Driver Source/ Sink Current	I_{DH2}	DH2-LX2 forced to 2.5V, BST2-LX2 forced to 5V.			1		A
DL2 Gate Driver On-Resistance	R_{DL2_SRC}	T_A = -40°C to +125°C	DL2 = high		2.5	5.0	Ω
	R_{DL2_SINK}		DL2 = low		1.0	3.0	
DL2 Gate Driver Source/ Sink Current	I_{DL2}				1		A
DL2 to DH2 Deadtime		DL2 fall to DH2 rise, C_L = 1nF			20		ns
BUCK / CURRENT MONITOR (I_{OUTV})							
Current Sense Gain					5		
Current Sense Offset				0.182	0.2	0.208	V
I_{OUTV} Source/Sink Current					±0.5		mA
BOOST / OSCILLATOR							
Switching-Frequency Range	F_{SW_RNG}	Set by the RT resistor, 14kΩ < R_{RT} < 171kΩ, or by an external clock		200		2200	kHz
Switching Frequency	F_{SW_BOOST}	Spread-Spectrum Disabled	R_{RT} = 85kΩ	370	400	430	kHz
			R_{RT} = 14kΩ	1980	2200	2365	
Spread-Spectrum Spreading Factor					±6		%
RT/SYNCIN Regulation Voltage		15kΩ < R_{RT} < 171kΩ			1.25		V
Soft-Start Time	t_{SS}	Voltage mode soft-start; based on F_{SW_BOOST} clocks			3712		clocks
Hiccup Period	t_{hiccup}	Triggers when current limit is reached and boost output voltage < 70%; based on F_{SW_BOOST} clocks			21504		clocks
Minimum Off-Time	$t_{OFF\_MIN\_BST}$				60		ns
Minimum On-Time	$t_{ON\_MIN\_BST}$				60		ns
RT/SYNCIN Input Low	V_{SYNCIN_IL}					1	V
RT/SYNCIN Input High	V_{SYNCIN_IH}			2.5			V
SYNCOUT Clock		Phase relation between internal oscillator clock and SYNCOUT clock			180		deg
BOOST / GATE DRIVERS							
DH1 Gate Driver On-Resistance	R_{DH1_SRC}	T_A = -40°C to +125°C, BST1-LX1 forced to 5V	DH1 = high		1.6	3.2	Ω
	R_{DH1_SINK}		DH1 = low		1.0	2.0	
DH1 Gate Driver Source/ Sink Current	I_{DH1}	DH1-LX1 forced to 2.5V, BST1-LX1 forced to 5V			1		A

Electrical Characteristics (continued)

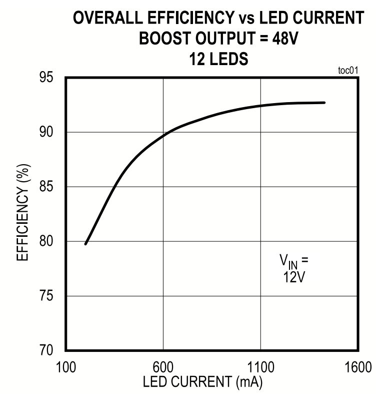
(V_{IN} = 12V, V_{UVEN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

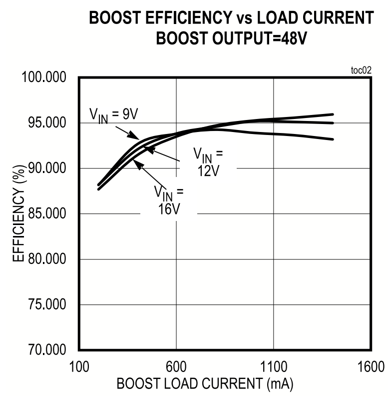
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DL1 Gate Driver On-Resistance	R_{DL1_SRC}	T_A = -40°C to +125°C	DL1 = high		1.7	3.5	Ω
	R_{DL1_SINK}		DL1 = low		0.8	1.6	
DL1 Gate Driver Source/ Sink Current	I_{DL1}				1.5		A
DH1 to DL1 Deadtime		DH1 fall to DL1 rise, C_L = 5nF			20		ns
DL1 to DH1 Deadtime		DL1 fall to DH1 rise, C_L = 5nF			20		ns
BOOST / REGULATION / CURRENT SENSE							
Feedback Voltage	V_{FB}			0.990	1.01	1.035	V
FB Input Current		T_A = 25°C		-1		+1	µA
OVP Threshold	$V_{TH\_OVP\_BST}$			1.14	1.20	1.24	V
OVP Hysteresis		Falling voltage			100		mV
INP-INN Current-Limit Threshold	V_{ILIM_BST}	Peak current limit		70	85	100	mV
INP-INN Negative Current-Limit Threshold	$V_{NEG\_ILIM\_BST}$	With respect to positive current limit			-30		%
Boost Current-Sense Gain	CSA_{BOOST}			9	11	12	V/V
Boost Current-Sense Amplifier Offset	$V_{CS\_OFS\_BOOST}$				0.5		V
Peak Slope-Compensation Ramp Voltage	V_{SC_RAMP}	8V ≤ V_{IN} ≤ 20V	R_{DL2} = 30kΩ		1.39		V
			R_{DL2} = 100kΩ		2.08		
BOOST / ERROR AMPLIFLIER							
Transconductance	Gm			200	300	400	µS
COMP Source Current		FB = 0V for maximum Gm source current			+92		µA
COMP Sink Current		FB = 2V for Minimum GM sink current			-45		µA
COMP Clamp Voltage					4		V
COMP Output Offset	V_{COMP_OFS}				1.7		
HUD INPUT/OUTPUT (32-pin TQFN Only)							
PWM_HUD Input High	$V_{PWM\_HUD\_IH}$	PWM_HUD Rising		2.0			V
PWM_HUD Input Low	$V_{PWM\_HUD\_IL}$	PWM_HUD Falling				0.8	V
PWM_HUD to HUD_ OUT Delay	t_{HUD_DLY}	PWM_HUD Rising to HUD_OUT Falling, or PWM_HUD Falling to HUD_OUT Rising. C_L = 10nF.			30		ns
HUD_OUT Driver On-Resistance	R_{HUD_SRC}	T_A = -40°C to +125°C	HUD_OUT = high		2.5	5	Ω
	R_{HUD_SNK}		HUD_OUT = low		1.5	3.0	
PWM_HUD Input Resistance					600		kΩ

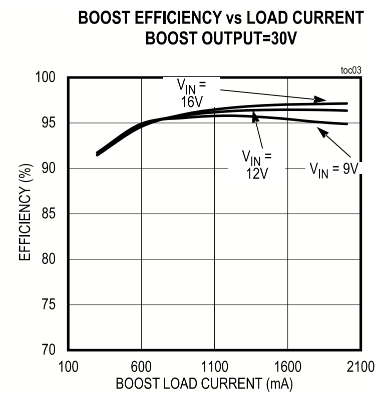
Note 1: Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

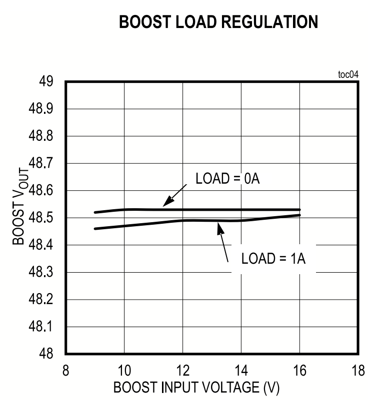
Typical Operating Characteristics

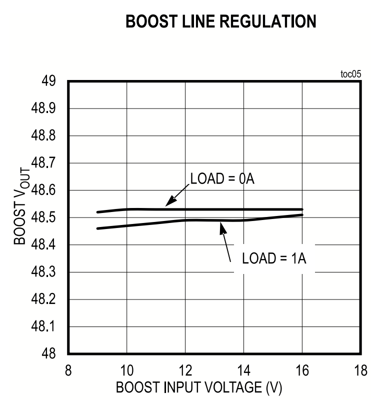
(V_{IN} = 12V, V_{REFI} = 1.2V, V_{DIM} = V_{CC}, C_{VCC} = C_{VDRV} = 4.7µF, T_A = +25°C, unless otherwise noted.)

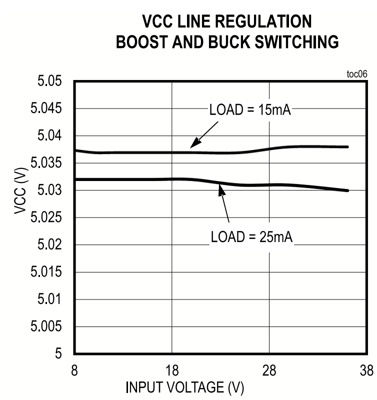


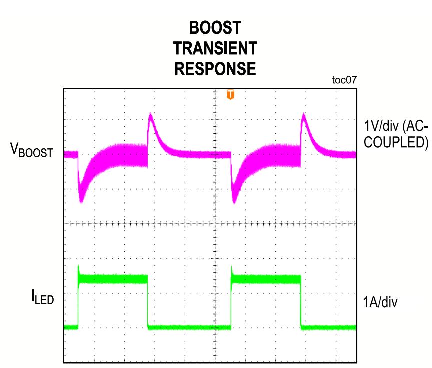


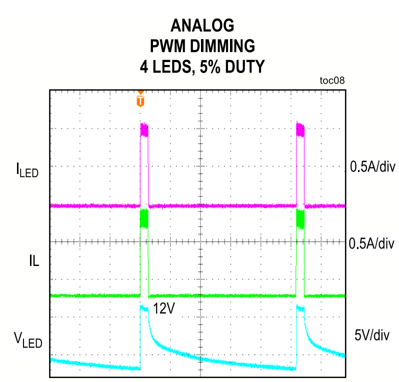


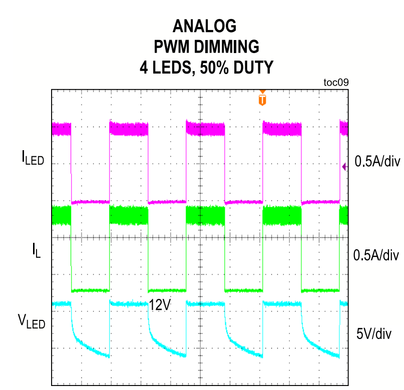








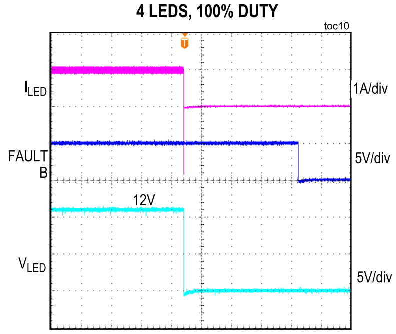




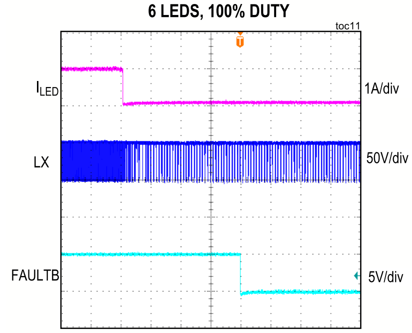
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{REFI} = 1.2V, V_{DIM} = V_{CC}, C_{VCC} = C_{VDRV} = 4.7µF, T_A = +25°C, unless otherwise noted.)

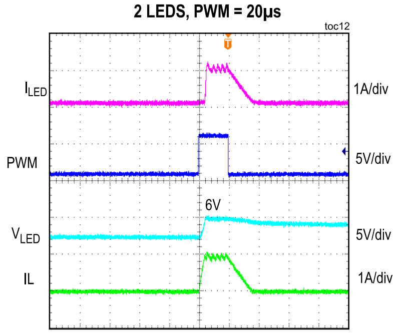
LED SHORT FAULT 4 LEDS, 100% DUTY



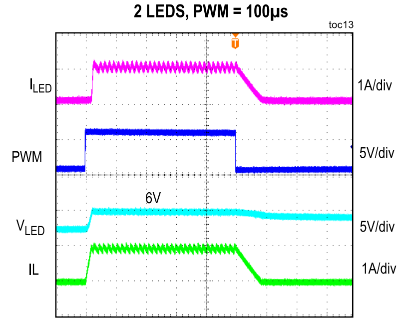
LED OPEN FAULT 6 LEDS, 100% DUTY



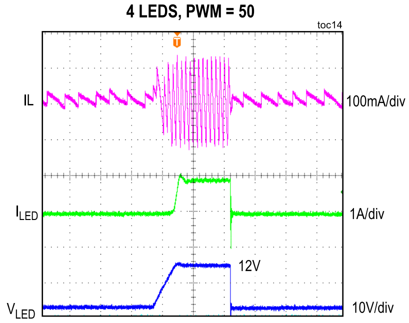
EXTERNAL PWM DIMMING 2 LEDS, PWM = 20µs



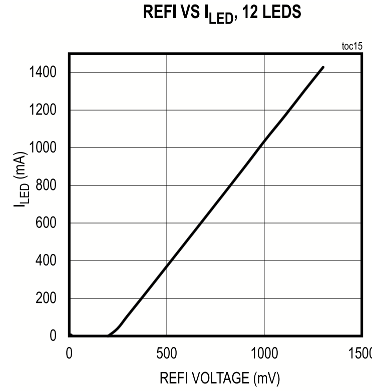
EXTERNAL PWM DIMMING 2 LEDS, PWM = 100µs



SHUNT PWM DIMMING 4 LEDS, PWM = 50



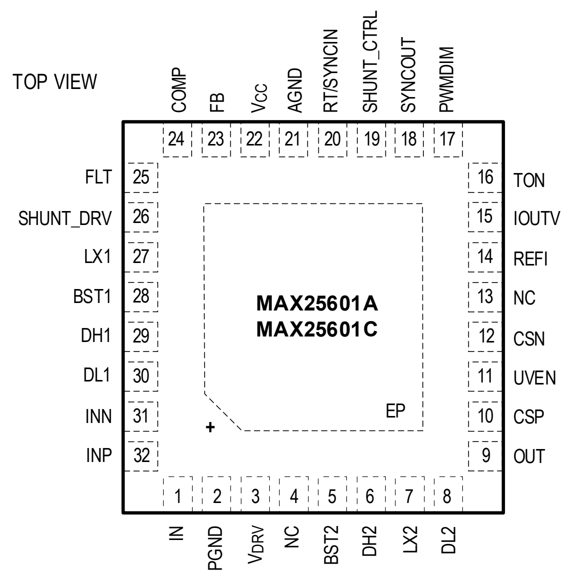
REFI VS I_{LED}, 12 LEDS



PRELIMINARY

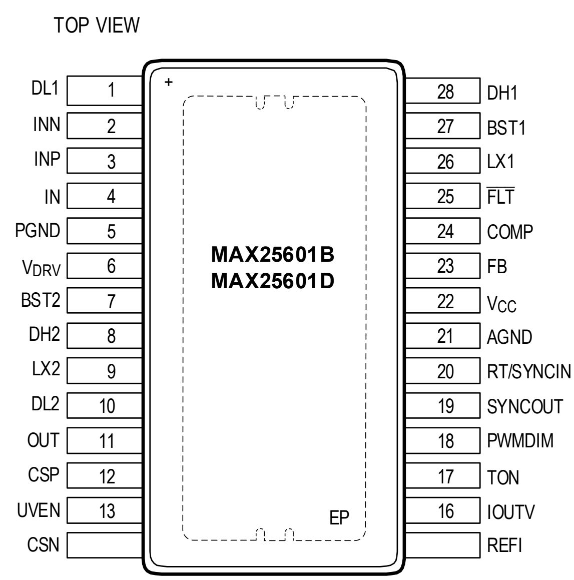
Pin Configurations

TQFN



TQFN-EP (SW)
(5mm x 5mm)

TSSOP



TSSOP-EP

Pin Description

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>TQFN</th><th>TSSOP</th></tr>
<tr><td>1</td><td>4</td><td>IN</td><td>Supply Input for V_{DRV} regulator. Connect a 0.1µF ceramic capacitor from this pin to PGND. If an external bias is used, then connect IN to V_{DRV}.</td></tr>
<tr><td>2</td><td>5</td><td>PGND</td><td>Power Ground</td></tr>
<tr><td>3</td><td>6</td><td>VDRV</td><td>+5V Regulator Output and Driver Supply. Connect a 4.7µF ceramic capacitor from V_{DRV} to PGND. If an external bias is used, then connect IN to V_{DRV}, and connect the external supply to V_{DRV}.</td></tr>
<tr><td>4</td><td>—</td><td>NC</td><td>Not Internally Connected</td></tr>
<tr><td>5</td><td>7</td><td>BST2</td><td>High-Side Power Supply for High-Side Gate Drive of Buck LED Regulator. Connect a 0.1µF ceramic capacitor from BST2 to LX2, and a BST diode between V_{DRV} and BST2.</td></tr>
<tr><td>6</td><td>8</td><td>DH2</td><td>High Side Driver of Buck LED Regulator. Connect to gate of the buck regulator's high-side n-channel MOSFET. Use series resistor to limit current slew rate and mitigate EMI noise, if required.</td></tr>
<tr><td>7</td><td>9</td><td>LX2</td><td>Switching Node of Buck LED Regulator</td></tr>
<tr><td>8</td><td>10</td><td>DL2</td><td>Low-Side Driver of Buck LED Regulator. Connect to gate of the buck regulator’s low-side n-channel MOSFET. Use series resistor to limit current slew rate and mitigate EMI noise, if necessary.

During startup, DL2 is used to select the slope compensation of the boost regulator based on the following options:
<table>
<tr><th>DL2 RESISTOR TO PGND</th><th>SLOPE COMPENSATION SELECTION</th></tr>
<tr><td>100kΩ</td><td>Larger slope compensation for boost output voltages greater than 45V</td></tr>
<tr><td>30kΩ</td><td>Smaller slope compensation for boost output voltages less than 45V</td></tr>
</table></td></tr>
<tr><td>9</td><td>11</td><td>OUT</td><td>Feedback Voltage of Buck. Connect a resistor-divider from this pin to the output voltage on buck. This pin has the scaled-down feedback of the output voltage of the buck.</td></tr>
<tr><td>10</td><td>12</td><td>CSP</td><td>Positive Current-Sense Input for Buck Regulator. Connect a resistor from this pin to CSN to sense the buck regulator inductor current.</td></tr>
<tr><td>11</td><td>13</td><td>UVEN</td><td>Input UVLO and Enable Pin. Dual-function pin to set the input UV threshold, or to use as an enable input. The UVEN threshold is set at 1.24V (typ).</td></tr>
<tr><td>12</td><td>14</td><td>CSN</td><td>Negative Current-Sense Input for Buck Regulator</td></tr>
<tr><td>13</td><td>---</td><td>NC</td><td>Not Internally Connected</td></tr>
<tr><td>14</td><td>15</td><td>REFI</td><td>Analog Dimming Input for Buck LED Regulator. The voltage at REFI sets the LED current.Connect a resistor-divider from V_{CC} to set the default LED current. Alternatively, drive REFI with an external voltage source for analog dimming.
$I_{LED} = (V_{REFI} - 0.2)/(5 \times R_{CS\_LED})$</td></tr>
</table>

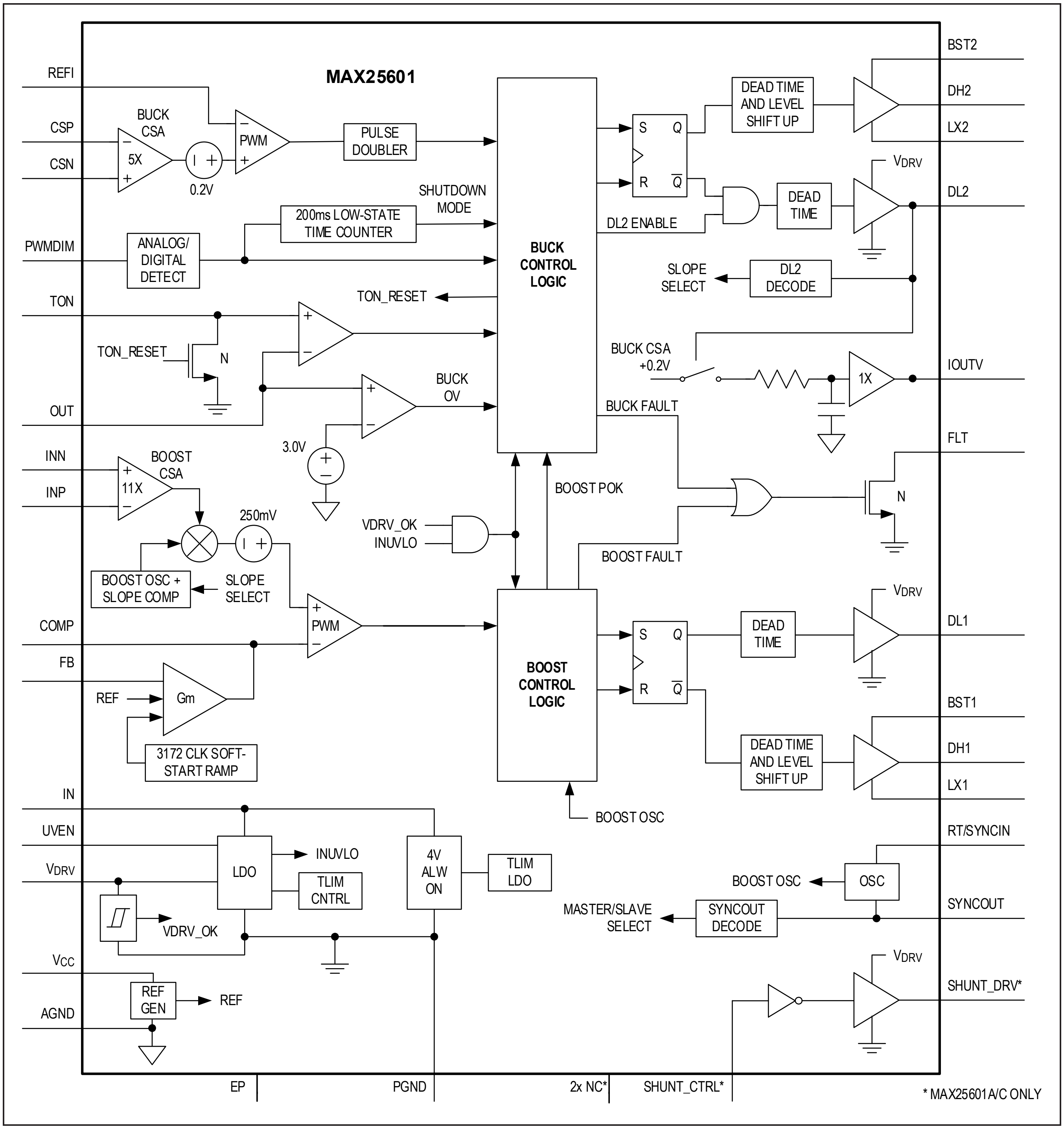
Pin Description (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>TQFN</th><th>TSSOP</th></tr>
<tr><td>15</td><td>16</td><td>IOUTV</td><td>Current Monitor output for the Buck LED controller. Connect a 100Ω resistor and 22nF capacitor from I_{OUTV} to AGND.
$V_{IOUTV} = I_{LED} \times R_{CS\_LED} \times 5 + 0.2$</td></tr>
<tr><td>16</td><td>17</td><td>TON</td><td>Frequency Setting Pin for the Buck. The buck switching frequency is set by a resistor from the input to the TON pin, a capacitor from the TON pin to AGND, and the resistor-divider on the OUT pin.
$F_{SW\_BUCK} = (R_{OUT2} + R_{OUT1})/(C_{TON}R_{TON}R_{OUT2})$</td></tr>
<tr><td>17</td><td>18</td><td>DIM</td><td>Dimming Input for Buck Regulator PWM Dimming.
Direct PWM dimming control: Connect to an external 3.3V or 5V PWM signal, with DIM frequency between 10Hz and 2kHz.
Analog-to-PWM dimming control: Connect to an analog voltage between 0.2V and 3V to set the PWM dimming duty cycle using the internal 200Hz clock.
Keep DIM above 3.2V for 100% duty cycle.</td></tr>
<tr><td>18</td><td>19</td><td>SYNCOUT</td><td>Sync Clock Output. 180-degree clock signal. Connect SYNCOUT to the RT/SYNCIN of a second MAX25601A/B/C/D to have it run at 180 degrees out of phase from this controller.
During startup, SYNCOUT is used to select the master/slave configuration for the boost regulator based on the following options:
<table>
<tr><th>SYNCOUT RESISTOR TO PGND</th><th>MASTER/SLAVE CONFIGURATION</th></tr>
<tr><td>35kΩ</td><td>Single-phase/dual-phase master</td></tr>
<tr><td>5kΩ</td><td>Dual-phase slave</td></tr>
</table></td></tr>
<tr><td>19</td><td>—</td><td>SHUNT_CTRL</td><td>PWM Input for SHUNT_DRV. PWM control input for the shunt driver.
<table>
<tr><th>SHUNT_CTRL</th><th>SHUNT_DRV</th><th>APPLICATION FUNCTION</th></tr>
<tr><td>Low</td><td>High</td><td>External FET on. HUD disabled (dimmed).</td></tr>
<tr><td>High</td><td>Low</td><td>External FET off. HUD enabled.</td></tr>
</table></td></tr>
<tr><td>20</td><td>20</td><td>RT/SYNCIN</td><td>Frequency Setting Pin for Boost Regulator. This pin sets the switching frequency of the boost regulator when driven by an external clock. or by using a resistor to AGND. When set by an external resistor, the switching frequency follows the equation:
$F_{SW\_BOOST} = 34.2 \times 10^9 / (R_T + 550)$
When using an external clock, drive SYNCIN with a 3.3V or 5V signal, between 200kHz and 2.2MHz, with a minimum off-time of 80ns. To shift SYNCOUT phase 180 degrees from SYNCIN, drive SYNCIN with a 50% duty cycle signal.</td></tr>
<tr><td>21</td><td>21</td><td>AGND</td><td>Analog Ground Connection. Low-noise ground pin.</td></tr>
<tr><td>22</td><td>22</td><td>VCC</td><td>Analog Power Supply. Connect to V_{DRV} through a series 10Ω resistor. Bypass V_{CC} to AGND with a 1µF ceramic capacitor.</td></tr>
</table>

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
23	23	FB	Feedback Input for the Boost Regulator. FB regulates to 1V, while the boost OVP threshold at FB is 1.2V. Connect a resistor-divider at FB to set the boost output voltage. $V_{OUT\_BOOST} = V_{FB}(R_{FB1} + R_{FB2})/R_{FB2}$ $V_{OVP\_BOOST} = V_{TH\_OVP\_BOOST}(R_{FB1} + R_{FB2})/R_{FB2}$
24	24	COMP	Compensation Pin for the Boost Regulator
25	25	$\overline{FLT}$	Fault Output Indicator. Buck and boost faults are reported on this pin. $\overline{FLT}$does not change state when DIM is low. Buck Faults: LED open, LED short, output overvoltage Boost Fault: Undervoltage
26	---	SHUNT_DRV	Shunt FET Driver Output. Connect SHUNT_DRV to the gate of an n-channel FET for dimming.
27	26	LX1	Switching Node of Boost Controller
28	27	BST1	High-Side Power Supply for High-Side Gate Drive of Boost Regulator. Connect a 0.1μF ceramic capacitor from BST1 to LX1, and a BST diode between V_{DRV} and BST2.
29	28	DH1	High-Side Driver of Boost Regulator. Connect to the gate of boost regulator's high-side n-channel MOSFET. Use series resistor to limit current slew rate and mitigate EMI noise, if necessary.
30	1	DL1	Low-Side Driver of Boost Regulator. Connect to gate of the boost regulator's low-side n-channel MOSFET. Use series resistor to limit current slew rate and mitigate EMI noise, if necessary.
31	2	INN	Negative Current-Sense Input for the Boost Regulator
32	3	INP	Positive Current-Sense Input for the Boost Regulator. The maximum differential voltage across INP and INN is 80mV (typ), and sets the peak input current limit.
EP	EP	EP	Exposed Pad. Connect EP to a large-area contiguous-copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to AGND.

Functional Block Diagram



Detailed Description

Input Voltage (IN)

The input supply pin (IN) is the input to the internal LDO, and must be locally bypassed with a minimum of 0.1μF capacitance close to the pin. All the input current drawn by the device goes through this pin. The positive terminal of the bypass capacitor must be placed as close as possible to this pin, and the negative terminal of the bypass capacitor must be placed as close as possible to the PGND pin.

V Regulator (VDRV)

A regulated 5V output is provided for driving the gates of the external MOSFETs and other external circuitry with a current up to 10mA. Bypass V_{DRV} to PGND with a minimum of 2.2μF ceramic capacitor, positioned as close as possible to the device. In certain applications when an external regulated 5V supply is available, the IN, V_{DRV} and V_{CC} pins can be connected together to the regulated 5V, saving the power dissipation in the internal regulator of the device.

Input Undervoltage/Enable (UVEN)

The device features adjustable UVLO using the enable input (UVEN). Connect UVEN to V_{IN_BOOST} through a resistive divider to set the UVLO threshold. The device is enabled when VUVEN exceeds the 1.24V (typ) threshold. UVEN also functions as an enable/disable input to the device. Drive UVEN low to disable the output and high to enable the output.

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. The high-side gate driver (DH) sources and sinks 1.5A, and the low-side gate driver (DL_) sources 1.0A and sinks 2.4A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET driver is powered by BST_, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply (VDRV).

High-Side Gate-Drive Supply (BST_)

The floating BST-LX capacitor provides the required supply for the high-side MOSFET. This capacitor is charged through the BST diode each time LX is pulled low.

Shunt Dimming (SHUNT_CTRL, SHUNT_DRV)

The MAX25601A/C includes an integrated gate driver for HUD dimming. This allows much faster on/off switching of the LEDs, enabling much wider dimming ratios up to 10,000.

A control signal at SHUNT_CTRL directly drives SHUNT_DRV. SHUNT_DRV is capable of driving n-channel MOSFETs with up to 10nC gate charge.

Thermal Shutdown

Internal thermal-shutdown circuitry is provided to protect the device in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 165°C with a 15°C hysteresis (both values typical). During thermal shutdown, the low- and high-side gate drivers are disabled.

Fault Indicator ($\overline{FLT}$)

The device features an active-low, open-drain fault indicator ($\overline{FLT}$). $\overline{FLT}$ asserts when one of the following conditions occur:

1) Buck overvoltage or open across the LED string
2) Buck short-circuit condition across the LED string
3) Boost undervoltage

Short-circuit condition across the LED string: When the LED string is shorted and the OUT pin voltage drops below the short threshold of 50mV for more than 1.2ms, the $\overline{FLT}$ pin goes low. During PWM dimming, the short detection is reported on the $\overline{FLT}$ pin only when DIM is high. Once $\overline{FLT}$ is asserted when the DIM is high, it stays asserted until the fault condition is removed.

Open LED detection: When the LED string is opened and the I_{OUTV} pin voltage drops to lower than 75% of the targeted voltage for more than 1.2ms, the $\overline{FLT}$ pin goes low. During PWM dimming, the open detection is reported on the $\overline{FLT}$ pin only when DIM is high. Once $\overline{FLT}$ is asserted when the DIM is high, it remains asserted until the fault condition is removed. The LED open detection works only when the REFI pin is greater than 325mV.

Overvoltage detection: When the voltage on the OUT pin exceeds the overvoltage threshold of 3V for more than 1.2ms, the $\overline{FLT}$ pin goes low. During PWM dimming, the overvoltage detection is reported on the $\overline{FLT}$ pin only when DIM is high. Once $\overline{FLT}$ is asserted when DIM is high, it remains asserted until the fault condition is removed.

Boost Controller

Boost Peak Current-Mode-Controlled Architecture

The MAX25601A/B/C/D offers peak current-mode control operation for best load-step performance and simpler compensation. The inherent feed-forward characteristic is especially useful in automotive applications where the input voltage changes quickly during cold-crank and load-dump conditions. While the current-mode architecture offers many advantages, there are some shortcomings. In high duty-cycle operation, subharmonic oscillations can occur. To avoid this, the device offers programmable internal slope compensation. To avoid premature turn-off at the beginning of the on-cycle, the current-limit and PWM comparator inputs have leading-edge blanking.

Loop Compensation

A transconductance amplifier in the voltage feedback path allows a simple type-2 configuration to compensate the loop. The appropriate poles and zeros are set by the external resistors and capacitors around the COMP output of the transconductance amplifier.

Slope Compensation

Slope compensation helps prevent subharmonic oscillations by decreasing any perturbation over subsequent switching cycles. The boost controller has internal slope compensation that is proportional to the selected switching frequency. Two options are available for selection based on the DL2 pin configuration at power on. The higher slope compensation setting is recommended for output voltages greater than 45V, while the lower setting is for output voltages less than 45V. The slope compensation is also automatically changed at appropriate input voltage thresholds as shown in Table 1.

Boost Switching Frequency (RT/SYNCIN)

The boost switching frequency can be set by a resistor from RT/SYNCIN to SGND, or driven externally by a PWM signal with a frequency between 200kHz and 2.2MHz. When set by an external resistor, the switching frequency follows the equation:

$$F_{SW\_BOOST}(kHz) = 37600/R_T(k\Omega)$$

When using an external clock, drive SYNCIN with a 3.3V or 5V signal, between 200kHz and 2.2MHz, with a minimum off-time of 80ns.

SYNCOUT

The SYNCOUT pin provides a 180-degree phase-shifted clock to the SYNCIN pin of another boost controller. When using an external clock, drive SYNCIN with a 50% duty cycle signal to shift SYNCOUT phase 180 degrees from SYNCIN.

Spread Spectrum

The boost controller has an internal spread-spectrum option to optimize EMI performance. The operating frequency is varied ±6%, centered on the oscillator frequency (F_{SW_BOOST}). The modulation signal is a triangular wave with a period of 1ms when the boost switching frequency is set to 400kHz. F_{SW_BOOST} ramps down -6% and ramps up +6% around 400kHz in 1ms. The cycle then repeats. The modulation period is inversely proportional to the boost switching frequency.

$$T_{SPREAD} = 1ms \times 400kHz / F_{SW\_BOOST}$$

The internal spread-spectrum function is disabled when using an external clock. Frequency dithering must then be done by the external clock.

Table 1. Slope Compensation Setting

DL2 RESISTOR	V_{IN_BOOST} THRESHOLD	SLOPE COMPENSATION (V/S)
100kΩ (Higher Slope Compensation)	< 8V	4.17x F_{SW_BOOST}
	8V-20V	2.08 x F_{SW_BOOST}
	> 20V	1.39 x F_{SW_BOOST}
30kΩ (Lower Slope Compensation)	< 8V	2.08 x F_{SW_BOOST}
	8V-20V	1.39 x F_{SW_BOOST}
	>20V	1.04 x F_{SW_BOOST}

Boost Output Voltage and Overvoltage Protection

The boost controller has programmable output voltage set by the resistor-divider at the FB pin. Overvoltage protection is 20% higher than the regulation voltage. The output voltage and overvoltage setpoints are defined by the following equations:

$$V_{OUT\_BOOST} = V_{FB} (R_{FB1} + R_{FB2})/R_{FB2}$$

$$V_{OVP\_BOOST} = V_{TH\_OVP\_BOOST} (R_{FB1} + R_{FB2})/R_{FB2}$$

where V_{FB} is 1V typ and $V_{TH\_OVP\_BOOST}$ is 1.2V typ in the *Electrical Characteristics* section.

If the output voltage reaches V_{OVP_BOOST}, the DH1 and DL1 pins are pulled low. The OVP circuit has a fixed hysteresis of 100mV before the driver attempts to switch again.

Multi phase Configurations

The boost controller can be configured for master or slave mode of operation in multiphase configurations. The modes are selected by the resistor value at the SYNCOUT pin. At power up, the resistor value is decoded during the 3ms power on initialization, and the selected configuration is latched.

Boost Output Undervoltage and Hiccup Operation

The boost controller includes output undervoltage protection. The boost controller must be in current limit when the boost output voltage drops below 70% of the setpoint to cause the boost controller to shut down and enter hiccup mode operation. Hiccup mode causes the boost controller to remain off during the hiccup period. The hiccup period is approximately 54ms when the boost switching frequency is set to 400kHz. The hiccup period is inversely proportional to the boost switching frequency.

$$t_{HICCUP\_BOOST} = 21504 / F_{SW\_BOOST}$$

Table 2. Multiphase Configuration

SYNCOUT RESISTOR	MASTER/SLAVE SELECTION
35kΩ	Single phase or multiphase master
5kΩ	Multiphase slave

Boost Soft-Start

The boost controller features a voltage soft-start to reduce inrush current. The soft-start time is approximately 9ms when the boost switching frequency is set to 400kHz. The soft-start time is inversely proportional to the boost switching frequency.

$$t_{SS\_BOOST} = 3712/F_{SW\_BOOST}$$

Buck Controller

Buck Average Current-Mode-Controlled Architecture

The buck controller uses a new average current-mode-control scheme to regulate the current in the output inductor of the buck LED driver. The inductor current is not directly sensed. Current is sensed across the low-side current-sense resistor (R_{CS_LED}) using the CSP and CSN pins, during the time when the synchronous FET is conducting. The voltage at REFI sets the regulation voltage for V(CSP-CSN).

In a buck converter operating in continuous-conduction mode, the average inductor current is the same as the output current. A pulse doubler is used to determine the on-time of the synchronous FET by doubling the time the inductor current is above the regulation threshold:

$$t_{OFF\_BUCK} = 2 \times t_{PW\_BUCK}$$

where t_{PW_BUCK} is the high-state pulse width of the internal comparator in the device.

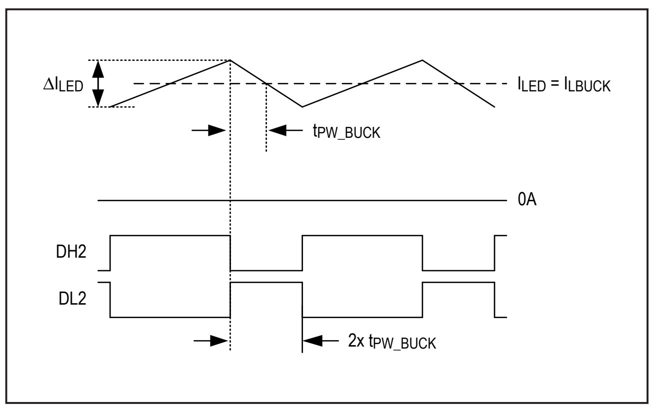


Figure 1. Buck Pulse Doubler

Buck Switching Frequency

The on-time is determined based on the external resistor (R_{TON}) connected between TON and the input voltage, in combination with a capacitor (C_{TON}) between R_{TON} and SGND pin. The input voltage and the R_{TON} resistor set the current sourced into the capacitor (C_{TON}), which governs the ramp speed. The ramp threshold is proportional to scaled-down feedback of the output voltage at the OUT pin. The proportionality of V_{OUT_BUCK} is set by an external resistor-divider (R_{OUT1}, R_{OUT2}) from V_{OUT}.

$$t_{ON\_BUCK}V_{IN\_BUCK}/R_{TON} = C_{TON}(V_{OUT\_BUCK}R_{OUT2}/(R_{OUT2} + R_{OUT1}))$$

In the case of a buck converter $t_{ON}V_{IN\_BUCK}$ is also given by:

$$t_{ON\_BUCK} = V_{OUT\_BUCK}/V_{IN\_BUCK}f_{SW\_BUCK}$$

where f_{SW_BUCK} is the switching frequency.

Based on that, the switching frequency in case of the new average current-mode-controlled architecture is given by:

$$f_{SW\_BUCK} = 1/K \text{ or } f_{SW\_BUCK} = (R_{OUT2} + R_{OUT1})/(C_{TON}R_{TON}R_{OUT2})$$

In the actual application, there will be slight variations in switching frequency due to the voltage drops in the switches and the inductor, the propagation delay from the t_{ON} input to the LX switching node, and the nonlinear current charging the t_{ON} capacitor. These effects have been ignored in the calculations for switching frequency.

Dimming (PWMDIM, REFI, SHUNT_CTRL, SHUNT_DRV)

The device supports both analog and PWM dimming of the LED. In analog dimming, the LED current is adjusted by the voltage on the REFI pin. In PWM dimming, dimming is achieved by repeatedly switching the LEDs on and off to achieve a lower effective brightness. Using the PWMDIM pin, PWM dimming can be achieved by driving a PWM signal on the PWMDIM pin, or by setting an analog voltage on the PWMDIM pin to use the internal 200Hz dimming oscillator. Using the SHUNT_CTRL pin, lower dimming duty cycles can be achieved by driving a PWM signal on the SHUNT_CTRL pin.

The PWMDIM pin must be set at its logic-high level when using PWM dimming through SHUNT_CTRL. The buck shuts down if the PWMDIM input is below the V_{DIM_OFS} for 210ms (to be confirmed).

Analog Dimming using REFI

The device has an analog dimming-control input (REFI). The voltage at REFI sets the LED current level when V_{REFI} ≤ 1.2V. For V_{REFI} > 1.3V, REFI is clamped to 1.3V (typ). The maximum withstand voltage of this input is 5.5V. The LED current is set to zero when the REFI voltage is at or below 0.18V typ. The LED current can be linearly adjusted from zero to full scale for the REFI voltage in the range of 0.2V to 1.2V.

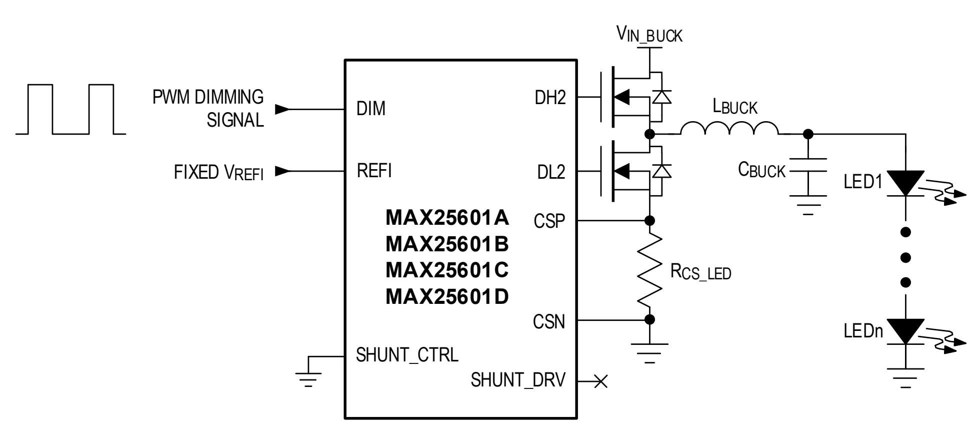


Figure 2. Analog Dimming using REFI

PWM Dimming using PWMDIM

The PWMDIM pin functions as the PWM dimming input of the buck. The PWMDIM pin can be driven with either an analog or PWM signal. This method of dimming repeatedly switches the buck regulator on and off to dim the LEDs. Minimum duty cycle is limited by the ramping up and down of the inductor current, which is determined by the inductor value, switching frequency, and input-to-output voltage ratio.

For PWM dimming with the PWM signal, drive the PWMDIM pin with an external PWM signal with a frequency between 10Hz and 2kHz to repeatedly switch the buck regulator on and off to dim the LEDs. When the PWMDIM signal is high, the switching of the synchronous MOSFETs in the buck LED driver is enabled. When the PWMDIM signal is low, both the high- and low-side MOSFETs are turned off. The LED current waveform is shown in Figure 4.

Analog-to-PWM Dimming: Set an analog voltage in the range of 0.2V ≤ V_{DIM} ≤ 3V on the PWMDIM pin. The IC compares the DC input voltage to an internally generated 200Hz ramp to pulse-width-modulate the buck.

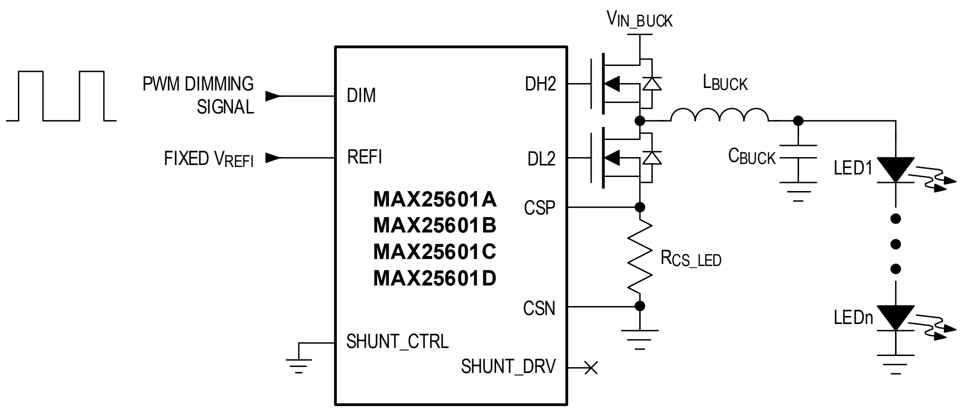


Figure 3. Digital PWMDIM Diming

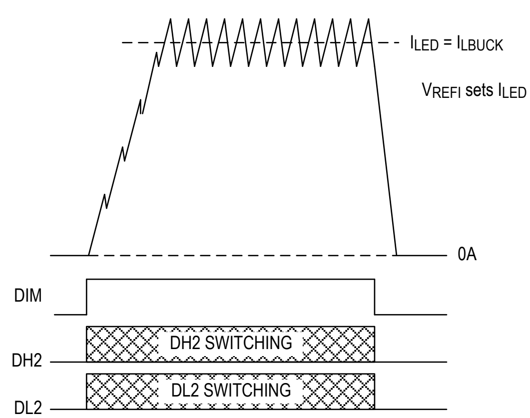


Figure 4. External PWM Dimming

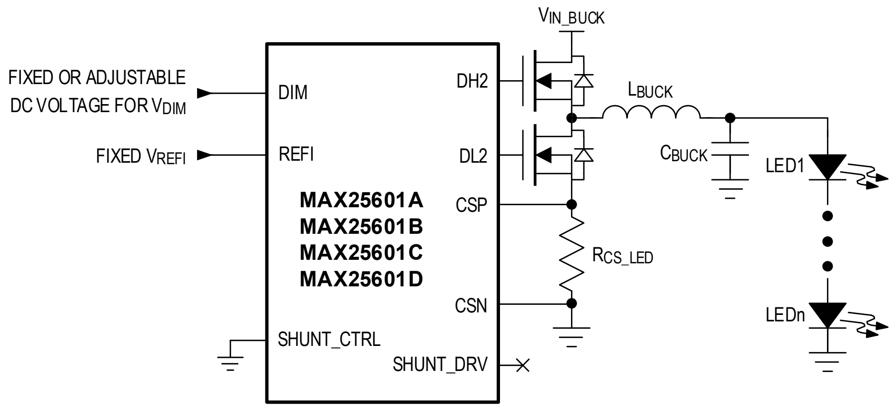


Figure 5. Analog-to-Digital PWMDIM Diming

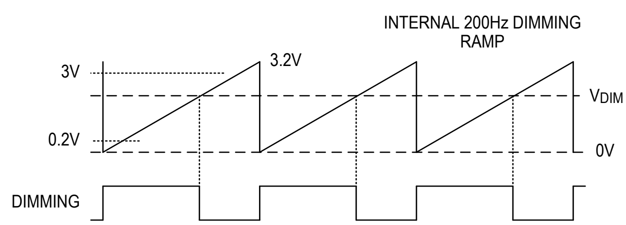


Figure 6. Analog-to-PWM Dimming

PWM Dimming using SHUNT_CTRL

The SHUNT_CTRL pin drives the SHUNT_DRV pin to control an external shorting FET. This provides extremely fast on/off switching of the LEDs that does not depend on the buck regulator startup or shutdown response, allowing for lower dimming duty cycles, and wider dimming range. Use a shorting FET with Q_G less than 10nC, and a low enough on-resistance to minimize power loss. Shunt dimming is typically used in HUD applications where the entire string is shorted out by the shunt. Shunt dimming can also be used in high-beam/low-beam applications in which the high-beam portion of the LED string is shorted out (disabled) by the shunt.

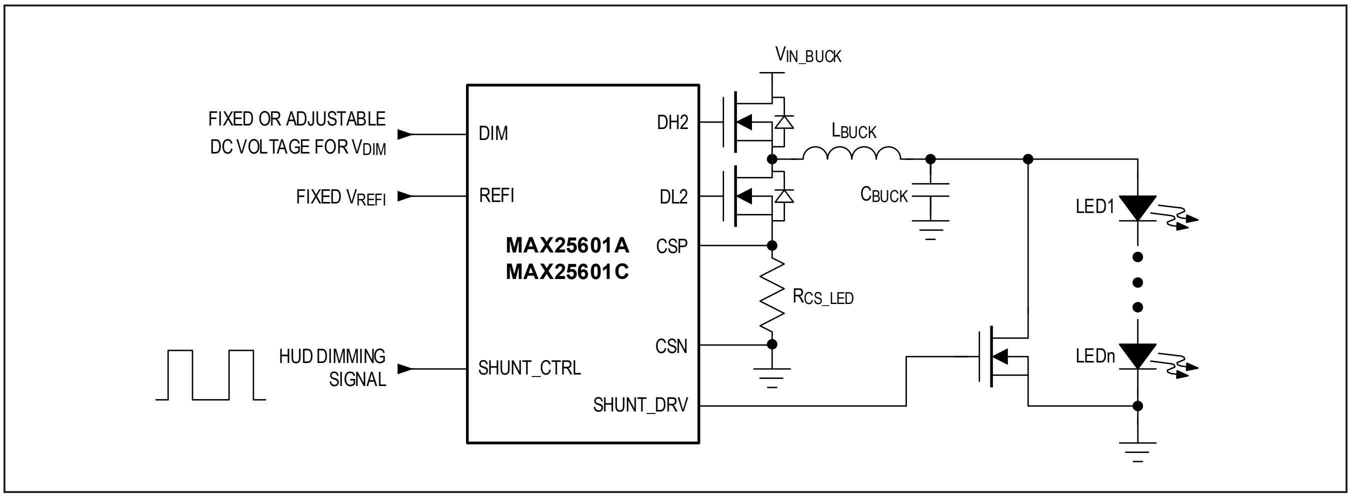


Figure 7. Shunt Dimming

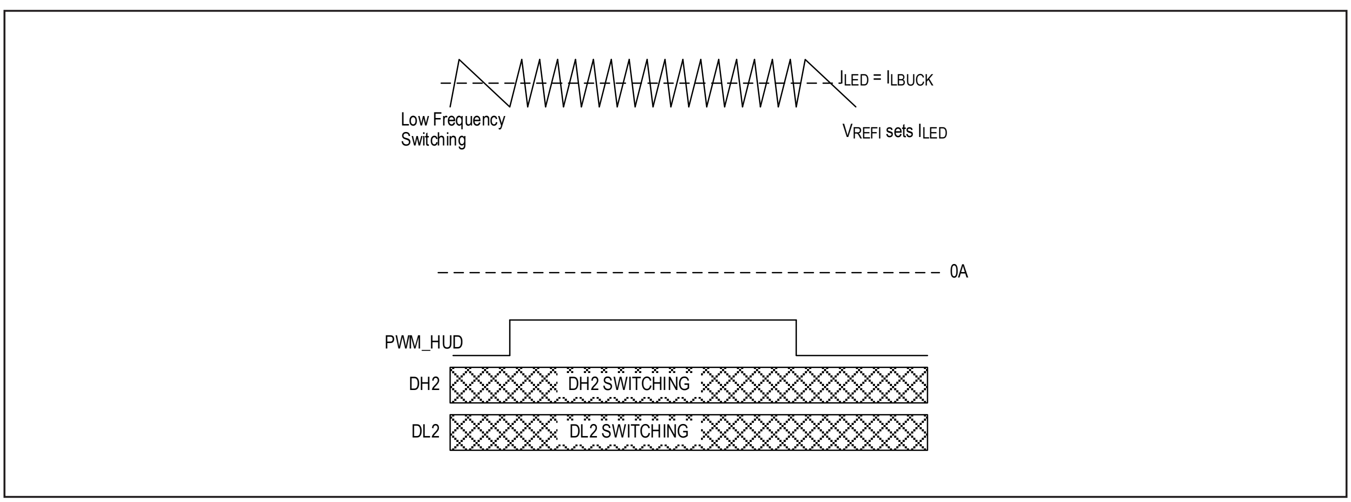


Figure 8. SHUNT_CTRL Dimming in HUD Applications

PWM Dimming by Shorting individual LEDs in the String

Extremely fast dimming of individual LEDs in the string can be acheived by applying a shorting FET across each LED, as shown in Figure 9. This application is used in matrix lighting where individual LEDs in the string are controlled by a shorting MOSFET across each LED. With this method, each LED in the string can be turned on and off without any impact on the brightness of the other LEDs in the string. If required, the entire string can be shorted at the same time while still maintaining current regulation in the inductor with minimal overshoot or undershoot. The rise and fall times of the currents in each LED are extremely fast. With this method, only the speed of the parallel-shunt MOSFET limits the dimming frequency and dimming duty cycle. Minimize the output capacitor (C_{BUCK}) to minimize current spikes due to the discharge of this capacitor into the LEDs when the shorting FETs are turned on. In some applications, this capacitor can be completely eliminated.

Buck Overvoltage Protection

The device has programmable overvoltage protection using the resistor-divider at the OUT pin. The overvoltage setpoint is defined by:

$$V_{OVP\_BUCK} = V_{TH\_OVP\_BUCK} (R_{OUT1} + R_{OUT2})/R_{OUT2}$$

where $V_{TH\_OVP\_BUCK}$ is 3V (typ) in the *Electrical Characteristics* section.

If the output voltage reaches V_{OVP_BUCK}, the DH2 and DL2 pins are pulled low to prevent damage to the LEDs or the rest of the circuit. The OVP circuit has a fixed hysteresis of 100mV before the driver attempts to switch again.

Buck Current Monitor (IOUTV)

The device includes a current monitor on the IOUTV pin. The IOUTV voltage is an analog voltage indication of the inductor current when PWMDIM is high. The current-sense signal on the bottom MOSFET across R_{CS_LED} is inverted and amplified by a factor of 5 by an inverting amplifier inside the device. An added offset voltage of 0.2V is also added to this voltage. This amplified signal goes through a sample and hold switch. The sample and hold switch is controlled by the DL2 signal. The sample-and-hold switch is turned on only when DL2 is high (and off when DL2 is low). This provides a signal on the output of the sample and hold that is a true representation of the inductor current when PWMDIM is high. The sample and hold signal passes through an RC filter and then the buffered output is available on the IOUTV pin. The voltage on the IOUTV pin is given by:

$$V_{IOUTV} = I_{LED} \times R_{CS\_LED} \times 5 + 0.2V$$

where I_{LED} is the LED current, which is the same as the average inductor current when PWMDIM is high. V_{IOUTV} indicates the same voltage when PWMDIM goes low as when PWMDIM was previously high.

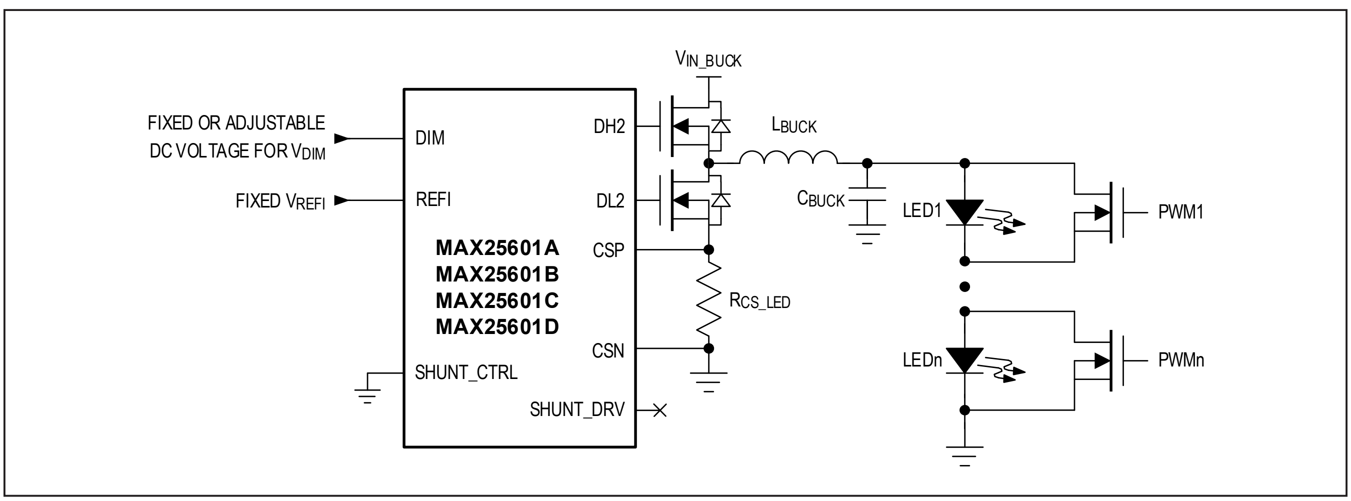


Figure 9. Matrix LED Dimming

Applications Information

Input Undervoltage/Enable

The minimum operating input voltage is set by the resistor-divider at UVEN.

$$V_{IN\_BOOST(MIN)} = V_{UVEN} (R_{UVEN1} + R_{UVEN2})/R_{UVEN2}$$

where V_{UVEN} is 1.24V (typ) in the *Electrical Characteristics* section.

Select R_{UVEN2} between 10kΩ and 50kΩ to minimize power loss.

Calculate R_{UVEN1} as follows:

$$R_{UVEN1} = (V_{IN\_BOOST(MIN)}/V_{UVEN} – 1) \times R_{UVEN2}$$

Boost Output Voltage and Power

As a pre-boost to the buck regulator, the boost output voltage and power requirements are determined by the buck regulator output voltage and power requirements. Establish these requirements with the equations below. These are then used in the subsequent boost calculation sections.

$$P_{OUT\_BOOST} = P_{IN\_BUCK} = (V_{OUT\_BUCK\_MAX} \times I_{LED})/\eta_{BUCK}$$

$$V_{OUT\_BOOST} = V_{IN\_BUCK} = V_{OUT\_BUCK\_MAX} / (1 – t_{ON\_MIN\_BUCK}/F_{SW\_BUCK})$$

where $V_{OUT\_BUCK\_MAX} = V_{LED} + I_{LED} \times R_{DYN}$ and η_{BUCK} is the buck efficiency, $t_{ON\_MIN\_BUCK}$ = 110ns max in the Electrical Characteristics, and F_{SW_BUCK} is the selected buck switching frequency.

Set the boost output voltage 20% above V_{IN_BUCK} to allow for boost output voltage transients and loadline. Calculate the required V_{OUT_BOOST} as follows:

$$V_{OUT\_BOOST} = 1.20 \times V_{IN\_BUCK}$$

$$I_{OUT\_BOOST} = P_{OUT\_BOOST}/ V_{OUT\_BOOST}$$

Boost Switching Frequency

Switching frequency is selected based on the tradeoffs between efficiency, solution size/cost, and the range of output voltage that can be regulated. Many applications place limits on switching frequency due to EMI sensitivity. Having selected the boost switching frequency, place a resistor from RT/SYNCIN to SGND based on the following equation:

$$R_T = (34.2\times10^9 /F_{SW\_BOOST}) – 550$$

If using an external clock, drive SYNCIN with a 3.3V or 5V signal, between 200kHz and 2.2MHz, with a minimum off-time of 80ns.

Boost Inductor Selection

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the equation below:

$$D_{MAX} = (V_{OUT\_BOOST} + VDS_{SYNC\_FET} + \Delta V_{IN\_RES} - V_{IN\_BOOST(MIN)})/(V_{OUT\_BOOST} + VDS_{SYNC\_FET} – VDS_{CTRL\_FET})$$

$$\Delta V_{IN\_RES} = I_{OUT\_BOOST} \times (R_{IN} + R_{DCR})$$

where V_{OUT_BOOST} and I_{OUT_BOOST} are determined in the *Boost Output Voltage and Power* section, $V_{IN\_BOOST(MIN)}$ is the minimum input supply voltage, and VDS_{CTRL_FET} and VDS_{SYNC_FET} are the average drain-to-source voltage of the boost control and synchronous FETs when they are on, and V_{IN_RES} is the voltage drop along the input current path.

Use an approximate value of 0.2V for VDS_{CTRL_FET} and VDS_{SYNC_FET} initially to calculate D_{MAX}. A more accurate value of the maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the following equations to calculate the maximum average inductor current ($I_{LBOOST(MAX)}$), peak-to-peak inductor current ripple (ΔI_{LBOOST}), and the peak inductor current (I_{IN_PK}) in amperes:

$$I_{LBOOST(MAX)} = I_{OUT\_BOOST}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔI_{LBOOST}, the peak inductor current is given by:

$$I_{LBOOST(PK)} = I_{LBOOST(MAX)} + 0.5 \times \Delta I_{LBOOST}$$

Select ΔI_{LBOOST} in the range of 0.2x to 0.4x of $I_{LBOOST(MAX)}$.

The inductance value (L) of inductor L_{BOOST} is calculated as:

$$L_{BOOST} = (V_{IN\_BOOST(MIN)} – \Delta V_{IN\_RES} - VDS_{CTRL\_FET}) \times D_{MAX}/(F_{SW\_BOOST} \times \Delta I_{LBOOST})$$

where F_{SW_BOOST} is the switching frequency, and other terms defined earlier. Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than I_{LPK} at the operating temperature.

Boost Input Current Sense

The boost input current sense is selected based on the required current limit at the peak inductor current.

$$R_{IN} = V_{ILIM\_BST} / I_{LBOOST(PK)}$$

where V_{ILIM_BST} is 72mV (min) in the *Electrical Characteristics* section, and I_{IN_PK} is determined in the *Boost Inductor Selection* section.

Boost Input and Output Capacitors

When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose 50% or more of their capacitance at their rated DC-voltage bias, and can also lose capacitance with extremes in temperature. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and operating temperature.

Boost Input Capacitor

The input current to a boost converter is almost continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and maximum ESR using the following equations:

$$C_{IN\_BOOST} = \Delta I_{LBOOST}/(4 \times F_{SW\_BOOST} \times \Delta V_{QPP})$$

$$ESR_{MAX} = \Delta V_{ESR}/\Delta I_{LBOOST}$$

ΔI_{LBOOST} is peak-to-peak inductor ripple current. ΔV_{QPP} is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_{QPP}) are equal when using a combination of ceramic and aluminium capacitors.

A large current is drawn from the input source during converter startup, especially at high output-to-input differential. The devices have an internal soft-start, but a larger input capacitor than calculated above may be necessary to avoid chattering due to finite hysteresis during startup.

Boost Output Capacitor

In a boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at lower duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to ESR while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak.

$$ESR = \Delta V_{ESR}/I_{OUT\_BOOST}$$

$$C_{OUT\_BOOST} = (I_{OUT\_BOOST} \times (1 - D_{MAX}))/(\Delta V_{QPP} \times F_{SW\_BOOST})$$

where I_{OUT_BOOST} is the output current, ΔV_{QPP} is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the ripple contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle (i.e., the duty cycle at the minimum input voltage). Low-ESR ceramic capacitors are suitable for lower output ripple and noise.

Since the buck input is taken from the boost output, the capacitance required is then the higher of the two requirements. See the Buck Input Capacitor Selection.

Boost Output Voltage and Overvoltage Setting

V_{OUT_BOOST} is set by the resistor-divider at FB.

$$V_{OUT\_BOOST} = V_{FB} (R_{FB1} + R_{FB2})/R_{FB2}$$

where V_{FB} is 1V (typ) in the *Electrical Characteristics* section.

Select R_{FB2} between 10kΩ and 50kΩ to minimize power loss.

Calculate R_{FB1} as follows:

$$R_{FB1} = (V_{OUT\_BOOST}/V_{FB} – 1) \times R_{FB2}$$

With R_{FB1} and R_{FB2} determined, calculate V_{OVP_BOOST}:

$$V_{OVP\_BOOST} = V_{TH\_OVP\_BOOST} (R_{FB1} + R_{FB2})/R_{FB2}$$

where $V_{TH\_OVP\_BOOST}$ is 1.2V (typ) in the *Electrical Characteristics* section.

Maximum Output/Input Ratio

The maximum boost output/input ratio is limited by the minimum off-time of the boost oscillator ($t_{OFF\_MIN\_BST}$).

$$(1 - D_{MAX})/F_{SW\_BOOST} = t_{OFF\_MIN\_BST}$$

Lower switching frequencies allow for higher D_{MAX}, and hence a higher output-to-input ratio. D_{MAX} can be roughly approximated as $(1 - V_{IN\_BOOST}/V_{OUT\_BOOST})$, or more accurately defined in the *Boost Inductor Selection* section.

Boost Controller Loop Compensation (COMP)

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in Figure 10. The power modulator has a DC gain set by g_{MC} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor ($C_{OUT\_}$), and its ESR. The loop response is set by the following equation:

$$G_{MOD} = g_{MC} \times R_{LOAD} \times \left(\frac{1-D}{2}\right) \times \left(\frac{1 + j\frac{f}{f_{zMOD}}}{1 + j\frac{f}{f_{pMOD}}}\right) \times \left(1 - j\frac{f}{f_{Rph\_zMOD}}\right)$$

where $R_{LOAD} = V_{OUT\_}/I_{LOUT(MAX)}$ in ohms and g_{MC} = $1/(A_{V\_CS\_}$ x $R_{DC})$ in S. $A_{V\_CS\_}$ is the voltage gain of the current-sense amplifier and is typically 11V/V. R_{DC} is the current-sense resistor in ohms.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT\_}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT\_}}$$

The right-half plane zero is at:

$$f_{Rph\_zMOD} = \frac{R_{LOAD}}{2\pi \times L} \times (1 - D) \times (1 - D)$$

When $C_{OUT\_}$ is composed of n identical capacitors in parallel, the resulting $C_{OUT\_}$ = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$/n. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor. The feedback voltage-divider has a gain of $GAIN_{FB\_} = V_{FB\_}/V_{OUT\_}$, where $V_{FB\_}$ is 1.005V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA}$ x $R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, which is 400μS (max), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 10MΩ (typ).

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB). Therefore:

$$f_{pEA} = \frac{1}{2\pi \times (R_{OUT,EA} + R_C) \times C_C}$$

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{p2EA} = \frac{1}{2\pi \times R_C \times C_C}$$

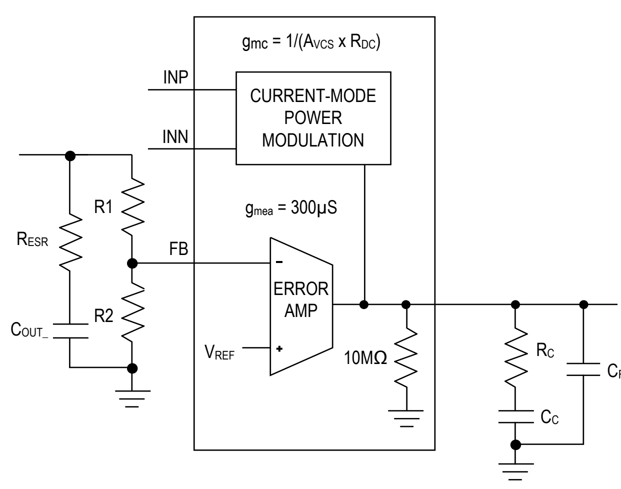


Figure 10. BOOST Controller Compensation Network

The loop gain crossover frequency (f_C) should be ≤ 1/3 of right-half plane zero frequency.

$$f_C \le \frac{f_{Rph\_zMOD}}{3}$$

At the crossover frequency, the total loop gain must be equal to 1. Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB\_}}{V_{OUT\_}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,\ EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB\_}}{V_{OUT\_}} \times g_{m,\ EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT\_}}{g_{m,\ EA} \times V_{FB\_} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP3 to AGND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

Multiphase/Parallel-Boost Configuration

A practical limit for a single-phase boost regulator is approximately 50W. This limitation is largely due to the losses in the power stage at low input voltages. While doubling the MOSFETs and inductors is possible, a more efficient solution is to add a second boost regulator that operates out of phase, dividing the losses between two phases, providing input and lower output-voltage ripple cancellation, and provide faster transient response.

The MAX25601A/B/C/D incorporates features that allow two or more boost regulators to operate in parallel. When two MAX25601A/B/C/D boost controllers are operated in parallel, the SYNCIN of the second MAX25601A/B/C/D can be driven by the SYNCOUT of the first MAX25601A/B/C/D for ideal 180-degree out-of-phase operation. When more than two boost regulators are used in parallel, an external clock is recommended to drive the SYNCIN pin of each regulator at the optimal phase separation of 360 degrees divided by the number of phases.

Dual-Phase Configuration

In the dual-phase configuration, one MAX25601A/B/C/D is set as the master (SYNCOUT = 30kΩ), while the other MAX25601A/B/C/D is set as a slave (SYNCOUT = 5kΩ). The transconductance amplifier of the slave is disabled in this configuration. The transconductance amplifier of the master provides the necessary compensation to the slave by connecting the COMP pins of the master and slave together.

Power-Up Sequence

The master and slave must be powered up together by tying the UVEN inputs together.

Buck Switching Frequency

Switching frequency is selected based on the tradeoffs between efficiency, solution size, solution cost, and the range of output voltage that can be regulated. Many applications place limits on switching frequency due to EMI sensitivity. The on-time of the MAX25601A/B/C/D's buck controller can be programmed for switching frequencies ranging from 100kHz up to 1MHz. This on-time varies in proportion to both input voltage and output voltage, as described in the *Buck Average Current-Mode-Controlled Architecture* section. However, in practice, the switching frequency shifts in response to large swings in input or output voltage. The maximum switching frequency is limited only by the minimum on-time and minimum off-time requirements. The switching frequency (F_{SW_BUCK}) is given by:

$$F_{SW\_BUCK} = (R_{OUT2} + R_{OUT1})/(C_{TON} R_{TON} R_{OUT2})$$

Choose C_{TON} between 100pF and 2.2nF. 470pF or 1nF are good choices. R_{OUT1} and R_{OUT2} are selected by the buck OVP requirement on the OUT pin. See the *Buck Overvoltage Setting* section. Rearranging the equation to solve for R_{TON}once the other component values are determined,

$$R_{TON} = (R_{OUT2} + R_{OUT1})/(C_{TON} R_{OUT2} f_{SW\_BUCK})$$

R_{TON} should be large enough so that at $V_{IN(MAX)}$, the voltage at the TON pin is < 50mV when the internal discharge FET is turned on.

$$R_{TON} > (V_{IN(MAX)} / 50mV – 1) \times 30\Omega$$

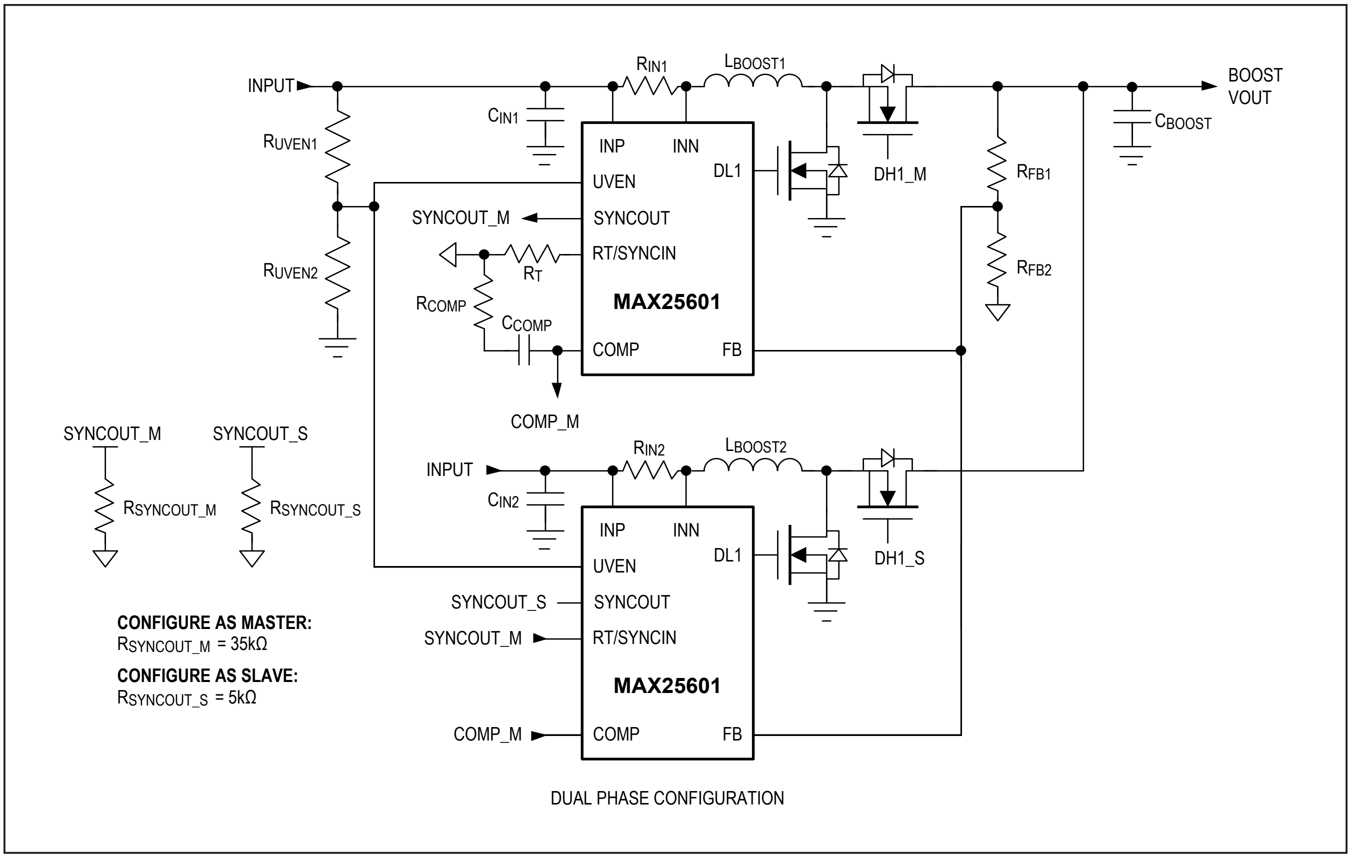


Figure 11. Dual-Phase Current-Sharing Configuration

Buck Overvoltage Setting

Overvoltage is typically set 20% higher than the maximum buck output voltage. The maximum buck output voltage is LED voltage.

$$V_{OUT\_BUCK\_MAX} = V_{LED} + I_{LED} \times R_{DYN}$$

$$V_{OVP\_OUT} = 1.2 \times V_{OUT\_BUCK\_MAX} = V_{TH\_OVP\_BUCK} (R_{OUT1}+R_{OUT2})/R_{OUT2}$$

where

V_{LED} is the maximum LED forward voltage of the LED string., I_{LED} is the maximum LED current, R_{DYN} is the total dynamic resistance of the LED string, and $V_{TH\_OVP\_BUCK}$ is 3V (typ) in the *Electrical Characteristics* section.

Select R_{OUT2} between 10kΩ and 50kΩ to minimize power loss.

Calculate R_{OUT1} as follows:

$$R_{OUT1} = ((1.2 \times V_{OUT\_BUCK\_MAX})/ V_{TH\_OVP\_BUCK} - 1)\ R_{OUT2}$$

Programming the LED Current

The LED current is programmed by the voltage on REFI when $V_{REFI} \leq 1.2V$ (analog dimming). The current is given by:

$$I_{LED} = (V_{REFI} - V_{CS\_OFS})/(5 \times R_{CS\_LED})$$

Rearranging the equation to solve for V_{REFI},

$$V_{REFI} = (I_{LED} \times 5 \times R_{CS\_LED}) + V_{CS\_OFS}$$

where V_{CS_OFS} is 0.2V (typ) in the *Electrical Characteristics* section.

Select R_{CS_LED} such that at the desired LED current, the voltage across R_{CS_LED} is in the 100mV to 200mV range, balancing signal-to-noise levels and power loss. Calculate the power loss in R_{CS_LED} and select a resistor with a higher power rating.

$$P_{LOSS} = I_{LED}^2 \times R_{CS\_LED} \times (1-D_{BUCK})$$

Buck Inductor Selection

The peak inductor current, selected switching frequency, and the allowable inductor-current ripple determine the value and size of the output inductor. Selecting a higher switching frequency reduces the inductance requirements, but at the cost of efficiency. The charge/discharge cycle of the gate capacitance of the external switching MOSFET's gate and drain capacitance create switching losses, which worsen at higher input voltages since the switching losses are proportional to the square of the input voltage. Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. High inductor-current ripple causes large peak-to-peak flux excursion, increasing the core losses at higher frequencies.

The peak-to-peak current-ripple values typically range from ±10% to ±40% of DC current (I_{LED}). Based on the LED current-ripple specification and desired switching frequency, the inductor value can be calculated as follows:

$$L = (V_{IN\_BUCK} - V_{OUT\_BUCK})\ t_{ON}/\Delta I_{LED}$$

where ΔI_{LED} is the peak-to-peak inductor ripple.

It is important to ensure that the rated inductor saturation current is greater than the worst-case operating current ($I_{LED}+\Delta I_{LED}/2$) under the wide operating temperature range.

Buck Input and Output Capacitors

When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose over 50% of their capacitance at their rated DC-voltage bias, and also lose capacitance with extremes in temperature. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature.

Buck Input Capacitor Selection

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. The input ripple consists of ΔV_{QPP} (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. A good starting point for selection of C_{IN} is to use an input-voltage ripple of 2% to 10% of V_{IN_BUCK}. C_{IN_MIN} can be selected as follows:

$$C_{IN\_MIN} = 2(I_{LED} \times t_{ON})/\Delta V_{IN\_BUCK}$$

where t_{ON} is the on-time pulse width per switching cycle.

As the buck input is taken from the boost output, the capacitance required is then the higher of the two requirements. See the Boost Output Capacitor Selection.

Buck Output Capacitor Selection

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance.

The output capacitance (C_{OUT_BUCK}) is calculated using the following equation:

$$C_{OUT\_BUCK} = ((V_{IN\_MIN\_BUCK} - V_{LED}) \times V_{LED}) / (\Delta V_R \times 2 \times L_{BUCK} \times V_{IN\_MAX\_BUCK} \times F_{SW\_BUCK}{}^2)$$

where ΔV_R is the maximum allowable voltage ripple.

Switching MOSFET Selection

The device requires two external n-channel MOSFETs for each switching regulator. The MOSFETs should have a voltage rating at least 20% higher than the maximum boost output voltage to ensure safe operation during the ringing of the switch node. In practice, all switching converters have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The MOSFETs should also have a current rating at least 50% higher than the average switch current. The total losses of the power MOSFETs in both high- and low-side MOSFETs should be estimated once the MOSFETs are chosen. The n-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. The conduction losses at minimum input voltage should not exceed MOSFET package thermal limits or violate the overall thermal budget. Also, ensure that the conduction losses plus switching losses at the maximum boost output voltage do not exceed package ratings or violate the overall thermal budget. In particular, check that the dV/dt caused by DH_ turning on does not pull up the DL_ gate through its drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

BST Capacitor Selection

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values (C_{BST} in the Typical Operating Circuit) according to the following equation:

$$C_{BST} = Q_G/\Delta V_{BST}$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST} = 100mV) when determining C_{BST}. Use a Schottky diode when efficiency is most important, as this maximizes the gate-drive voltage. If the quiescent current at high temperature is important, it may be necessary to use a low-leakage switching diode. The boost capacitor should be a low ESR ceramic capacitor. A minimum value of 100nF works in most cases. A minimum value of 220nF is recommended when using a Schottky diode.

Gate-Drive Power Loss

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Therefore, the power dissipation in the controller due to drive losses must be checked. MOSFETs must be selected so that their total gate charge is low enough, such that the gate total drive current is within the V_{DRV} LDO capability, and that the IC can power the drivers without overheating the device. The total power dissipated in the internal gate drivers of the device is given by:

$$P_{DRIVE} = V_{DRV} \times (QG_{HS\_BOOST} + QG_{LS\_BOOST}) \times F_{SW\_BOOST} + V_{DRV} \times (QG_{HS\_BUCK} + QG_{LS\_BUCK}) \times F_{SW\_BUCK}$$

where QG_{HS_BOOST} and QG_{HS_BUCK} are the high-side MOSFET gate charge, and QG_{LS_BOOST} and QG_{LS_BUCK} are the low-side MOSFET gate charge for the boost and buck, respectively.

The power dissipated in the 5V regulator in the device due to the gate drivers is given by:

$$P_{DIS} = V_{IN\_BOOST} \times (P_{DRIVE} / V_{DRV})$$

PCB Layout

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a dv/dt source; therefore, minimize the surface area of the heatsink as much as is compatible with the MOSFET power dissipation, or shield it. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large continuous copper plane under the IC package. Ensure that all heat-dissipating components have adequate cooling.
2) Isolate the power components and high-current path from the sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops, power traces, and load connections short:
    a) Keep the high-side and low-side FETs, input and output capacitors, and inductors close together for each regulator.
    b) Keep the LX area as small as possible.
    c) Place the boost capacitor (C_{BST}) as close as possible to the BST and LX pins.
    d) Follow the EV kit layout example.
4) Route high-speed switching nodes and high-voltage switching nodes away from the sensitive analog areas. High-speed gate-drive signals can generate significant conducted and radiated EMI. This noise can couple with high-impedance nodes of the IC and result in undesirable operation. A low-value resistor (4 to 10Ω at R_{DH} and R_{DL}), in series with the gate-drive signals, are recommended to slow the slew rate of the LX_ node and reduce the noise signature. They also improve the robustness of the circuit by reducing the noise coupling into sensitive nodes.

5) Use thick-copper PCBs (2oz rather than 1oz) to enhance full-load efficiency.
6) Connect PGND and SGND to a star-point configuration. Use an internal PCB layer for the PGND and SGND plane as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.
7) The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heatsink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the device to additional ground planes within the circuit board.
8) The parasitic capacitance between switching node and ground node should be minimized to reduce common-mode noise. Other common layout techniques, such as star ground and noise suppression using local bypass capacitors, should be followed to maximize noise rejection and minimize EMI within the circuit.

Dual-Phase Boost PCB Layout

1) It is important that the inputs of both regulators are very close together. Place the input current-sense resistors side by side, immediately after the input ceramic capacitors, to ensure a common point and input sense.
2) Place the controller such that the input current sense traces are < 1.5in long.
3) The FB resistor should sense the boost output voltage at the mid-point between both outputs so that the ripple is symmetrical.
4) Connect COMP and AGND of both ICs together. The traces should be well shielded and ground referenced, and placed away from any noise sources and fast-switching signals

Typical Application Circuits

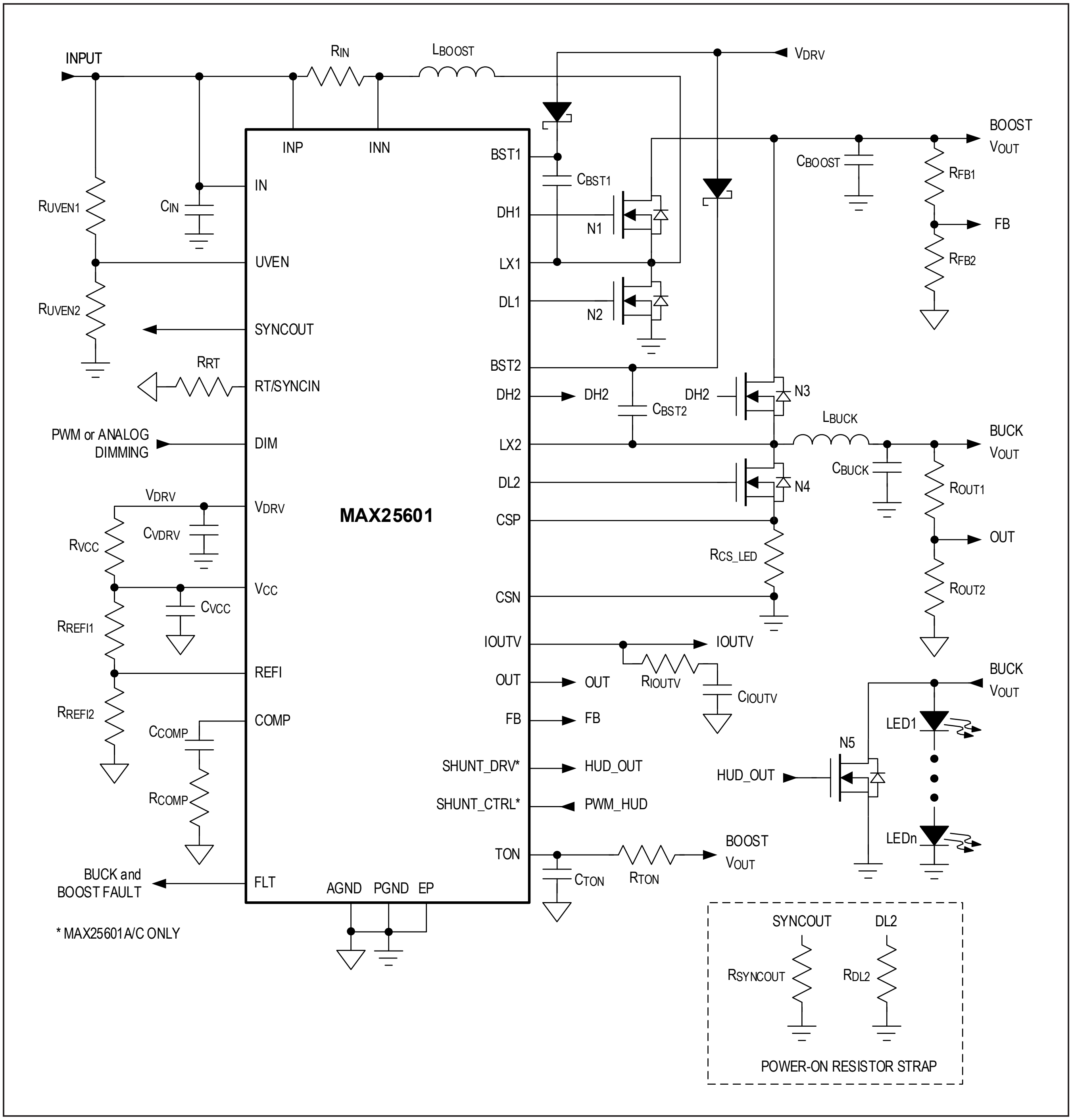


Table 3. Typical Application Example

		CASE 1	CASE 2	CASE 3
		High F_{SW},	Low F_{SW},	Low F_{SW},
		Low Power	Low Power	High Power
V_{IN} Typical Operating Range	V	8V to 16V	8V to 16V	8V to 16V
V_{IN} UV Setting	V	7V	7V	7V
Boost Fsw	Hz	2MHz	400kHz	400kHz
Buck Fsw	Hz	750kHz	750kHz	750kHz
n_{LED}		8	8	12
V_{LED} (max)	V	3.25V	3.25V	3.25V
V_{OUT} Buck	V	26V	26V	39V
I_{LED}	A	1A	1A	1.5A
P_{OUT}	W	26W	26W	58.5W
V_{OUT} Boost Output Voltage (margin Buck Dmax - 20%)	V	35V	35V	55V
BOOST POWER STAGE				
L_{BOOST}	H	3.3µH	10µH	10µH
Boost Control FET	N2	BUK9Y59-60E (59mΩ, 6.1nC Qg)	SQJ464EP (20mΩ, 7.35nC Qg)	SQJA84EP (11.2mΩ, 21nC Qg)
Boost Sync FET	N1	BUK9Y59-60E (59mΩ, 6.1nC Qg)	BUK9M19-60E (19mΩ, 13.8nC Qg)	BUK9Y25-80E (27mΩ, 17.1nC Qg)
C_{OUT} Boost	F	2x 22µF/ 5mΩ	2x 22µF/5mΩ	2x 22µF/5mΩ
		(derate 50%)	(derate 50%)	(derate 50%)
Compensation		50kΩ/1nF	50kΩ/1nF	50kΩ/1nF
R_{IN}	Ω	10mΩ	10mΩ	5mΩ
BUCK POWER STAGE				
L_{BUCK}	H	39µH	39µH	39µH
Buck Control FET	N3	BUK9Y52-60E dual (55mΩ, 5.6nC Qg)	BUK9Y52-60E dual (55mΩ, 5.6nC Qg)	BUK9Y72-80E (78mΩ, 7.9nC Qg)
Buck Sync FET	N4	BUK9Y52-60E dual (55mΩ, 5.6nC Qg)	BUK9Y52-60E dual (55mΩ, 5.6nC Qg)	BUK9Y72-80E (78mΩ, 7.9nC Qg)
C_{OUT} Buck	F	1x1µF	1x1µF	1x1µF
		(derate 50%)	(derate 50%)	(derate 50%)
R_{CS_LED}	Ω	150mΩ	150mΩ	100mΩ

Ordering Information

PART	PIN-PACKAGE	FEATURE	FEATURE
MAX25601AATJ/VY+	32 TQFN-EP (SW)*	With HUD Driver	36V
MAX25601BAUI/V+	28 TSSOP-EP*	No HUD Driver	36V
MAX25601CATJ/VY+	32 TQFN-EP (SW)*	With HUD Driver	48V
MAX25601DAUI/V+	28 TSSOP-EP*	No HUD Driver	48V

Note: *All parts operate over the -40°C to +125°C automotive temperature range.*
/V denotes an automotive-qualified part.
Y denotes side-wettable package.
+ denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed Pad*
(SW) = Side-Wettable.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/19	Initial release	—
1	7/19	Updated title from MAX25601 to MAX25601A/MAX25601B	1–32
2	9/19	Updated title from MAX25601A/MAX25601B to MAX25601A/MAX25601B/ MAX25601C/MAX25601D	1–32
3	1/20	Removed all remaining future-product indications from *Ordering Information* section	32

