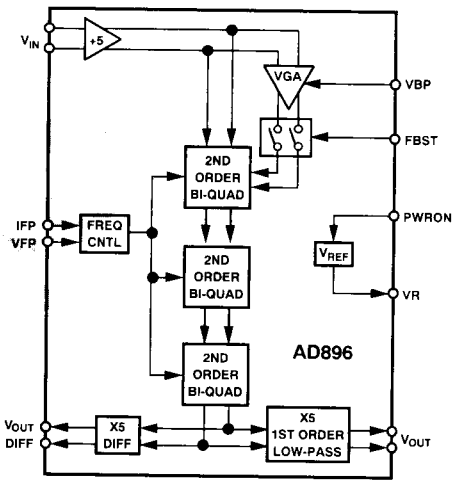
Fully Programmable Filter

AD896

FEATURES
7th Order Bessel Filter
Programmable Characteristics
Cutoff Frequency
Boost Amplitude
Two Versions
13 MHz Max Cutoff Frequency AD896-13
23 MHz Max Cutoff Frequency AD896-23
Fully Differential Data Path
±10% Cutoff Frequency Accuracy
750 ps Group Delay Variation
Power-Down Function
16-Pin SOIC, Plastic DIP
+5 V Supply

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD896 is a seventh order Bessel filter with a programmable cutoff frequency and equalization/boost. The seventh order Bessel function provides excellent group delay characteristics making it ideal for applications requiring time domain signal integrity, such as in disk drive read channels. Group delay flatness for the AD896 is specified at ±750 ps over its complete operating range. The programmable equalization/boost function is implemented by a "$1-kS^2$" providing up to 9 dB boost. Since the "$1-kS^2$" function provides for two real and complementary zeros, it does not impact the group delay characteristics.

The AD896 signal path is completely differential for both the low-pass normal and differentiated signals. The normal and differentiated outputs have matched delays to ensure time coherency. By providing time coherent low-passed and differentiated signals, the AD896 easily replaces discrete low-pass filters and differentiators for most data qualification schemes in disk drive read channels.

With the advent of constant density recording, programmability of cutoff frequency and equalization/boost becomes a must. Programmability of the AD896 is easily achieved through analog control lines: IFP, VFP and VBP. The analog control lines may be readily interfaced with DACs for ultimate system flexibility.

Also, the equalization/boost function is enabled through a separate control line, FBST.

The AD896 also provides a power management capability. A separate control line provides the "power-up" function which enables the chip (logic level high) during read mode and disables (logic level low) it for power savings during write or idle mode. Power dissipation during idle mode is a low 50 mW.

The AD896 is available in a 16-pin narrow body SOIC, and plastic DIP; it is also specified to operate over the commercial (0°C to +70°C) temperature range.

AD896—SPECIFICATIONS

AD896-13 (@ 0°C ≤ T_A ≤ +70°C, 4.50 V ≤ V_{CC} ≤ 5.50 V)

Parameter		Conditions	Min	Typ	Max	Units
Filter						
FC	Filter Cutoff Frequency	FC = 16.25 MHz/mA × (IFP)	5		13	MHz
FCA	Filter Cutoff Frequency Accuracy	FC = 13 MHz	−10		+10	%
AO	V_{OUT} Norm Differential Gain	F = 0.67 FC, FB = 0 dB	0.8		1.2	V/V
AD	V_{OUT} Diff Differential Gain	F = 0.67 FC, FB = 0 dB	0.8AO		1.0AO	V/V
FB	Frequency Boost at FC	$FB(dB) = 20\ Log\left[1.884 \times \frac{(VBP)}{(VR)} + 1\right]$		9.2		dB
FBA	Frequency Boost Accuracy	FB = 9 dB	−1		+1	dB
TGDO	Group Delay Variation	0 dB ≤ FB ≤ 9.2 dB	−0.75		+0.75	ns
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
RIN	Filter Diff Input Resistance		3.0			kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differential Output	BW = 100 MHz, R_S = 50 Ω		5.5		mV rms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, R_S = 50 Ω		2.5		mV rms
IO−	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance				60	Ω
VR	Reference Voltage		2.0		2.4	V
IFP	Frequency Program Current	VR = 2.2 V	0.31		0.8	mA
VFP	Frequency Program Current	I_{VFP} = 0.33 × VR/RX, VR = 2.2 V[1]	0.31		0.8	mA
Logic Levels		TTL Inputs (PWRON, FBST)				
V_{IL}			−0.3		0.8	V
V_{IH}			2.0		V_{CC}+0.3	V
I_{IL}		V_{INPUT} = 0.8 V			−1.5	mA
I_{IH}		V_{INPUT} = 2.7 V			20	μA
Power Supply Requirements						
Supply Voltage V_{CC}			4.5	5.0	5.5	V
Supply Current I_{CC}		PWRON = 0.8 V		10	13	mA
		PWRON = 2.0 V		60	78	mA
Absolute Maximum Ratings[2]						
Supply Voltage V_{CC}					7.5	V
Storage Temperature Range			−65		+150	°C
Operating Temperature Range[3]			0		+70	°C
Lead Temperature Range		Soldering 60 Sec			300	°C

NOTES

[1]RX is a series resistance placed between VR and VFP. The voltage difference between VR and VFP is .33 × VR.

[2]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[3]16-Pin Narrow Body SOIC Package θ_{JA} = 105°C/Watt

16-Pin Plastic DIP Package: θ_{JA} = 170°C/Watt.

Specifications subject to change without notice.

AD896-23 (@ 0°C ≤ T_A ≤ +70°C, 4.50 V ≤ V_{CC} ≤ 5.50 V)

Parameter		Conditions	Min	Typ	Max	Units
Filter						
FC	Filter Cutoff Frequency	FC = 28 MHz/mA × (IFP)	8.7		22.5	MHz
FCA	Filter Cutoff Frequency Accuracy	FC = 13 MHz	−10		+10	%
AO	V_{OUT} Norm Differential Gain	F = 0.67 FC, FB = 0 dB	0.8		1.2	V/V
AD	V_{OUT} Diff Differential Gain	F = 0.67 FC, FB = 0 dB	0.8AO		1.0AO	V/V
FB	Frequency Boost at FC	$FB(dB) = 20\ Log\left[1.884 \times \frac{(VBP)}{(VR)} + 1\right]$		9.2		dB
FBA	Frequency Boost Accuracy	FB = 9 dB	−1		+1	dB
TGDO	Group Delay Variation	0 dB ≤ FB ≤ 9.2 dB	−0.75		+0.75	ns
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
RIN	Filter Diff Input Resistance		3.0			kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differential Output	BW = 100 MHz, R_S = 50 Ω		5.5		mV rms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, R_S = 50 Ω		2.5		mV rms
IO−	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance				60	Ω
VR	Reference Voltage		2.0		2.4	V
IFP	Frequency Program Current	VR = 2.2 V	0.31		0.8	mA
VFP	Frequency Program Current	I_{VFP} = 0.33 × VR/RX, VR = 2.2V[1]	0.31		0.8	mA
Logic Levels		TTL Inputs (PWRON, FBST)				
V_{IL}			−0.3		0.8	V
V_{IH}			2.0		V_{CC}+0.3	V
I_{IL}		V_{INPUT} = 0.8 V			−1.5	mA
I_{IH}		V_{INPUT} = 2.7 V			20	μA
Power Supply Requirements						
Supply Voltage V_{CC}			4.5	5.0	5.5	V
Supply Current I_{CC}		PWRON = 0.8 V		10	13	mA
		PWRON = 2.0 V		75	95	mA
Absolute Maximum Ratings[2]						
Supply Voltage V_{CC}					7.5	V
Storage Temperature Range			−65		+150	°C
Operating Temperature Range[3]			0		+70	°C
Lead Temperature Range		Soldering 60 Sec			300	°C

NOTES

[1]RX is a series resistance placed between VR and VFP. The voltage difference between VR and VFP is .33 × VR.

[2]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[3]16-Pin Narrow Body SOIC Package θ_{JA} = 105°C/Watt

16-Pin Plastic DIP Package: θ_{JA} = 170°C/Watt.

Specifications subject to change without notice.

AD896-13—Typical Characteristics

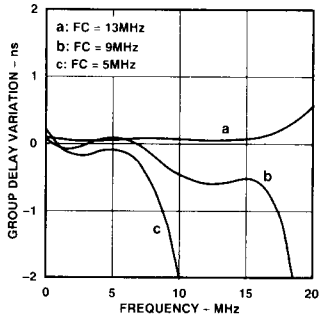

Figure 1. Normal Output Group Delay Variation vs. Frequency

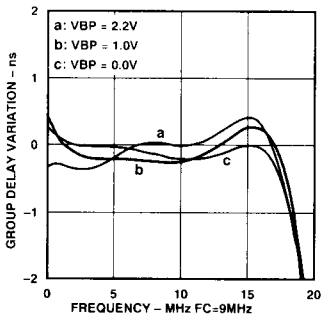

Figure 2. Normal Output Group Delay Variation vs. Frequency with Boost

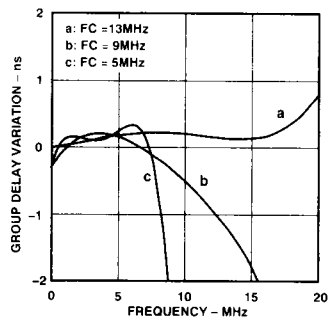

Figure 3. Differentiated Output Group Delay Variation vs. Frequency

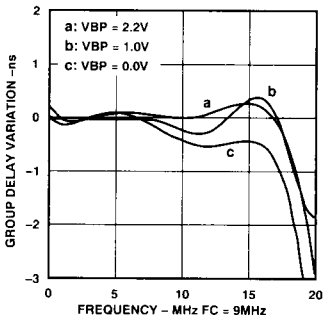

Figure 4. Differentiated Output Group Delay Variation vs. Frequency with Boost

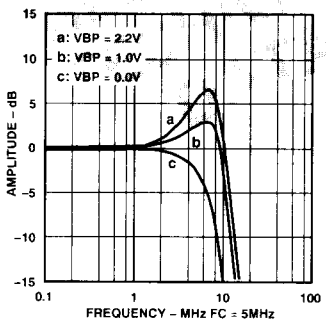

Figure 5. Normal Output Frequency Response with Boost

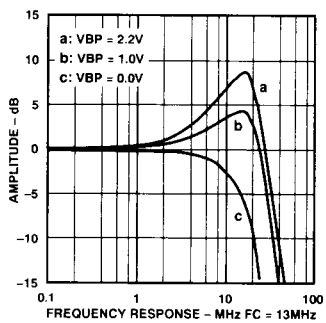

Figure 6. Normal Output Frequency Response with Boost

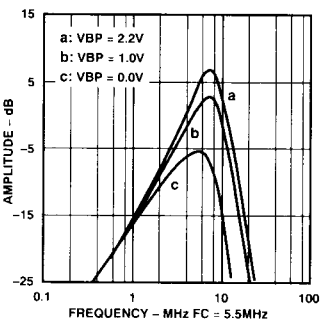

Figure 7. Differentiated Output Frequency Response with Boost

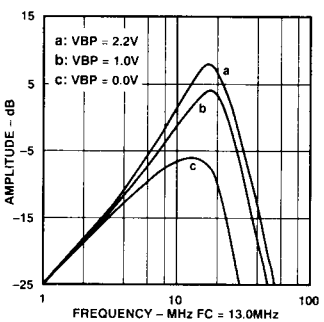

Figure 8. Differentiated Output Frequency Response with Boost

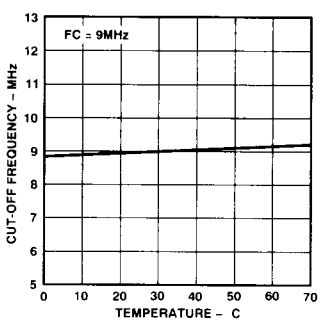

Figure 9. Cutoff Frequency vs. Temperature

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

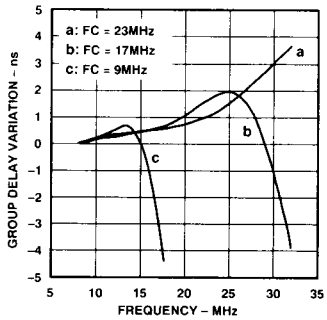

Figure 10. Normal Output Group Delay Variation vs. Frequency

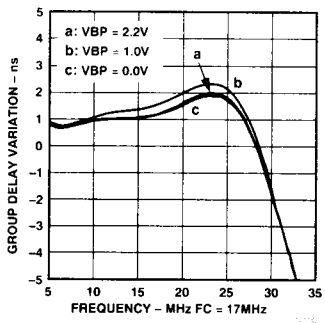

Figure 11. Normal Output Group Delay Variation vs. Frequency with Boost

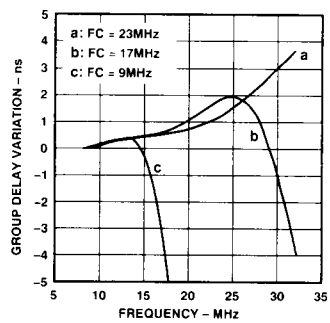

Figure 12. Differentiated Output Group Delay Variation vs. Frequency

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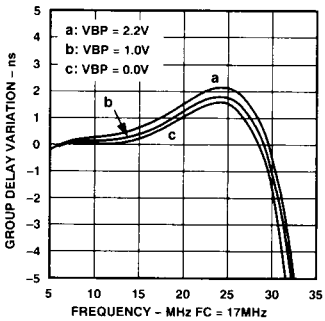


Figure 13. Differentiated Output Group Delay Variation vs. Frequency with Boost

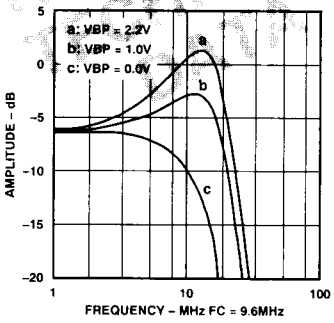


Figure 14. Normal Output Frequency Response with Boost

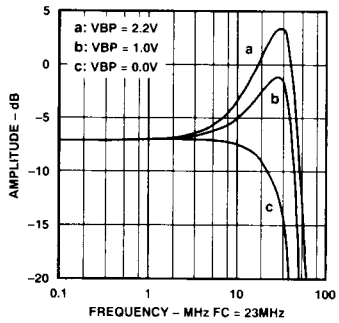


Figure 15. Normal Output Frequency Response with Boost

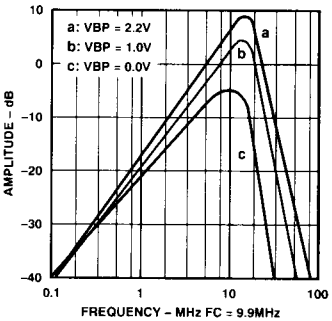


Figure 16. Differentiated Output Frequency Response with Boost

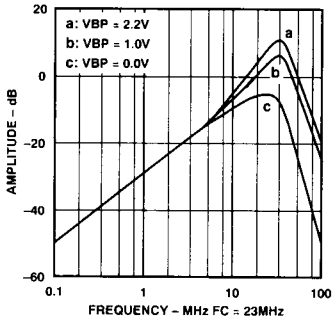


Figure 17. Differentiated Output Frequency Response with Boost

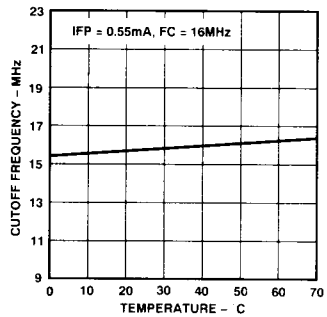
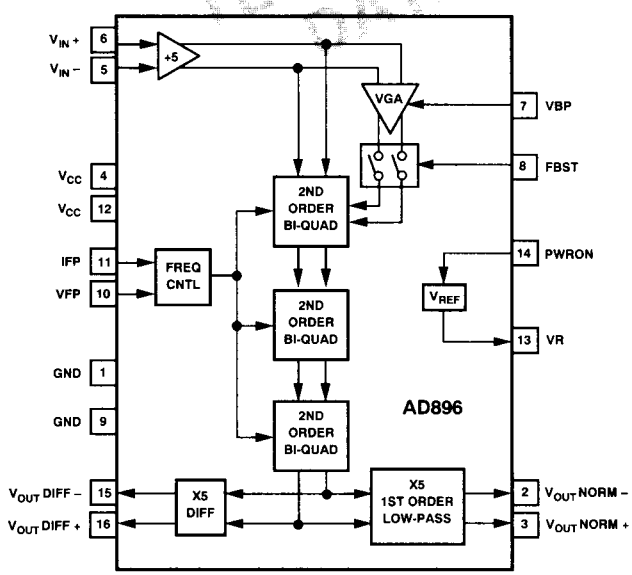


Figure 18. Cutoff Frequency vs. Temperature

Pin	Description	I/O Type	Application Notes
1	Ground	Power Input	
2	V_{OUT} NORMAL (Neg)	Analog Voltage Output	Low-Pass Filter Output, AC Couple
3	V_{OUT} NORMAL (Pos)	Analog Voltage Output	Low-Pass Filter Output, AC Couple
4	V_{CC} (+5 V dc)	Power Input	Decoupling with 0.1 μF‖0.01 μF Capacitors Required
5	V_{IN} (Neg)	Analog Voltage Input	Filter Input, Biased at V_{REF}, AC Couple Signal into Pin
6	V_{IN} (Pos)	Analog Voltage Input	Filter Input, Biased at V_{REF}, AC Couple Signal into Pin
7	VBP	Analog Voltage Input	Voltage to Set Amount of Boost
8	FBST	TTL Compatible Input	Boost/Equalizer Switch: Enabled (High Level), Disabled (Low Level)
9	Ground	Power Input	
10	VFP	Analog Current Input	Set Filter Cutoff Frequency. If VFP Is Used Leave IFP Floating
11	IFP	Analog Current Input	Set Filter Cutoff Frequency. If IFP Is Used Leave VFP Floating.
12	V_{CC} (+5 V dc)	Power Input	Decoupling with 0.1 μF‖0.01 μF Capacitors Required
13	VR	Voltage Output	Internally Generated Reference Voltage (2.2 V)
14	PWRON	TTL Compatible Input	Power-Up (High Level) or Power-Down (Low Level) the Chip
15	V_{OUT} DIFFERENTIATED (Neg)	Analog Voltage Output	Differentiated Output, AC Couple
16	V_{OUT} DIFFERENTIATED (Pos)	Analog Voltage Output	Differentiated Output, AC Couple

PIN CONFIGURATIONS



ORDERING GUIDE

Model	Description	Package Option*
AD896JR-13N	Narrow Body 16-Pin SOIC	R-16A
AD896JN-13	Plastic 16-Pin DIP	N-16
AD896JR-23N	Narrow Body 16-Pin SOIC	R-16A
AD896JN-23	Plastic 16-Pin DIP	R-16

*N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

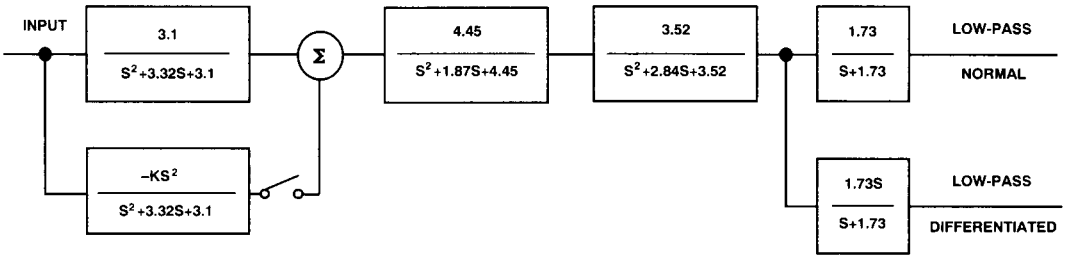


Figure 19. Block Diagram

FILTER OPERATION

The AD896 performs a seventh order Bessel function approximation by cascading three bi-quad sections and a single pole section to produce the normal low-pass output. The differentiated output is produced by placing a single zero, single pole section in parallel with the normal output single pole section. The architecture implemented in the AD896 ensures no time delay differential between the normal low-pass and the differentiated output. This is an important characteristic for data qualification schemes which depend on time coherency between the low-pass normal and differentiated read back signals. The normalized block diagram for the AD896 is shown in Figure 19.

The programmability of the AD896 is made possible by using variable transconductance amplifiers in the bi-quad sections to produce tunable amplifiers. The transconductivity (Gm) of each amplifier is changed by varying the current ratios in different stages of the amplifier. By varying the transconductance (Gm) the amplifier can be "tuned" to different frequencies. With the use of the tunable amplifiers in the bi-quad sections the cutoff frequency of the AD896 can be changed without changing external components or altering the approximation of the Bessel function. This makes the AD896 ideal for use in applications where programmable cutoff frequencies are desired.

The cutoff frequency of the AD896 is programmed by a control current which is used to tune the bi-quad sections. This control current can be applied directly to IFP or by connecting a voltage source in series with a resistor to VFP. By using a DAC the cutoff frequency can be microprocessor controlled (see application Figures 26 and 27).

Figure 20 and 21 are plots of IFP current versus cutoff frequency for the AD896-13 and AD896-23 respectively. Because the AD896 uses current to control the cutoff frequency of the filter the supply current varies with the setting of the cutoff frequency. Figure 22 and 23 illustrate the relationship between cutoff frequency and supply current for the AD896-13 and AD896-23, respectively.

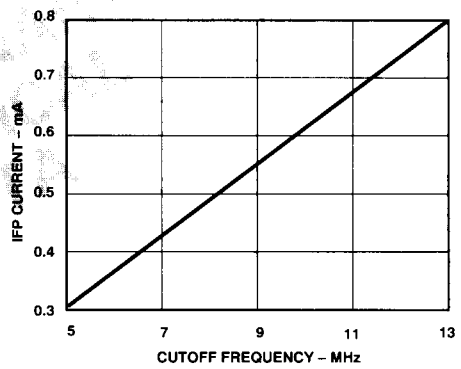


Figure 20. AD896-13 IFP Current vs. Cutoff Frequency

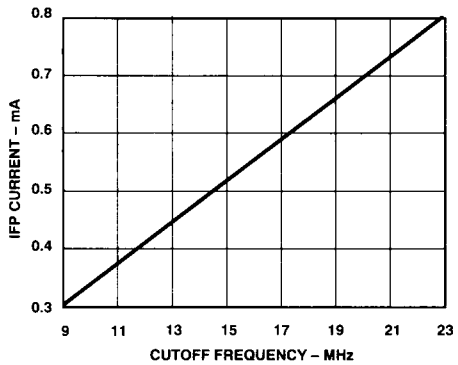


Figure 21. AD896-23 IFP Current vs. Cutoff Frequency

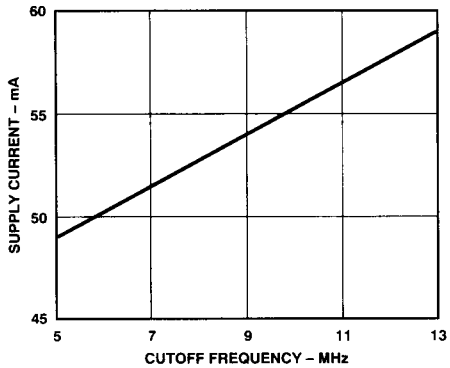


Figure 22. AD896-13 Supply Current vs. Cutoff Frequency

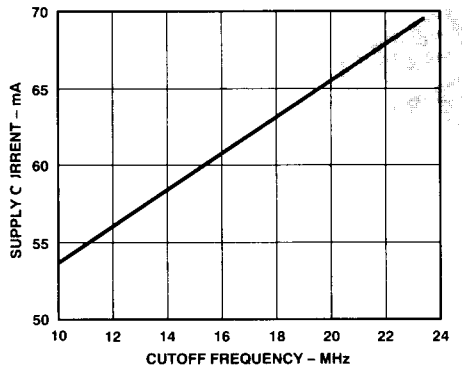


Figure 23. AD896-23 Supply Current vs. Cutoff Frequency

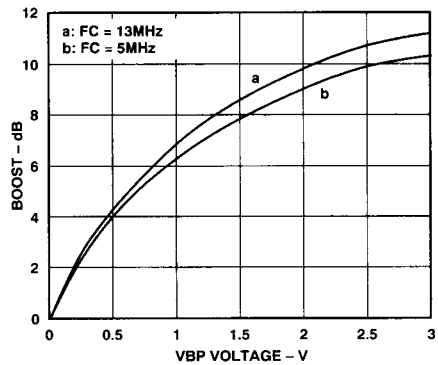


Figure 24. AD896-13 Boost vs. VBP Voltage

EQUALIZATION/BOOST

The Equalization/Boost can be enabled (high level) or disabled (low level) by a TTL input to the FBST pin. Gain equalization is performed, when enabled, by feeding forward the input signal and combining the signal with the low-pass filtered output of the first bi-quad section. The feed forward signal is amplified by a variable gain amplifier, which the user controls by applying a voltage to the VBP pin. The amplified signal is then summed together with the low-pass output of the first bi-quad and continues through the remaining bi-quad sections. The amount of boost is controlled by the voltage level applied to the VBF pin. The VBP voltage vs. Boost for the AD896-13 and AD896-23 are presented in Figures 24 and 25.

POWER-DOWN

Power management for the AD896 is achieved through the "PWRON" pin. A "high level" applied at this pin will enable the chip for normal operation. A "low level" applied to the PWRON pin will put the AD896 into the sleep mode. In the sleep mode, the AD896 will dissipate only 50 mW of power.

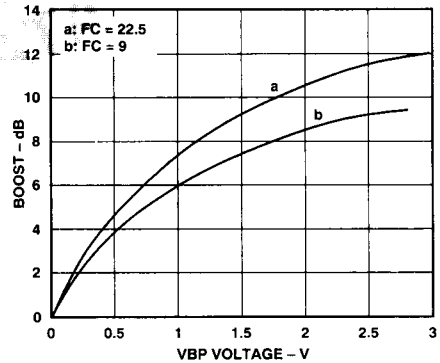


Figure 25. AD896-23 Boost vs. VBP Voltage

APPLICATIONS FOR THE AD896

The AD896 is a seventh order Bessel function filter with both programmable cutoff frequency and boost equalization. The AD896 is fully differential providing both low-pass normal and differentiated outputs with no time delay introduced between the two signals. The AD896 is ideally suited for applications where low group delay and time coherency between the normal low-pass and differentiated signals is a necessity. In order to enable the equalization/boost function the FBST must be held high (Logic Level 1), a low level will disable equalization.

Programming the cutoff frequency can be achieved through the IFP or VFP input. Both inputs are connected to the emitter of a PNP transistor which behaves as a current sink. The IFP input has a series combination of a 500 Ω resistor and two diodes. The input bias voltage at VFP is VR − 700 mV. The bias voltage at IFP with 300 μA program current is approximately VR + 200 mV; with 800 μA it is approximately VR + 500 mV. Programming of the AD896 through the IFP pin is achieved by varying the current from 0.3 mA to 0.8 mA. Programming the AD896 through the VFP is achieved by applying a voltage through a series resistor (R_X) to the VFP pin. The following formula can be used to calculate the current into the VFP: = (VFP voltage − 0.66 VR)/R_X.

Programming the amount of Boost is achieved by applying a voltage to the VBP input which is a high impedance input. The voltage range for operation is 0 to VR volts, where VR is the AD896 reference voltage (normally 2.2 V).

Figure 26 shows the AD896 being used along with an AD897 "40 mb/s Peak Detector and Data Synchronizer" and an AD7528 "CMOS Dual 8-Bit Buffered Multiplying DAC" in a constant density recording disk drive application. The cutoff frequency and equalization/boost are microprocessor controlled through the AD7528 dual DAC. The AD7528 is operated in the voltage mode with the reference being applied to OUTA (Pin 2) and OUTB (Pin 20) pins, the voltage output taken from V_{REF} A (Pin 4) and V_{REF} B (Pin 18). DAC A controls the voltage applied to the VBP pin for equalization/boost. The voltage from DAC B is used to develop a current which sets the cutoff frequency. Both outputs of the DAC are buffered through an OP-221 operational amplifiers before being applied to the AD896. The microprocessor controls the enabling/disabling of the equalization through the FBST input (Pin 8 high level = ON, low level = OFF), and the power up/ down of the filter is accomplished by the PWRON input (Pin 14 high level = ON, low level = OFF).

This application will allow the cutoff frequency to be changed by the processor to match the data rate of a particular zone (as in a disk drive) The amount of boost can also be changed as needed for different areas of the disk and for different data rates through DAC A. The low-pass normal and differentiated outputs of the AD896 are both needed for data qualification in the AD897. The AD896 is internally biased by VR (typically 2.2 V), therefore the input and output signals need to be ac coupled. The LSB of DAC B in this application corresponds to approximately 100 kHz after the bias voltage is reached of (0.66 VR). This will vary slightly with the reference voltage of different parts.

Figure 27 shows the AD896 being used as an antialiasing filter in a high speed data acquisition application. Using the AD773 "10-Bit 18 MSPS Monolithic A/D Converter," AD7528 "CMOS Dual 8-Bit Buffered Multiplying DAC," AD680 "2.5 V Reference," and a matched transistor pair. In this application the Boost is controlled by the DAC A voltage, the same as the previous application. The cutoff frequency is controlled by the current set up by the voltage out of DAC B and the matched transistors. This is a very accurate method of programming the cutoff frequency. The cutoff frequency must be set below Nyquist frequency (sample frequency/2) to prevent aliasing errors.

GENERAL LAYOUT REQUIREMENT

Care must be taken to ensure good RF practice in the PC layout to avoid oscillations. A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the V_{CC} (Pin 4 and Pin 12) as possible.

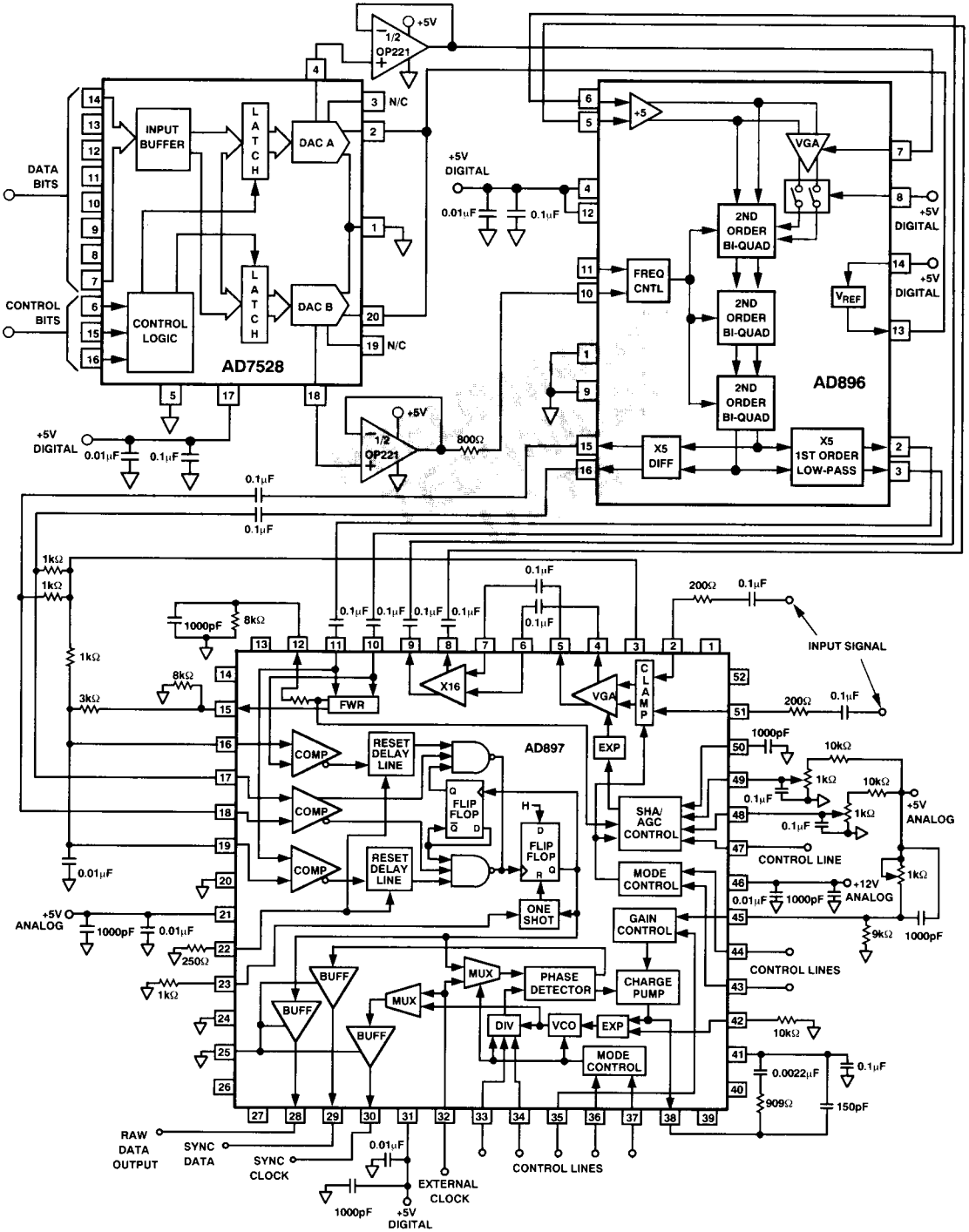


Figure 26. Constant Density Read Channel Application

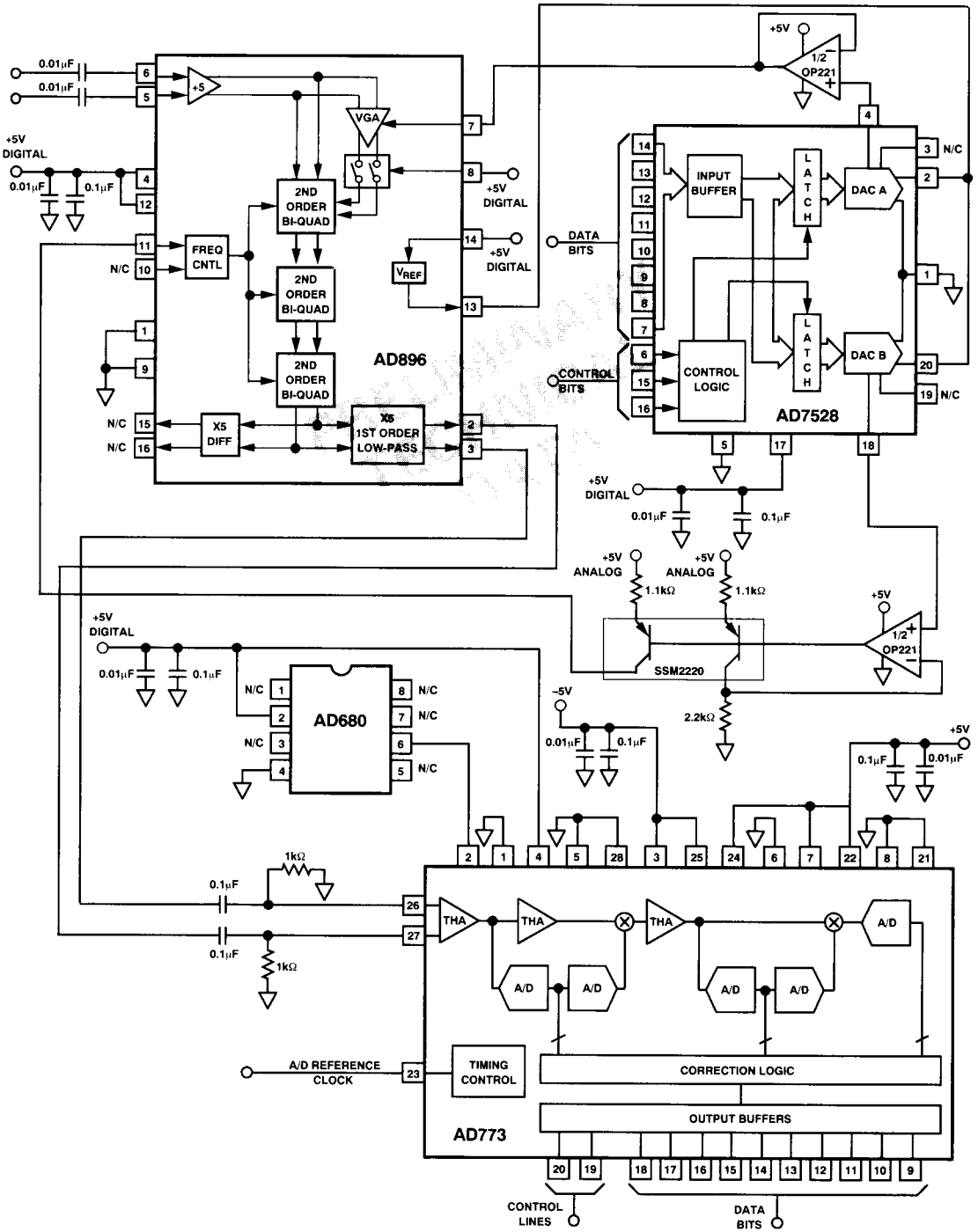


Figure 27. High Speed Data Acquisition Application