

0.4 μ V Input Noise, 14V RRIO Operational Amplifiers (Dual/Quad)

Description

The SL2122 (dual), and SL2124 (quad) are ultra-low noise dual and quad mid voltage (3V to 14V) operational amplifiers (opamps) with rail-to-rail input and output swing capabilities. These devices are very suitable for applications where ultra-low noise, high voltage operation and a small footprint. SL2122S and SL2124S are with Shutdown function.

Features

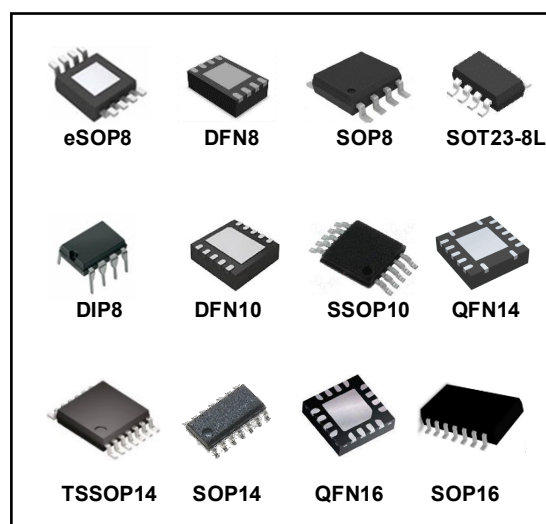
- Supply voltages from 3V to 14V
- Ultra-low input voltage noise (20Hz to 20kHz) 0.4 μ V
- Excellent THD+N 96dB
- Excellent SNR 120dB
- Rail-to-rail input and output
- Low input offset voltage: \pm 0.1mV typ
- Unity-gain bandwidth: 25MHz
- Low quiescent current (per opamp): 1.2mA typ @14V
- Shutdown function (SL2122S and SL2124S)

Applications

- Infotainment system
- HVAC: heating, ventilating, and air conditioning
- Industrial control
- Test equipment
- Portable Equipment
- Active filters
- Data acquisition system

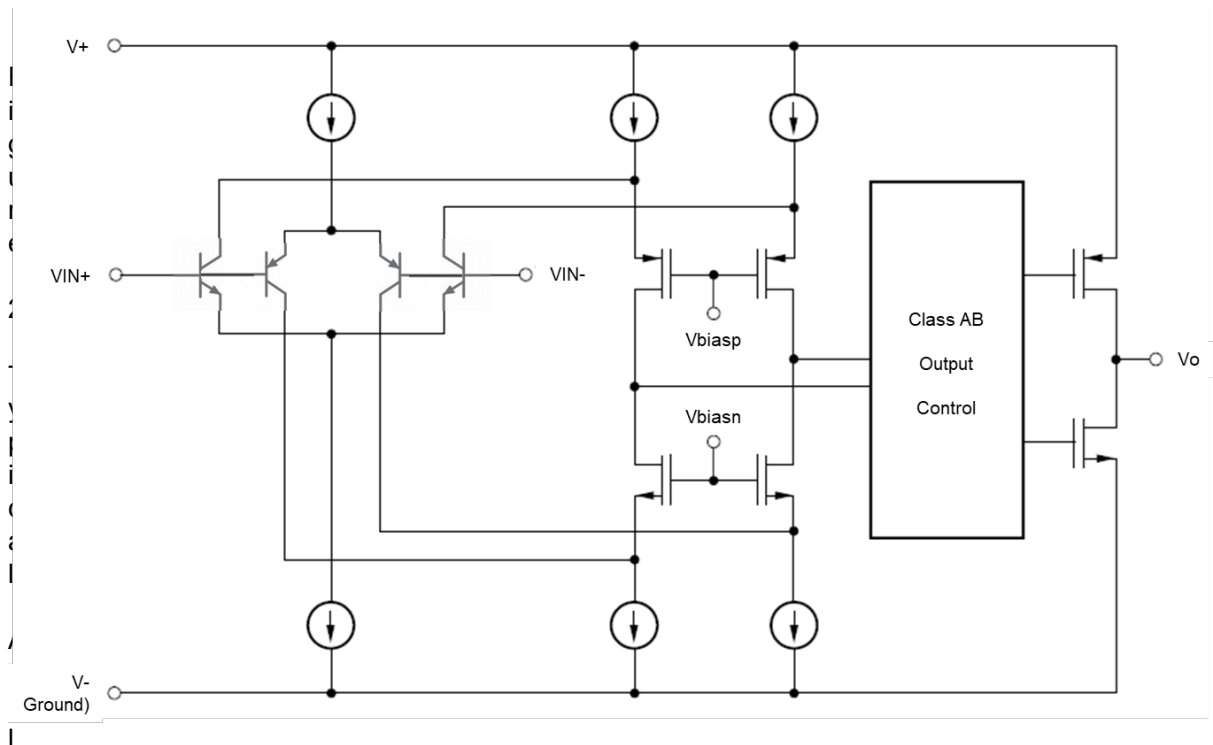
Table 1 Device Summary

Order code	Package	Packing	MOQ
SL2122A	eSOP8	Reel	2500
SL2122B	DFN8	Reel	3000
SL2122C	SOP8	Reel	4000
SL2122D	SOT23-8L	Reel	3000
SL2122E	DIP8	Tube	2000
SL2122SA	DFN10	Reel	5000
SL2122SB	SSOP10	Reel	2500
SL2124A	QFN14	Reel	6000
SL2124 B	TSSOP14	Reel	3000
SL2124 C	SOP14	Reel	2500
SL2124SA	QFN16	Reel	6000
SL2124SB	SOP16	Reel	4000

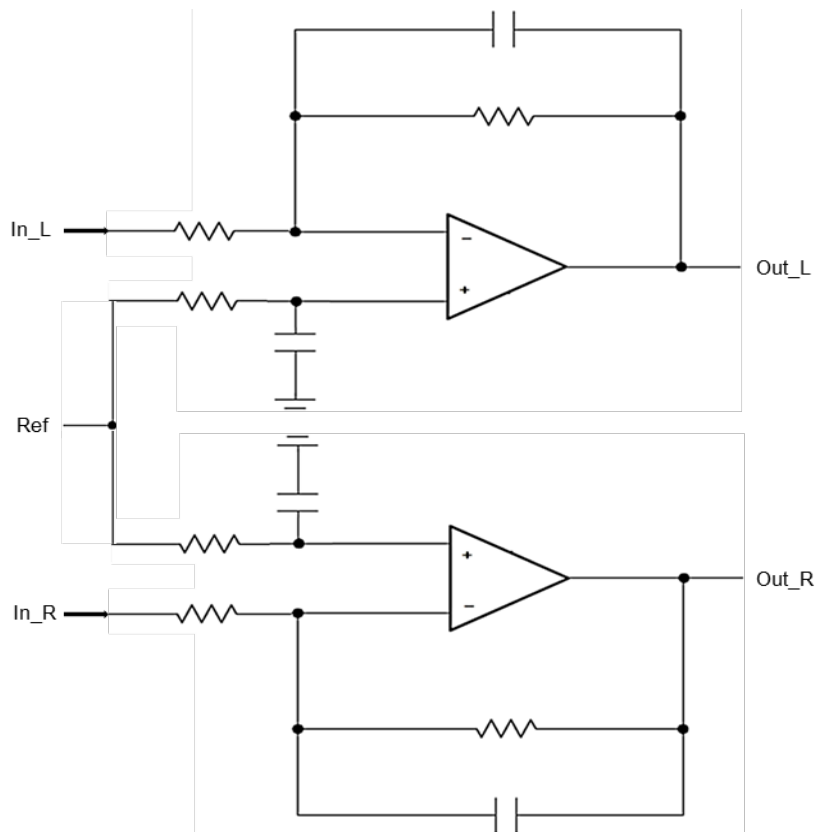


1 Block Diagram and Application Circuit

Figure 1 Block Diagram



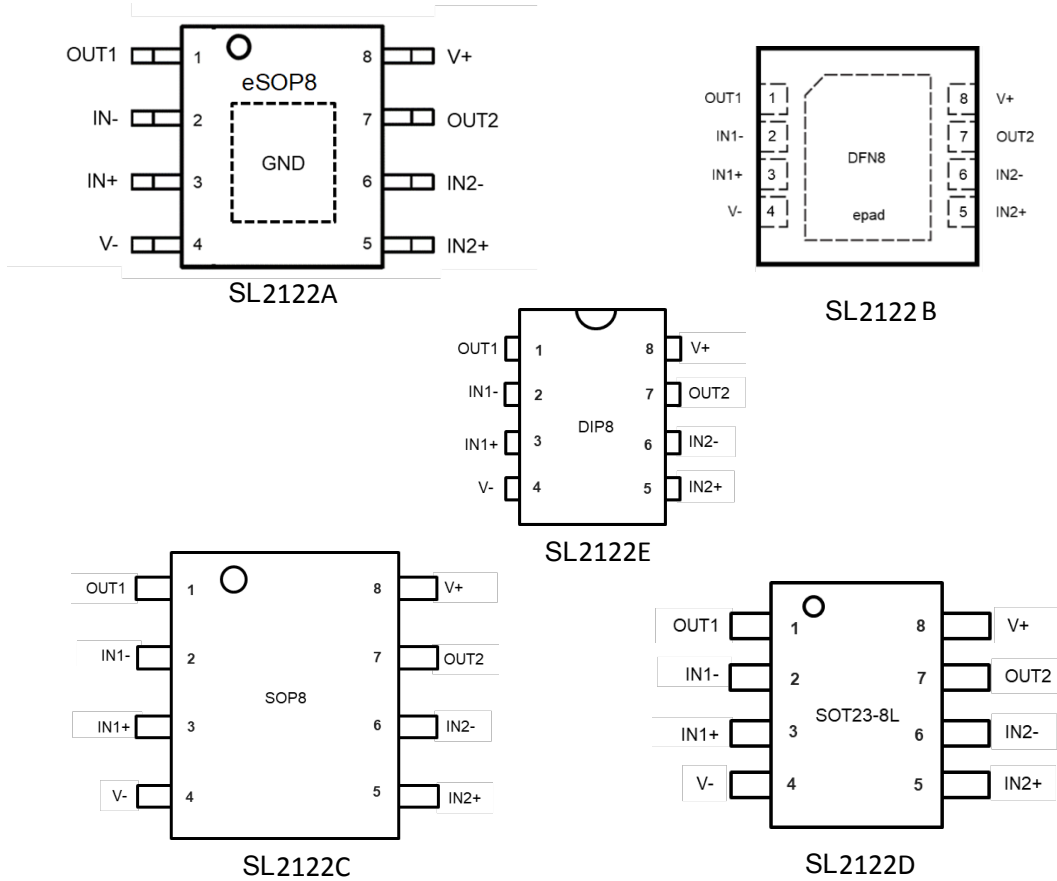
Application Circuit (Stereo Sound Input Amplifier)



2 Pin Description

2.1 SL2122A/B/C/D/E Pinouts

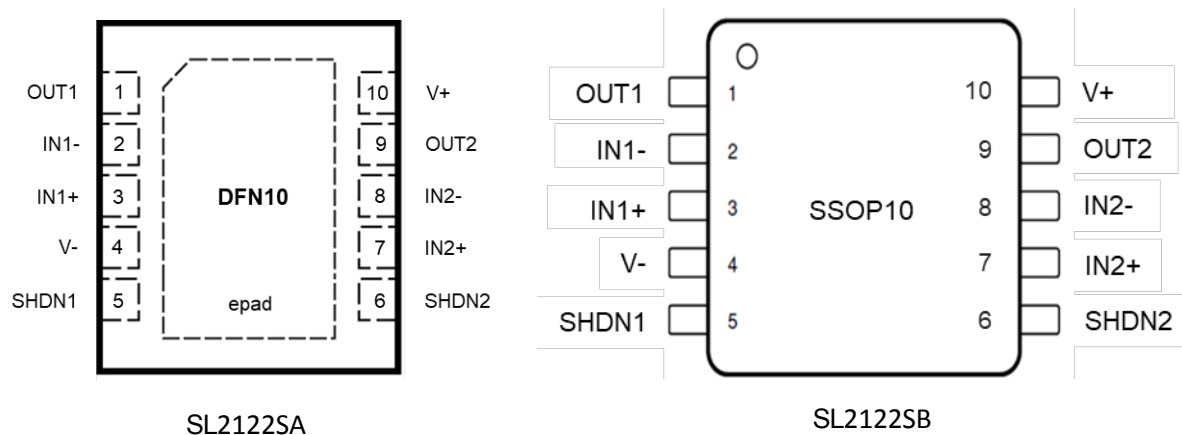
Figure 3 SL2122A/B/C/D/E Pinouts



Pin number	Pin name	Description
1	OUT1	Output 1
2	IN1-	Inverting input 1
3	IN1+	Non-inverting input 1
4	V-	Negative supply or ground
5	IN2+	Non-inverting input 2
6	IN2-	Inverting input 2
7	OUT2	Output 2
8	V+	Positive supply

2.2 SL2122SA/B Pinouts

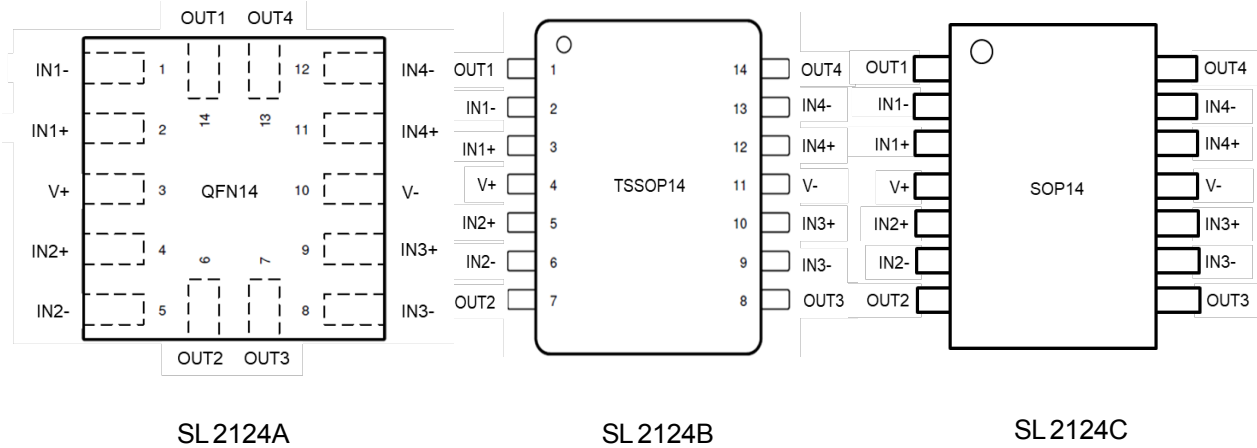
Figure 4 SL2122SA/B Pinouts



Pin number	Pin name	Description
1	OUT1	Output 1
2	IN1-	Inverting input 1
3	IN1+	Non-inverting input 1
4	V-	Negative supply or ground
5	SHDN1	Shutdown1: "High" = opamp 1 disabled Shutdown1: "Low" = opamp 1 enabled Shutdown1: "Float" = opamp 1 enabled
6	SHDN2	Shutdown2: "High" = opamp 1 disabled Shutdown2: "Low" = opamp 1 enabled Shutdown2: "Float" = opamp 1 enabled
7	IN2+	Non-inverting input 2
8	IN2-	Inverting input 2
9	OUT2	Output 2
10	V+	Positive supply

2.3 SL2124A/B/C Pinouts

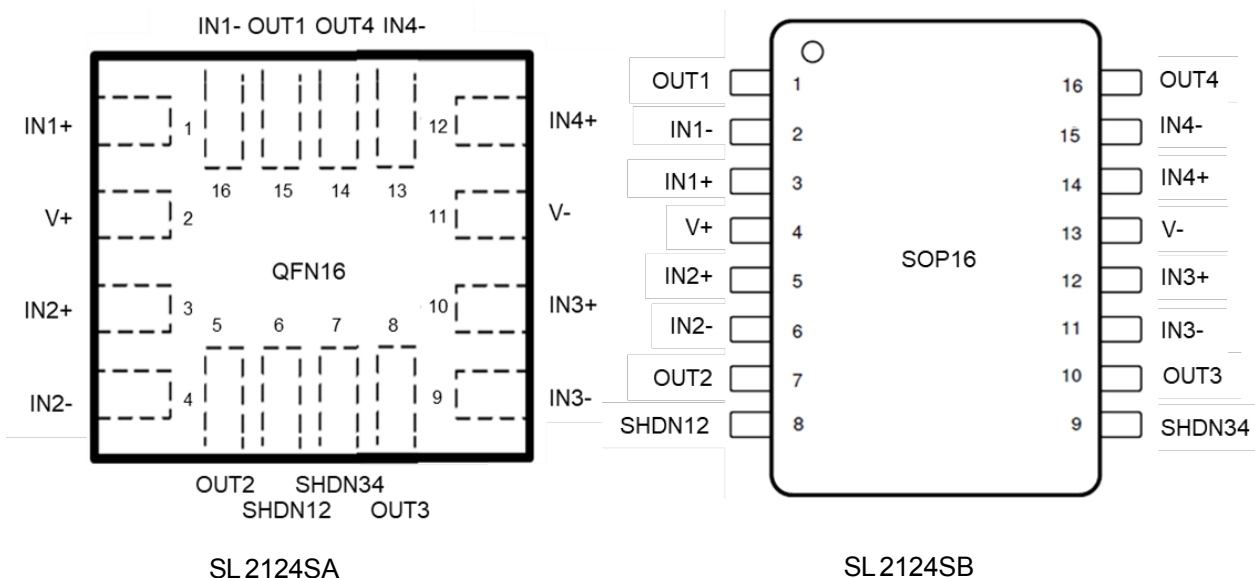
Figure 5 SL 2124A/B/C Pinouts



Pin number	SL 2124A		SL 2124B/C	
	QFN14 Pin name	QFN14 Description	TSSOP14/SOP14 Pin name	TSSOP14/SOP14 Description
1	IN1-	Inverting input 1	OUT1	Output 1
2	IN1+	Non-inverting input 1	IN1-	Inverting input 1
3	V+	Positive supply	IN1+	Non-inverting input 1
4	IN2+	Non-inverting input 2	V+	Positive supply
5	IN2-	Inverting input 2	IN2+	Non-inverting input 2
6	OUT2	Output 2	IN2-	Inverting input 2
7	OUT3	Output 3	OUT2	Output 2
8	IN3-	Inverting input 3	OUT3	Output 3
9	IN3+	Non-inverting input 3	IN3-	Inverting input 3
10	V-	Negative supply or ground	IN3+	Non-inverting input 3
11	IN4+	Non-inverting input 4	V-	Negative supply or ground
12	IN4-	Inverting input 4	IN4+	Non-inverting input 4
13	OUT4	Output 4	IN4-	Inverting input 4
14	OUT1	Output 1	OUT4	Output 4

2.4 SL 2124SA/B Pinouts

Figure 6 SL 2124SA/B Pinouts



Pin number	SL 2124SA		SL 2124SB	
	QFN16 Pin name	QFN16 Description	SOP16 Pin name	SOP16 Description
1	IN1+	Non-inverting input 1	OUT1	Output 1
2	V+	Positive supply	IN1-	Inverting input 1
3	IN2+	Non-inverting input 2	IN1+	Non-inverting input 1
4	IN2-	Inverting input 2	V+	Positive supply
5	OUT2	Output 2	IN2+	Non-inverting input 2
6	SHDN12	Shutdown12: "High" = opamp 1&2 disabled	IN2-	Inverting input 2
7	SHDN34	Shutdown34: "High" = opamp 3&4 disabled	SHDN12	Shutdown12: "High" = opamp 1&2 disabled
8	OUT3	Output 3	SHDN34	Shutdown34: "High" = opamp 3&4 disabled
9	IN3-	Inverting input 3	IN3-	Inverting input 3
10	IN3+	Non-inverting input 3	OUT3	Output 3
11	V-	Negative supply or ground	IN3-	Inverting input 3
12	IN4+	Non-inverting input 4	IN3+	Non-inverting input 3
13	IN4-	Inverting input 4	V-	Negative supply or ground

14	OUT4	Output 4	IN4+	Non-inverting input 4
15	OUT1	Output 1	IN4-	Inverting input 4
16	IN1-	Inverting input 1	OUT4	Output 4

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _s	Supply voltage (V ₊) - (V ₋)	-0.3 to +18	V
IN+, IN-	Input pin voltage	(V ₋) - 0.5 to (V ₊) +0.5	V
OUT	Output pin voltage	(V ₋) - 0.5 to (V ₊) +0.5	V
T _j	Junction temperature	150	°C
T _{stg}	Storage temperature	-55 to +150	°C

3.2 Thermal Data

Table 3 Thermal Data

Package	R _{th j-amb}	R _{th j-case}	Unit
eSOP8	60	10	°C/W
DFN8	43	5	°C/W
SOP8	136	77	°C/W
SOT23-8L	184	100	°C/W
DIP8	85	41	°C/W
DFN10	42	6	°C/W
SSOP10	160	45	°C/W
QFN14	47	4	°C/W
TSSOP14	113	62	°C/W
SOP14	106	64	°C/W
QFN16	45	5	°C/W
SOP16	80	30	°C/W

3.3 ESD

Table 4 ESD

Symbol	Parameter	Value	Unit
All pins	ESD (HBM)	±2,000	V

3.4 Electrical Characteristics

For $V_s = (V_+) - (V_-) = 14V$ at $T_a = 25^\circ C$, $R_L = 10k\Omega$ connected to $V_s/2$, $V_{cm} = V_s/2$, and $V_{out} = V_s/2$ (unless otherwise noted).

Table 5 Electrical Characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_s	Supply voltage (V_+) - (V_-)		3		14	V
T_a	Operating ambient temperature		-40		85	$^\circ C$
Power Supply						
I_q	Quiescent current per amplifier	$V_s=14V$, $I_o=0mA$		1.2	2.0	mA
		all temp			3.0	
Offset Voltage						
V_{os}	Input offset voltage			±0.1	±1	mV
		all temp			±2	mV
dV_{os}/dT	Drift	all temp		±0.2		$\mu V/^\circ C$
PSRR	Power-supply rejection ratio	At DC		120		dB
Csep	Channel separation	At DC		120		dB
Input Voltage Range						
V_{cm}	Common mode voltage range	$V_s=3V$ to 14V	(V_-)-0.1		(V_+)+0.1	V
CMRR	Common mode rejection ratio	At DC		100		dB
Input Bias Current						
I_b	Input bias current				±1	μA
I_{os}	Input offset current				±0.1	μA
Noise						
E_n	Input voltage noise	$f=20Hz$ to 20kHz		0.4		μV
Open Loop Gain						
A_{ol}	Open loop voltage gain			130		dB
Frequency Response						
GBP	Gain bandwidth product	$G=+1$, $C_L=10pF$		25		MHz
SR	Slew rate	$G=+1$, $C_L=10pF$		12		$V/\mu s$
T_s	Settling time	To 0.1%, 2V step, $G=+1$, $C_L=10pF$		0.3		μs
THD+N	Total harmonic distortion + Noise (3 rd order filter;	$V_s=14V$, $V_{cm}=10V$, $V_o=1V_{rms}$, $G=+1$,		96		dB

	BW= 80kHz at -3dB.)	f=1kHz, no load				
SNR	Signal to Noise Ratio	Vs=14V, Vin=1Vrms, G=+1, f=1kHz		120		dB
Output						
Vo	Voltage output swing from supply rails	RL=10kΩ		60	80	mV
		RL=2kΩ		170	200	
Isc	Short circuit current			±20		mA
		SL2122A only eSOP8 package		±100		mA
Shutdown (SL2122S and SL2124S only)						
Iqsd	Quiescent current per amplifier	Vs=3V to 14V, amplifier disabled, SHDN = "High"		20	40	μA
Vsd	Shutdown threshold	Vs=3V to 14V, amplifier disabled, SHDN = "High"	4			V
Vsdl	Low level shutdown threshold	Vs=3V to 14V, amplifier enabled, SHDN = "Float" or SHDN = "Low"			1	V
ton	Amplifier enable time	Vs=3V to 14V, full shutdown; G=+1, Vo = 0.9×Vs/2, RL connected to V-		10		μs
toff	Amplifier disable time	Vs=3V to 14V, G=+1, Vo=0.1×Vs/2, RL connected to V-		1		μs

Disable time (toff) and enable time (ton) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

3.5 Typical Electrical Characteristics

Figure 7 Vos Distribution

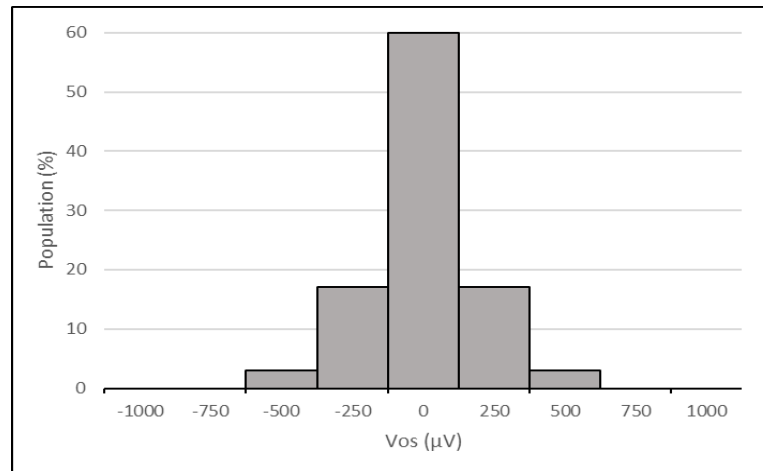


Figure 8 Vos vs Input Common Mode Voltage

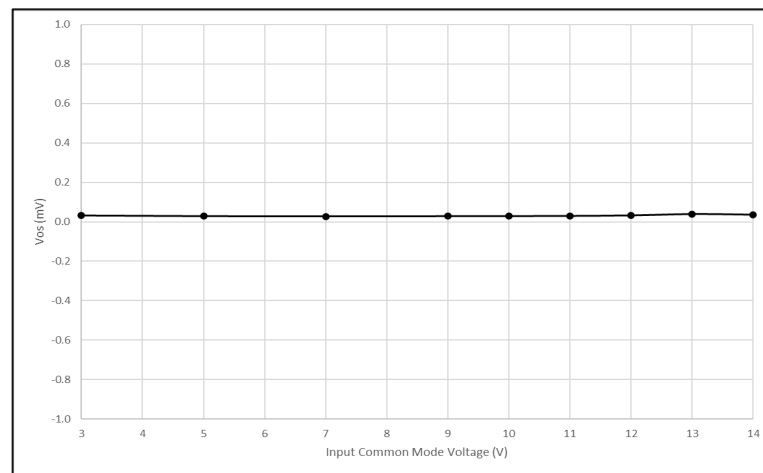


Figure 9 Vos vs Vs

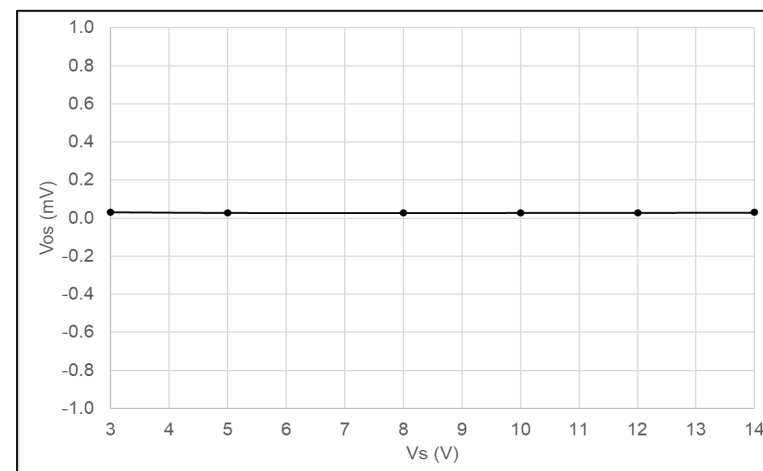


Figure 10 Iq (per opamp) vs Input Common Mode Voltage

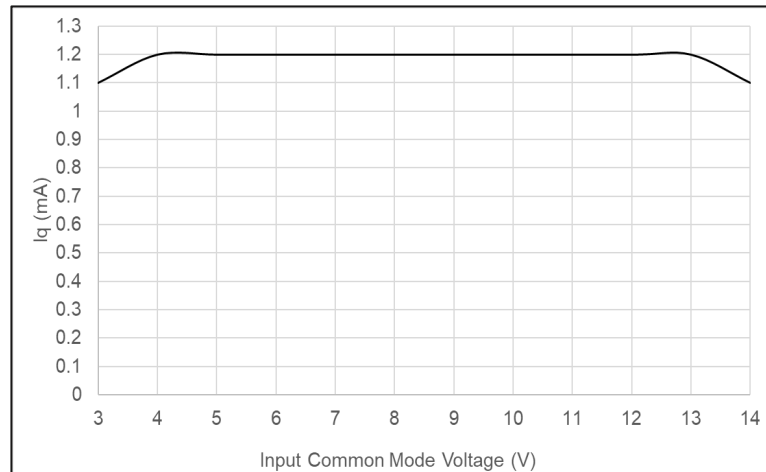


Figure 11 Iq (per opamp) vs Vs

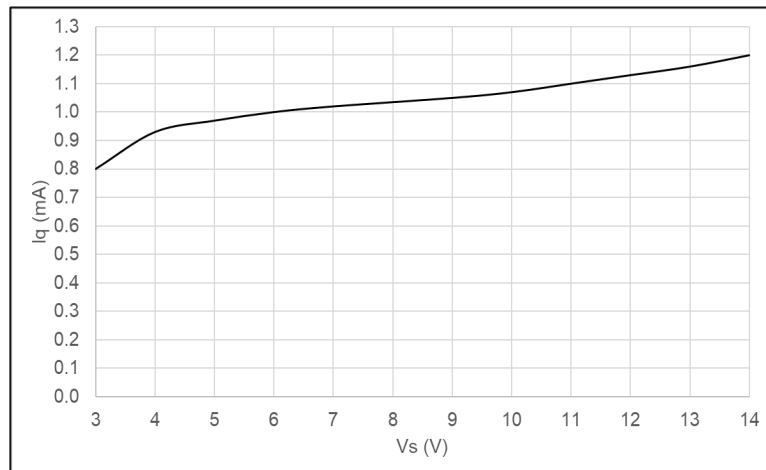


Figure 12 THD+N vs Frequency

Figure 13 Large Signal Step Response

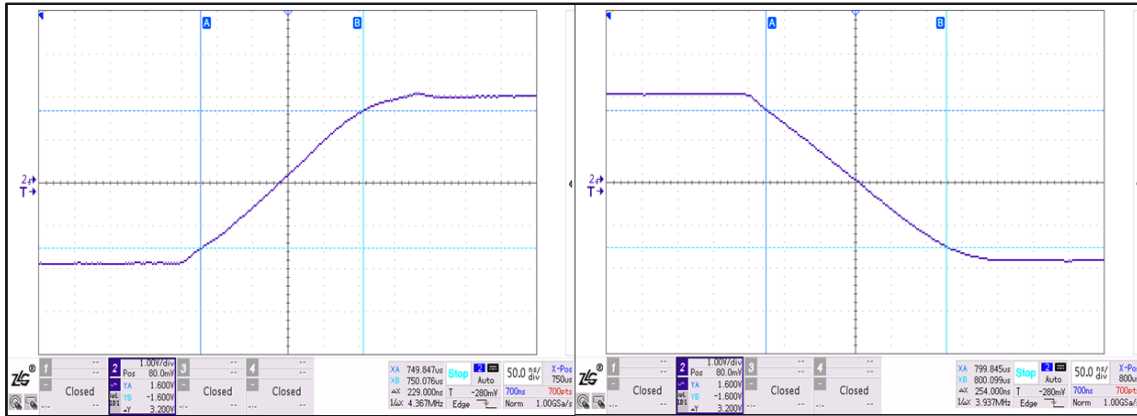


Figure 14 Settling Time

4 Functional Description

4.1 Overview

The SL212x devices are a family of high voltage, rail-to-rail input and output opamps. These devices operate from 3V to 14V, are unity gain stable, and are designed for a wide range of applications and used in virtually any single supply application.

4.2 Rail to Rail Input and Output

The input common mode voltage range of the SL 212x family extends 100mV beyond the supply rails for the full supply voltage range of 3V to 14V. This performance is achieved with a complementary input stage: a NPN input differential pair in parallel with a PNP differential pair, as shown in Figure 1.

Designed as a high voltage operational amplifier, the SL212x series delivers a robust output drive capability. A class AB output stage with common source Mosfets achieves full rail-to-rail output swing capability. For resistive loads of 10k Ω , the output swings to within 60mV (typ) of either supply rail, regardless of the applied power supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

4.3 Overload Recovery

Overload recovery is defined as the time required for the opamp output to recover from a saturated state to a linear state. The output devices of the opamp enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. The overload recovery time for the SL212x family is approximately 20ns.

4.4 EMI Rejection

The SL212x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components.

4.5 Shutdown

The SL212xS has shutdown function. The amplifiers can be shut down by enabling the respective shutdown pin.

5 Package Information

5.1 Package Dimensions

Figure 15 eSOP8 Mechanical Data and Package Dimensions

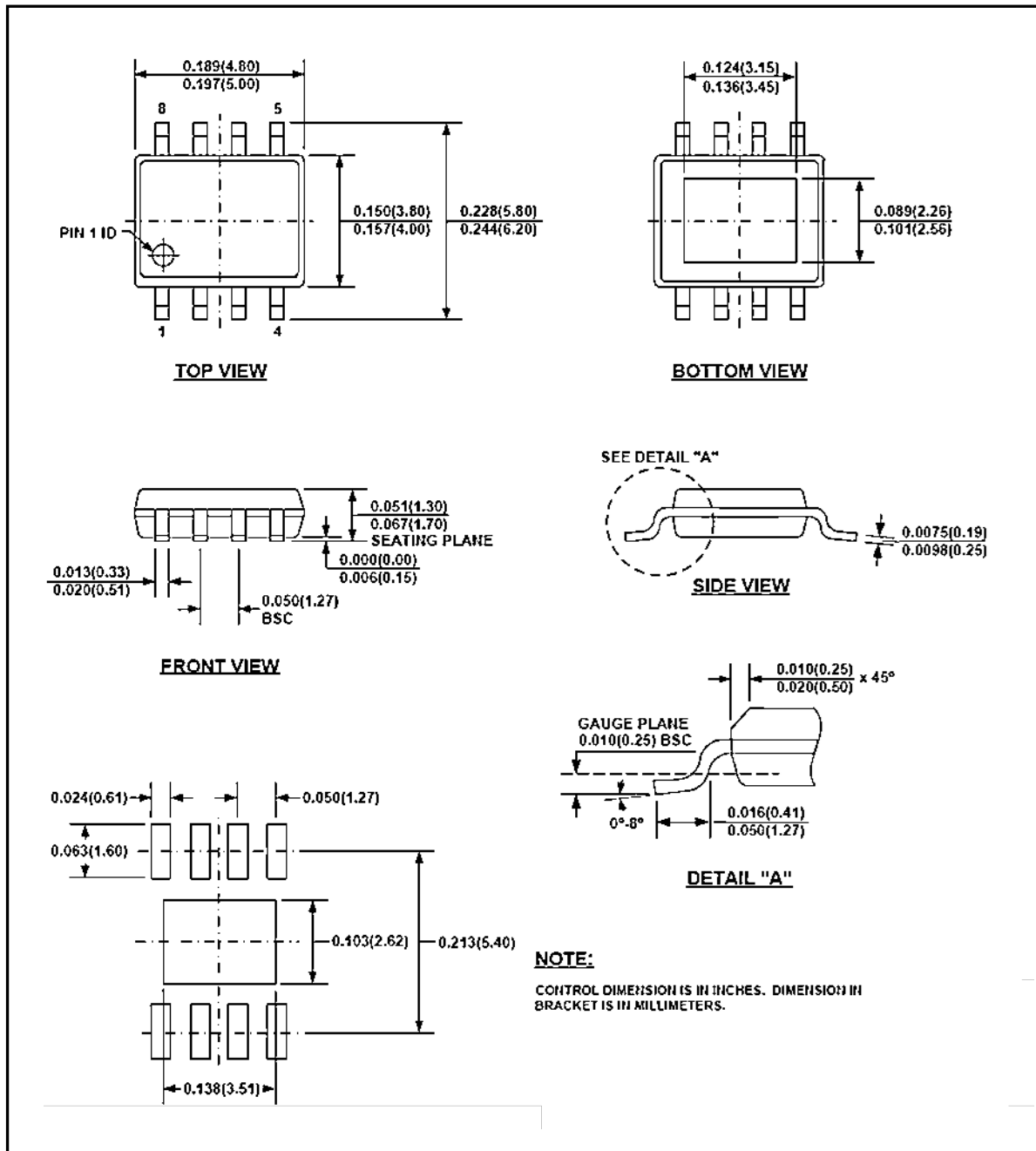


Figure 16 DFN8 Mechanical Data and Package Dimensions

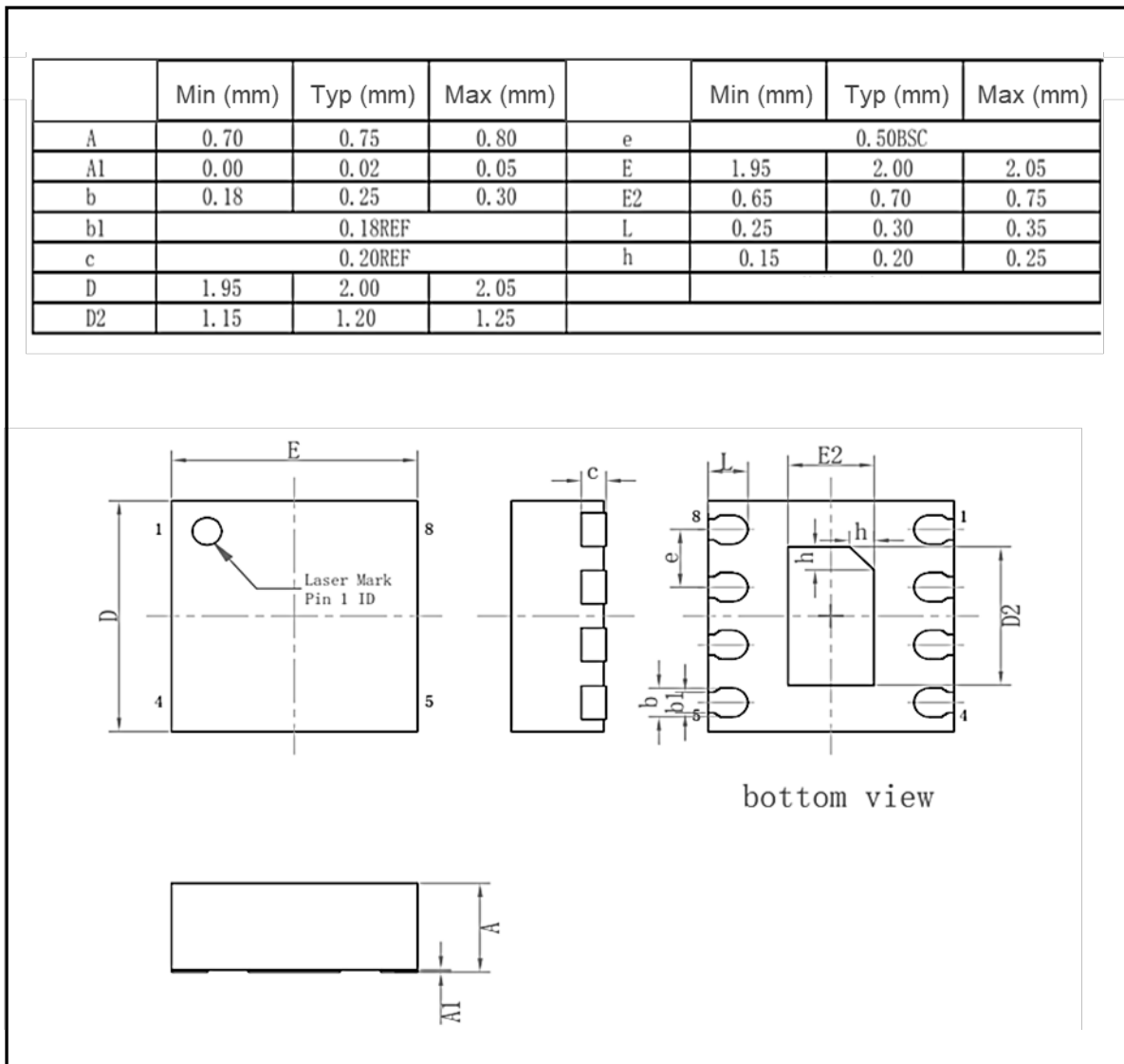


Figure 17 SOP8 Mechanical Data and Package Dimensions

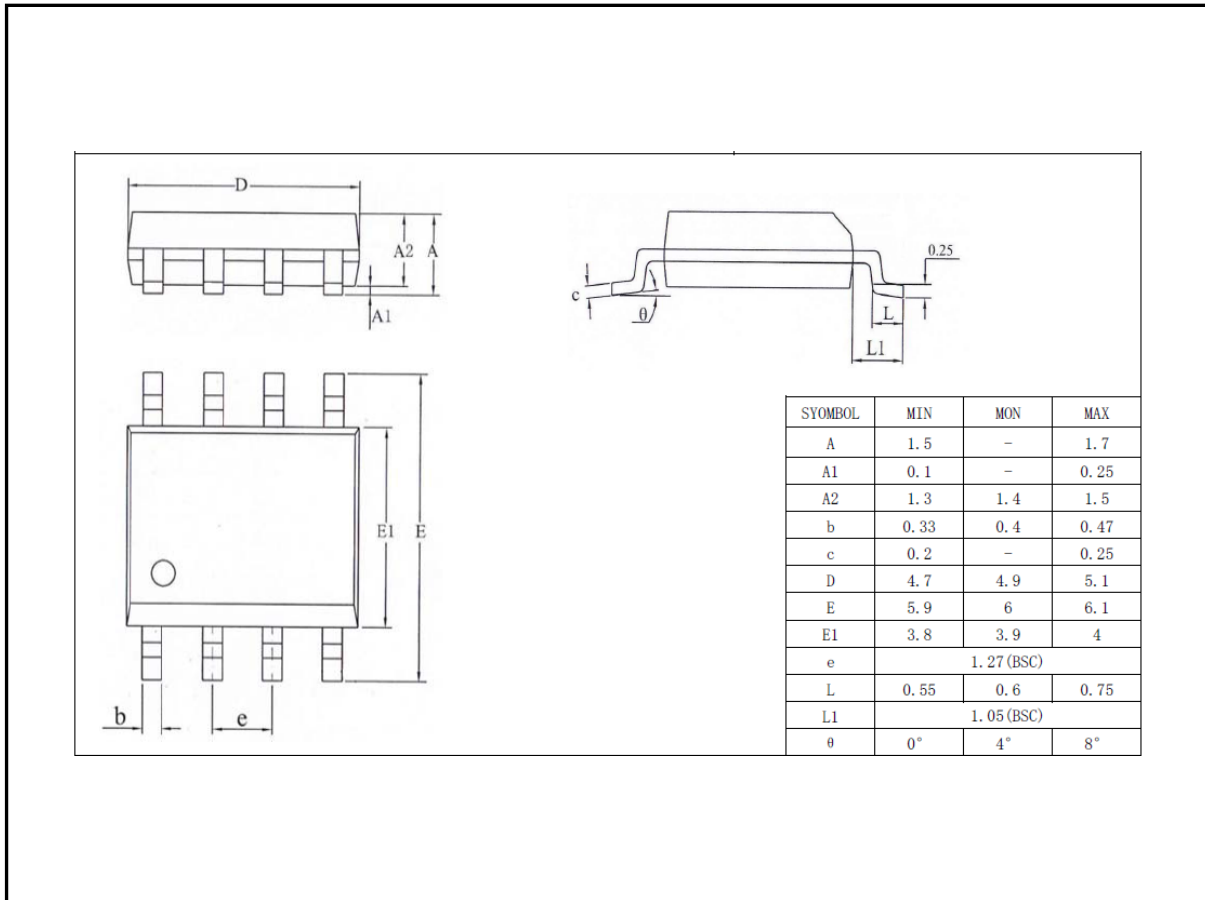


Figure 18 SOT23-8L Mechanical Data and Package Dimensions

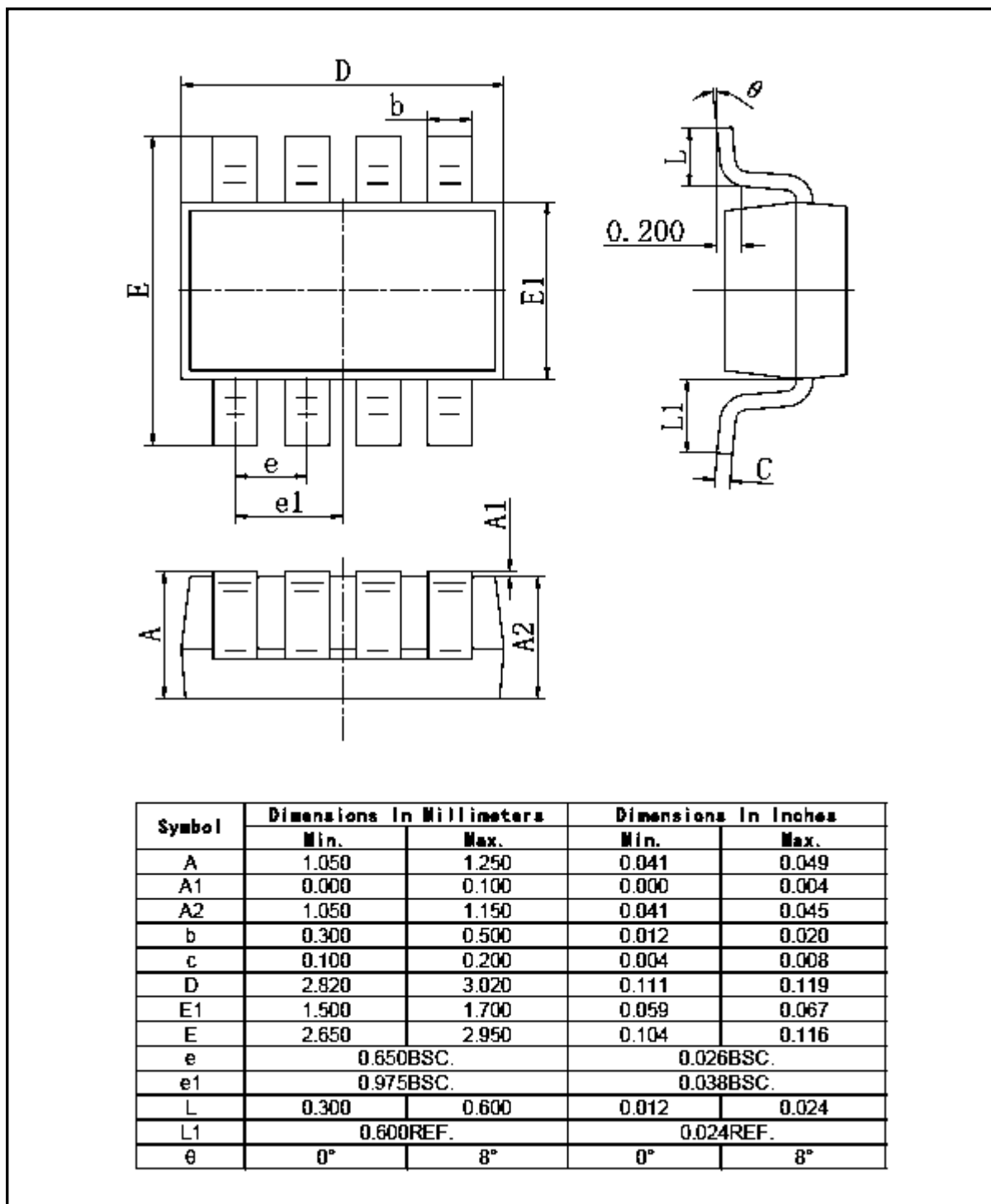


Figure 19 DIP8 Mechanical Data and Package Dimensions

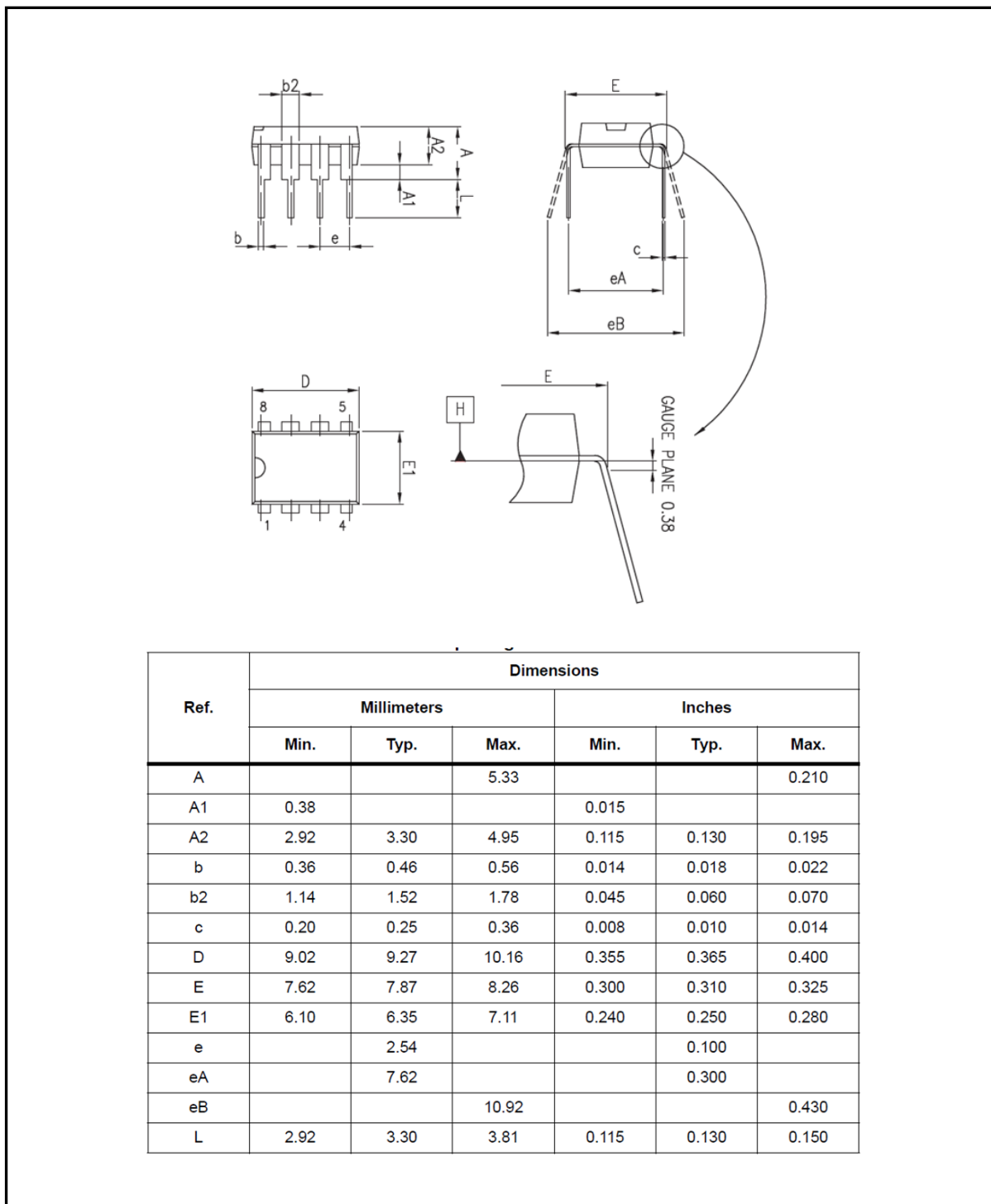


Figure 20 DFN10 Mechanical Data and Package Dimensions

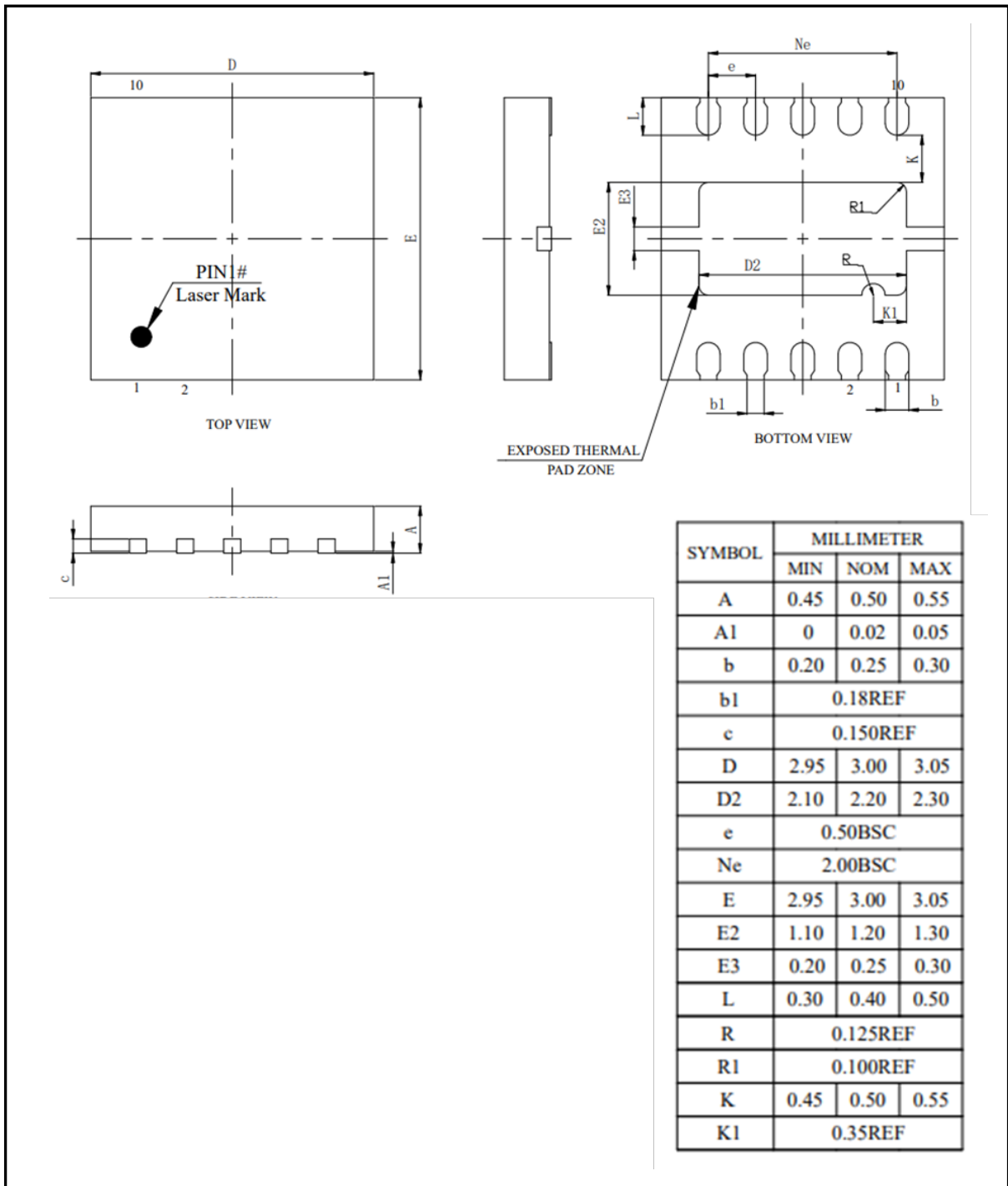


Figure 21 SSOP10 Mechanical Data and Package Dimensions

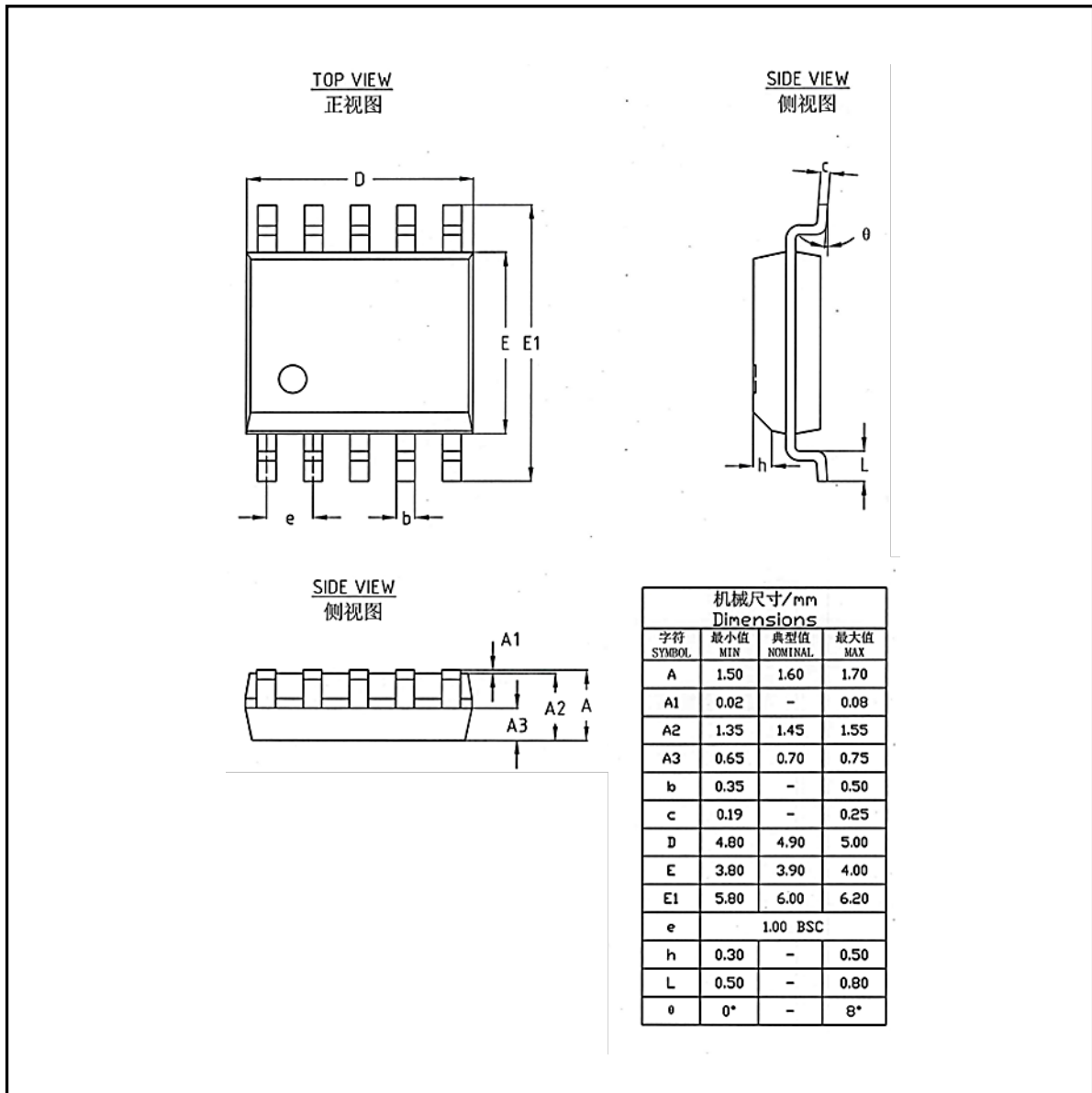


Figure 22 QFN14 Mechanical Data and Package Dimensions

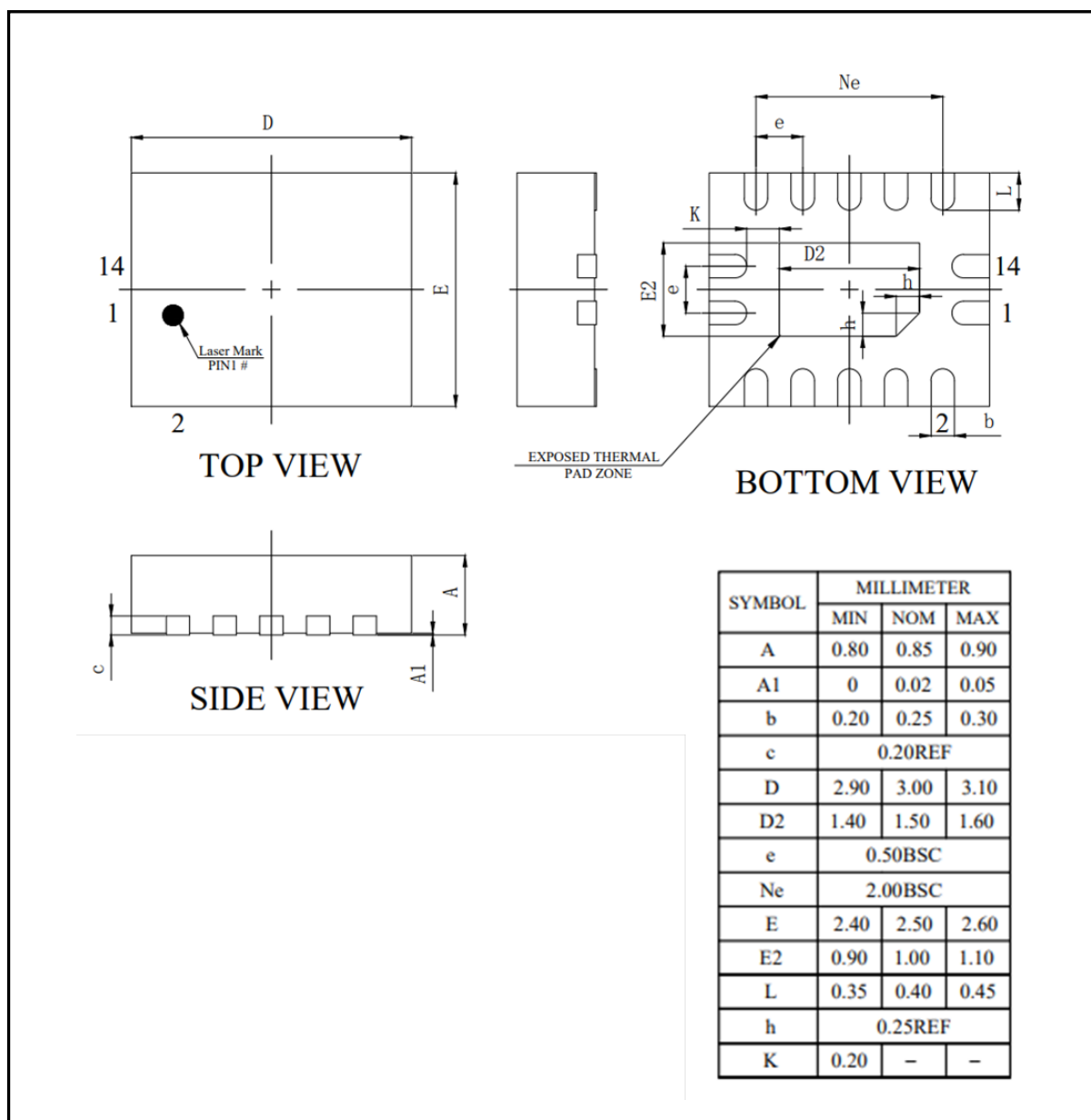


Figure 23 TSSOP14 Mechanical Data and Package Dimensions

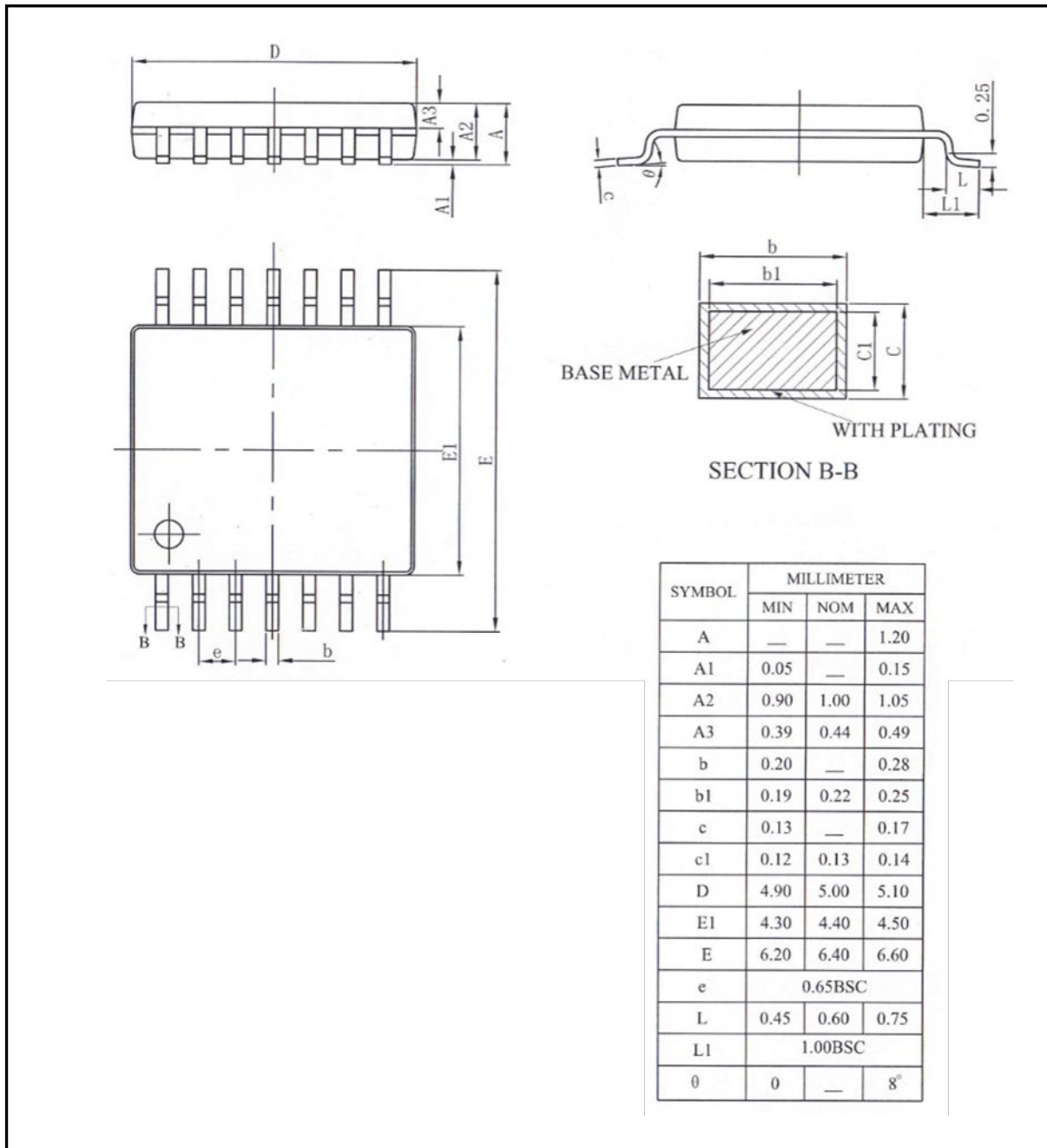


Figure 24 SOP14 Mechanical Data and Package Dimensions

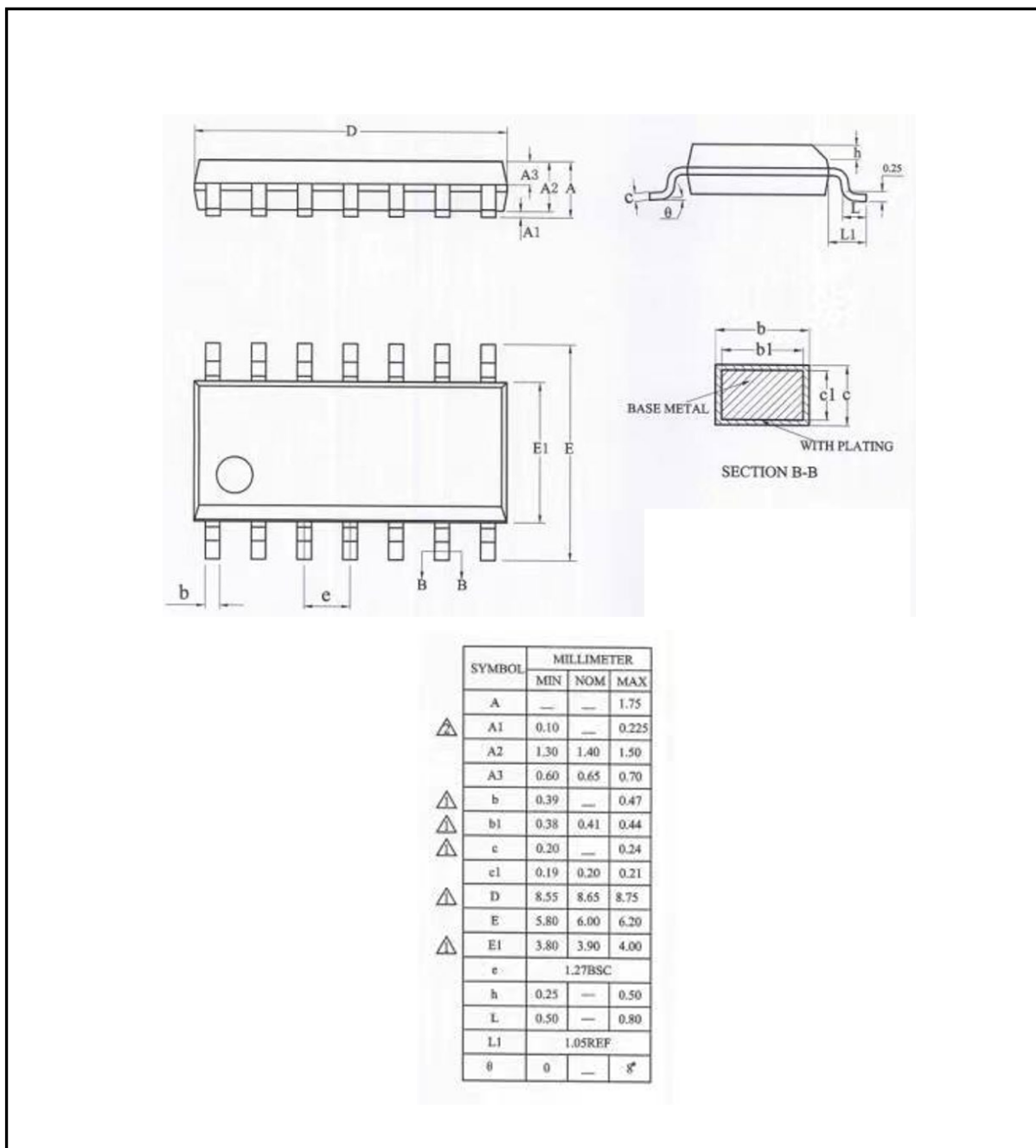


Figure 25 QFN16 Mechanical Data and Package Dimensions

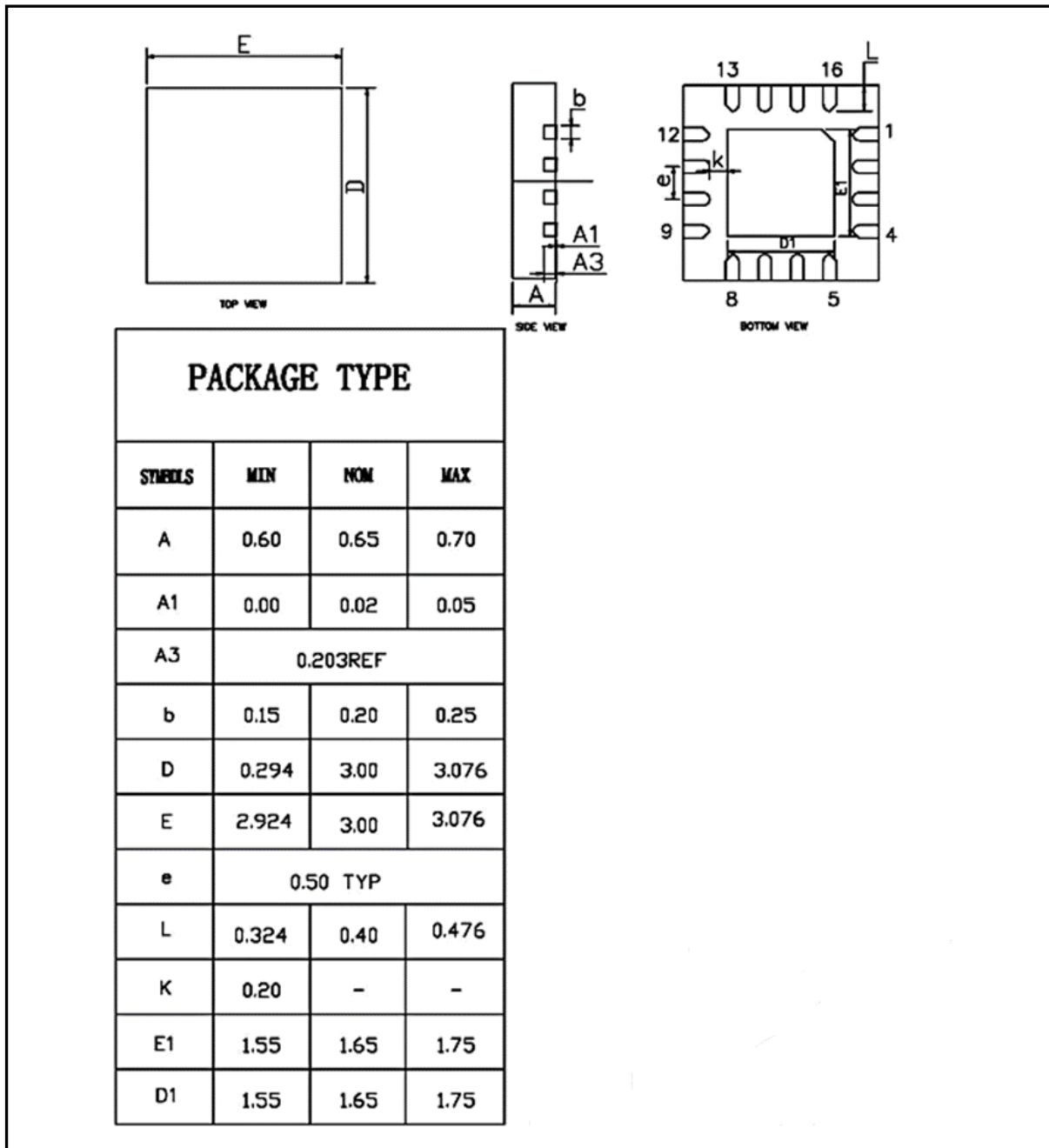


Figure 26 SOP16 Mechanical Data and Package Dimensions

