

# MSKSEMI 美森科

SEMICONDUCTOR



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## AO4812-MS

Product specification

## Description

The AO4812-MS uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

## General Features

$V_{DS} = 30V$   $I_D = 6A$

$R_{DS(ON)} < 42m\Omega$  @  $V_{GS}=4.5V$

$R_{DS(ON)} < 30m\Omega$  @  $V_{GS}=10V$

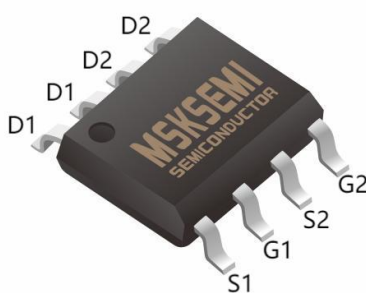
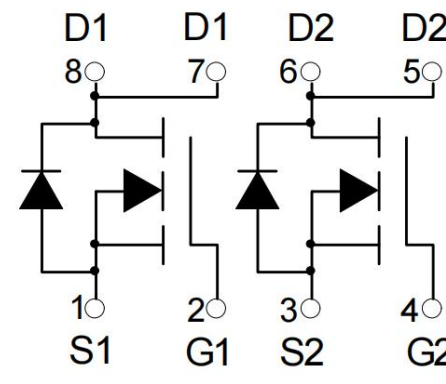

## Application

Battery protection

Load switch

Uninterruptible power supply

## Reference News

PACKAGE OUTLINE	Pin Configuration	Marking
		
SOP-8	N-Channel MOSFET	

## Absolute Maximum Ratings@T<sub>J</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Drain Current, $V_{GS}$ @ 4.5V <sup>3</sup>	6	A
$I_D@T_A=70^\circ C$	Drain Current, $V_{GS}$ @ 4.5V <sup>3</sup>	5	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	62.5	°C/W

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.2	1.8	2.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =6A		25	30	mΩ
		T <sub>J</sub> =125°C		40	48	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A		33	42	mΩ
F <sub>S</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =6A		15		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.76	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			255	310	pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		45		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			35	50	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.6	3.25	4.9	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge			5.2	6.3	nC
Q <sub>g(4.5V)</sub>				2.55	3.2	nC
Q <sub>gs</sub>	Gate Source Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =6A		0.85		nC
Q <sub>gd</sub>	Gate Drain Charge			1.3		nC
t <sub>D(on)</sub>	Turn-On DelayTime			4.5		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =2.5Ω		2.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime	, R <sub>GEN</sub> =3Ω		14.5		ns
t <sub>f</sub>	Turn-Off Fall Time			3.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =6A, dI/dt=100A/μs		8.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =6A, dI/dt=100A/μs		2.2		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using ≤ 10s junction-to-ambient thermal resistance.

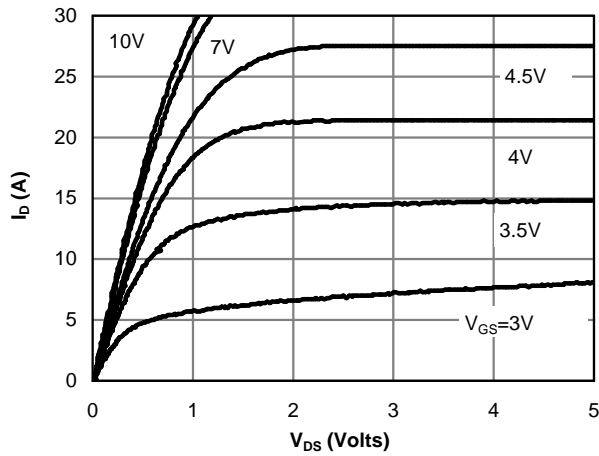
C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initialT<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

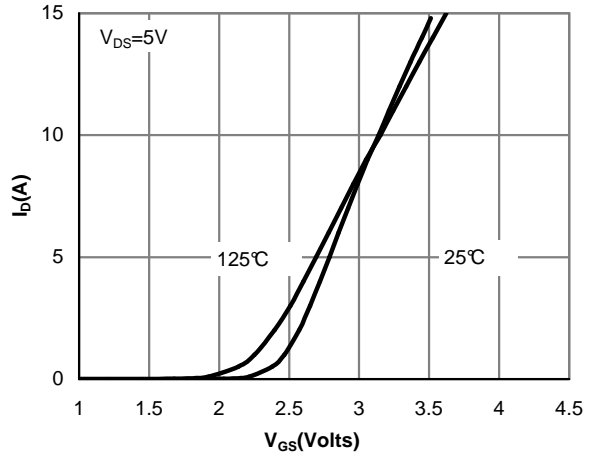
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

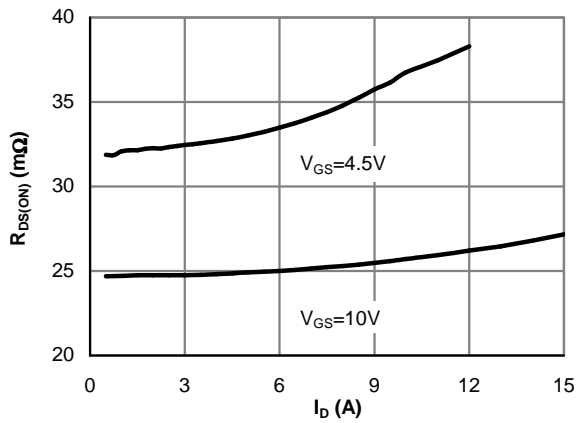
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



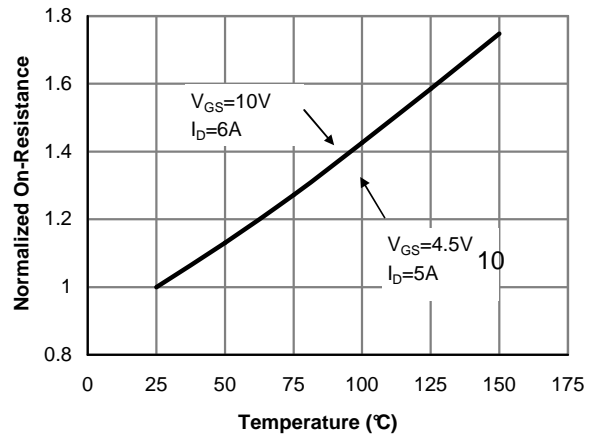
**Fig 1: On-Region Characteristics (Note E)**



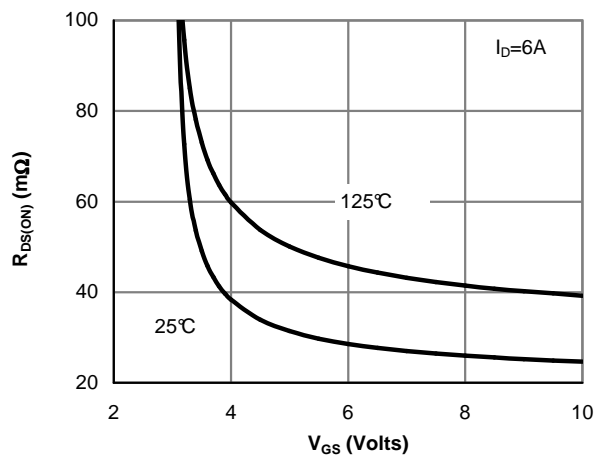
**Figure 2: Transfer Characteristics (Note E)**



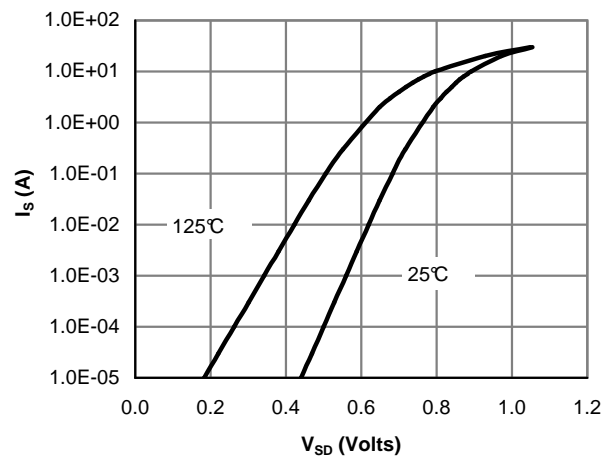
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

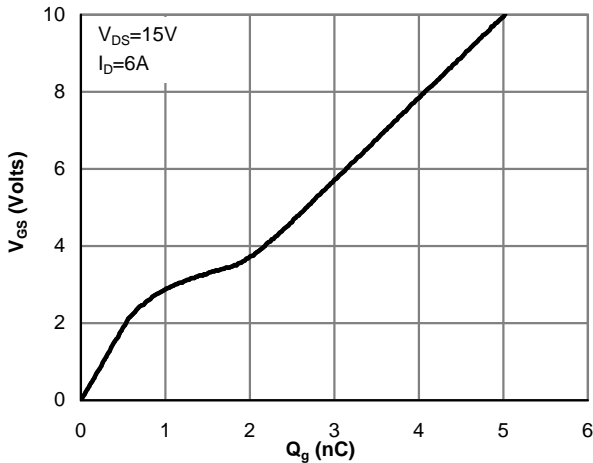


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

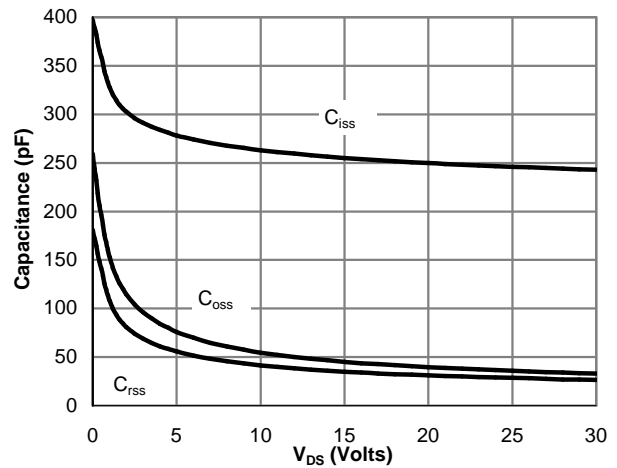


**Figure 6: Body-Diode Characteristics (Note E)**

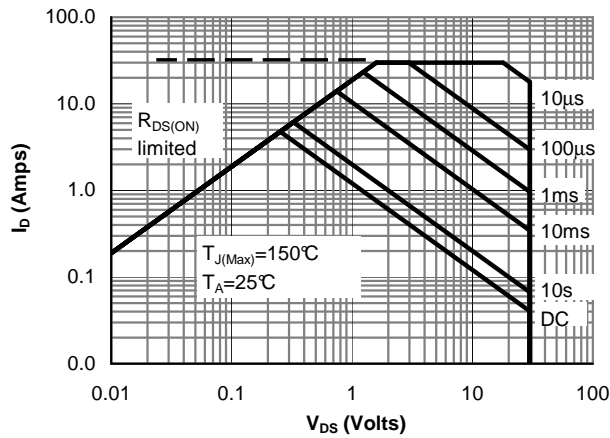
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



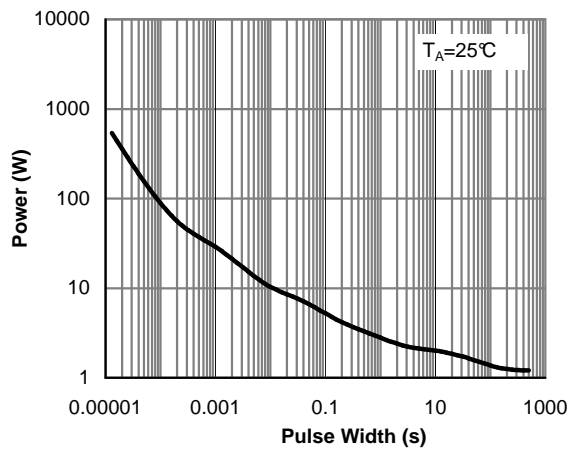
**Figure 7: Gate-Charge Characteristics**



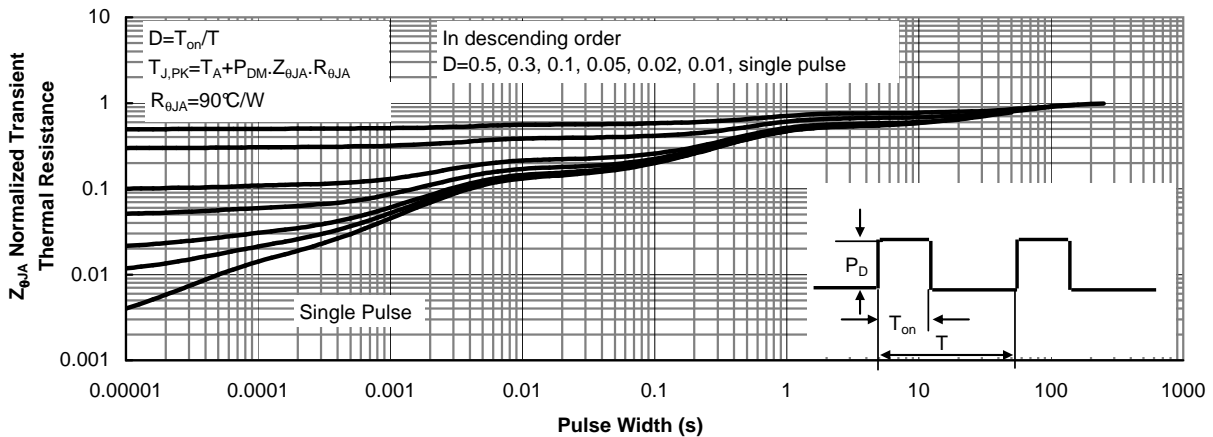
**Figure 8: Capacitance Characteristics**



**Figure 10: Maximum Forward Biased Safe Operating Area (Note F)**

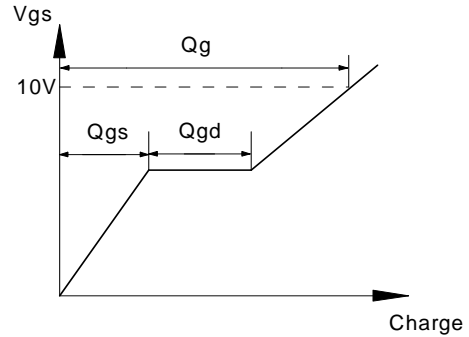
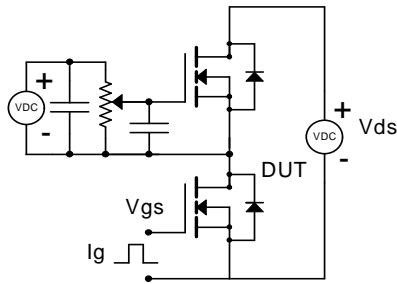


**Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)**

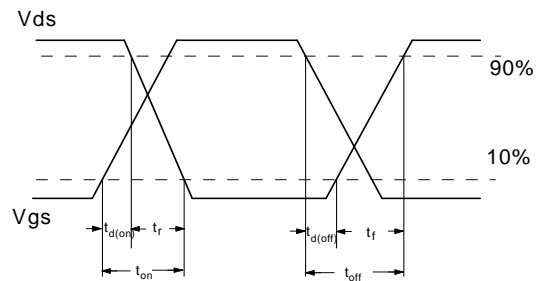
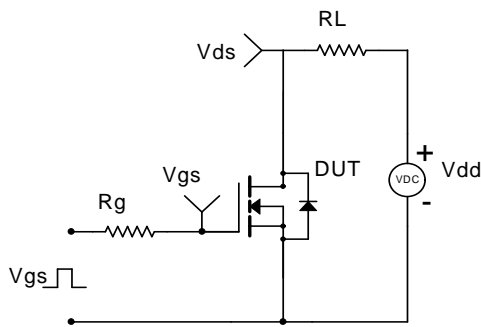


**Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)**

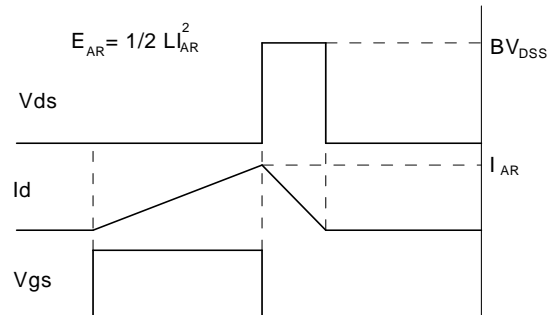
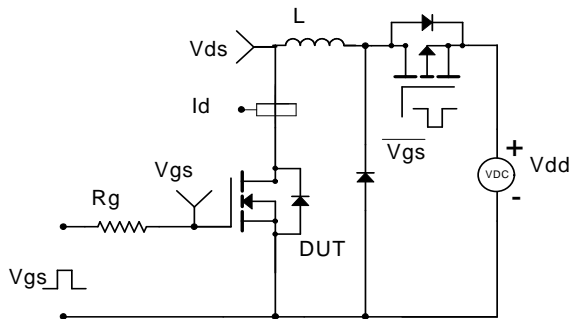
**Gate Charge Test Circuit & Waveform**



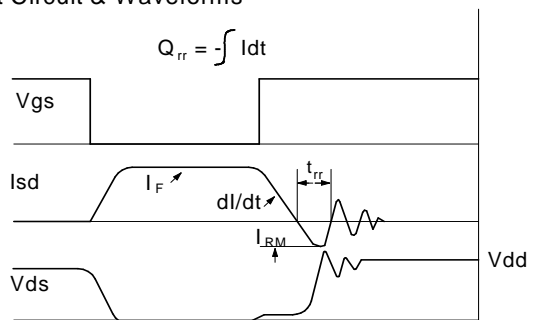
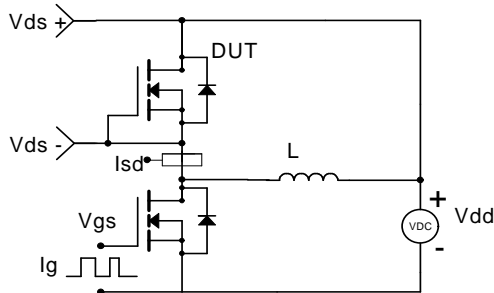
**Resistive Switching Test Circuit & Waveforms**



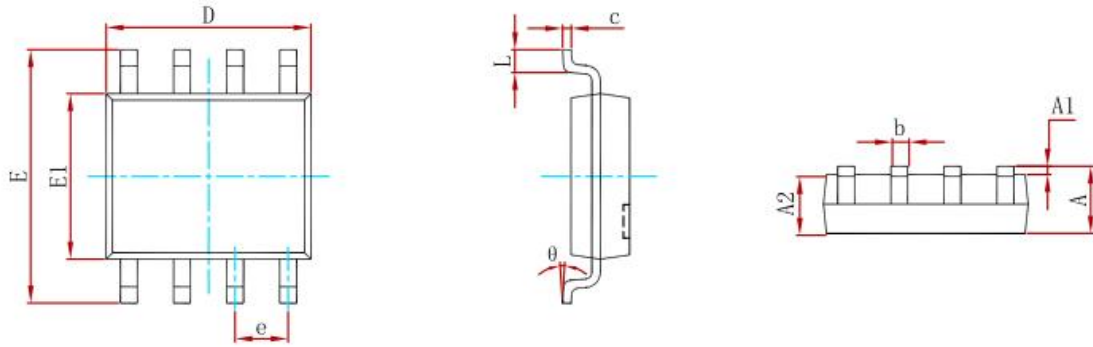
**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

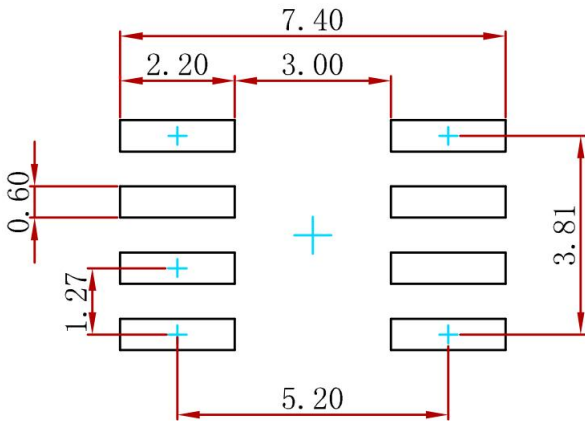


**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

**Suggested Pad Layout**



**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only

**REEL SPECIFICATION**

P/N	PKG	QTY
AO4812-MS	SOP--8	4000

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