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National Semiconductor

October 2007

LM48510 Boomer® Audio Power Amplifier Series
Boosted Class D Audio Power Amplifier

General Description

The LM48510 integrates a boost converter with a high efficiency mono, Class D audio power amplifier to provide 1.2W continuous power into an 8Ω speaker when operating on a 3.3V power supply with boost voltage (PV_1) of 5.0V. When operating on a 3.3V power supply, the LM48510 is capable of driving a 4Ω speaker load at a continuous average output of 1.7W with less than 1% THD+N. The Class D amplifier is a low noise, filterless PWM architecture that eliminates the output filter, reducing external component count, board area consumption, system cost, and simplifying design.

The LM48510's switching regulator is a current-mode boost converter operating at a fixed frequency of 0.6MHz.

The LM48510 is designed for use in mobile phones and other portable communication devices. The high (76%) efficiency extends battery life when compared to Boosted Class AB amplifiers. The LM48510 features a low-power consumption shutdown mode. Shutdown may be enabled by driving the Shutdown pin to a logic low (GND).

The gain of the Class D is externally configurable which allows independent gain control from multiple sources by summing the signals. Output short circuit and Thermal shutdown protection prevent the device from damage during fault conditions. Superior click and pop suppression eliminates audible transients during power-up and shutdown.

Key Specifications

- Quiescent Power Supply Current — 6mA (typ)
- Output Power (R_L = 8Ω, THD+N ≤ 1%, V_{DD} = 3.3V, PV_1 = 5.0V) — 1.2W (typ)
- Shutdown Current — 0.01µA (typ)

Features

- Click and Pop Suppression
- Low 0.01µA Shutdown Current
- 76% Efficiency
- Filterless Class D
- 2.7V - 5.0V operation (V_{DD})
- Externally configurable gain on Class D
- Very fast turn on time: 17µs
- Independent Boost and Amplifier shutdown pins

Applications

- Mobile Phones
- PDAs
- Portable media
- Cameras
- Handheld games

Typical Application

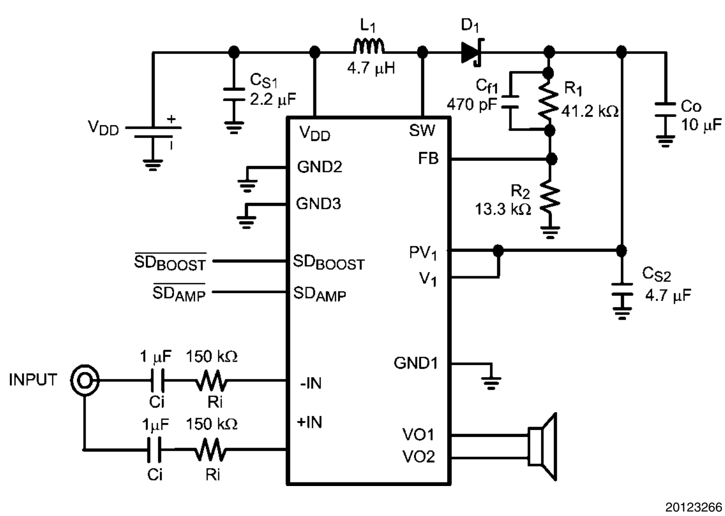

FIGURE 1. Typical LM48510 Audio Amplifier Application Circuit

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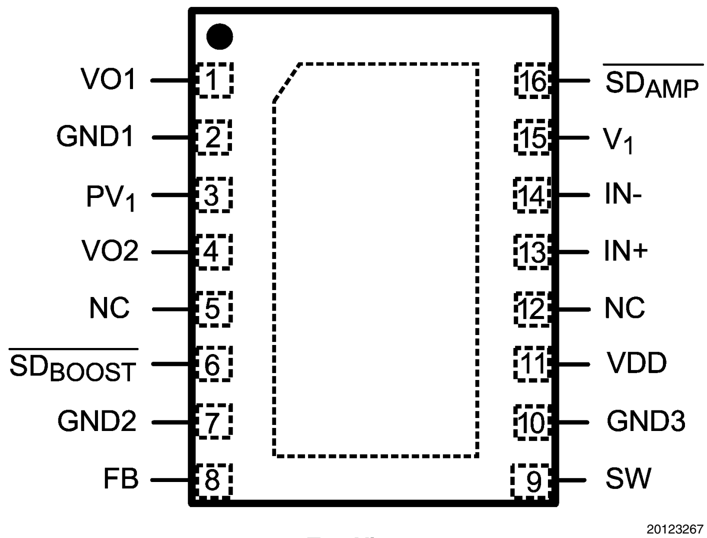
Connection Diagram

LM48510SD



Top View
Order Number LM48510SD
See NS Package Number SDA16B

LLP-14 Pin	Name	Function
1	VO1	Amplifier Output
2	GND1	Ground
3	PV1	Amplifier Power Input
4	VO2	Amplifier Output
5	NC1	No Connect
6	SD_{BOOST}	Boost Regulator Active Low Shutdown
7	GND2	Signal Ground (Booster)
8	FB	Feedback point that connects to external resistive divider
9	SW	Drain of the Internal FET Switch
10	GND3	Power Ground (Booster)
11	VDD	Power Supply
12	NC2	No Connect
13	IN+	Amplifier Non-Inverting Input
14	IN-	Amplifier Inverting Input
15	V1	Amplifier Power Input
16	SD_{AMP}	Amplifier Active Low Shutdown
DAP		To be soldered to board for enhanced thermal dissipation.

Absolute Maximum Ratings (Notes 2, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD}, V_1)	6V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150°C

Thermal Resistance

θ_{JA} (SD)	37°C/W

See AN-1187 'Leadless Leadframe Packaging (LLP)'

Operating Ratings

Temperature Range

$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (V_{DD})	$2.7V \le V_{DD} \le 5.0V$
Supply Voltage (V_1)	$4.5V \le V_1 \le 5.5V$

Electrical Characteristics V_{DD} = 3.3V (Notes 1, 2)

The following specifications apply for V_{DD} = 3.3V, $PV_1 = V_1$ = 5.0V, A_V = 6dB (R_i = 150kΩ), R_L = 15µH + 8Ω +15µH, f_{IN} = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48510		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, $R_{LOAD} = \infty$	6.06	8.75	mA (max)
I_{SD}	Shutdown Current	$SD_{AMP} = SD_{BOOST}$ = GND (Note 9)	0.01	1	µA (max)
V_{SDIH}	Shutdown Voltage Input High	SD1 Boost SD2 Amplifier		1.5 1.4	V (min) V (min)
V_{SDIL}	Shutdown Voltage Input Low	SD1 Boost SD2 Amplifier		0.5 0.4	V (max) V (max)
T_{WU}	Wake-up Time		17		µs
V_{OS}	Output Offset Voltage		10		mV
P_O	Output Power	R_L = 15µH + 4Ω + 15µH THD+N = 1% (max), f = 1kHz, 22kHz, BW V_{DD} = 3.3V	1.7		W
		R_L = 15µH + 8Ω + 15µH THD+N = 1% (max), f = 1kHz, 22kHz, BW V_{DD} = 3.3V	1.2	0.9	W (min)
		R_L = 15µH + 4Ω + 15µH THD+N = 10% (max), f = 1kHz, 22kHz, BW V_{DD} = 2.7V V_{DD} = 3.3V	1.11 1.9		W W
		R_L = 15µH + 8Ω + 15µH THD+N = 10% (max), f = 1kHz, 22kHz, BW V_{DD} = 2.7V V_{DD} = 3.3V	0.98 1.55		W W
THD+N	Total Harmonic Distortion + Noise	P_O = 500mW, f = 1kHz, R_L = 15µH + 8Ω + 15µH, V_{DD} = 2.7V	0.06		%
		P_O = 500mW, f = 1kHz, R_L = 15µH + 8Ω + 15µH, V_{DD} = 3.3V	0.07		%

Symbol	Parameter	Conditions	LM48510		Units (Limits)
			Typical (Note 6)	**Limit** (Notes 7, 8)	
ε_{OS}	Output Noise	V_{DD} = 3.3V, f = 20Hz – 20kHz Inputs to AC GND, No weighting input referred	67		μV_{RMS}
		V_{DD} = 3.3V, f = 20Hz – 20kHz Inputs to AC GND, A weighted input referred	47		μV_{RMS}
A_V	Gain		300kΩ/R_i		V/V
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} Sine, $f_{RIPPLE\,=}$ = 217Hz	89		dB
		V_{RIPPLE} = 200mV_{P-P} Sine, $f_{RIPPLE\,=}$ = 1kHz	83		dB
		V_{RIPPLE} = 200mV_{P-P} Sine, $f_{RIPPLE\,=}$ = 10kHz	55		dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 1V_{P-P}, f_{RIPPLE} = 217Hz	70		dB
η	Efficiency	P_O = 1W, f = 1kHz, R_L = 15µH + 8Ω + 15µH, V_{DD} = 3.3V	76		%
V_{FB}	Feedback Pin Reference Voltage	(Note 10)	1.23		V

Note 1: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in Absolute Maximum Ratings, whichever is lower.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

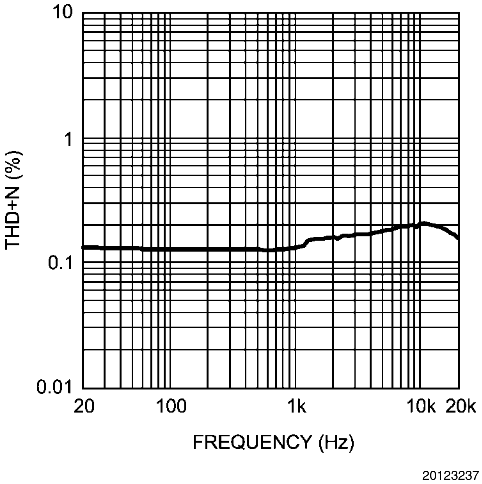
Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Shutdown current is measured with components R1 and R2 removed.

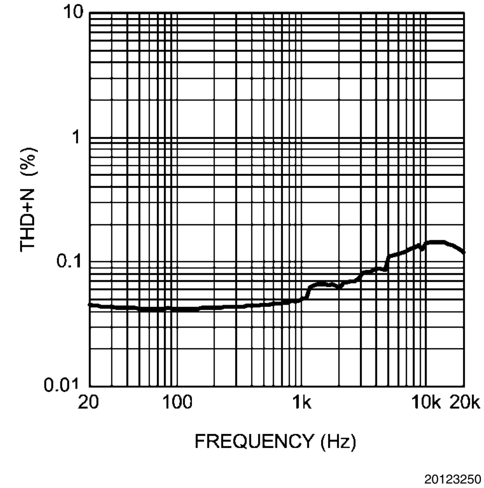
Note 10: Feedback pin reference voltage is measured with the Audio Amplifier disconnected from the Boost converter (the Boost converter is unloaded).

Typical Performance Characteristics

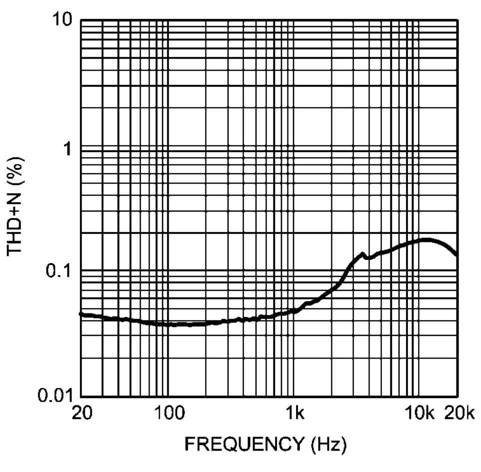
THD+N vs Frequency
V_{DD} = 2.7V, R_L = 15µH + 4Ω + 15µH



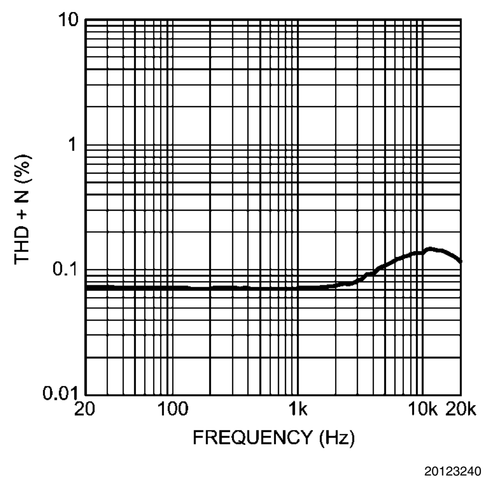
THD+N vs Frequency
V_{DD} = 2.7V, R_L = 15µH + 8Ω + 15µH



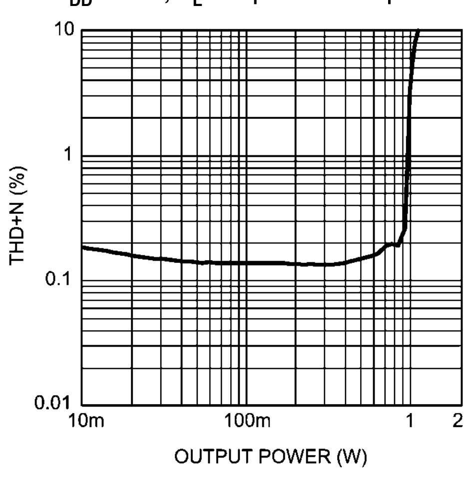
THD+N vs Frequency
V_{DD} = 3.3V, R_L = 15µH + 4Ω + 15µH



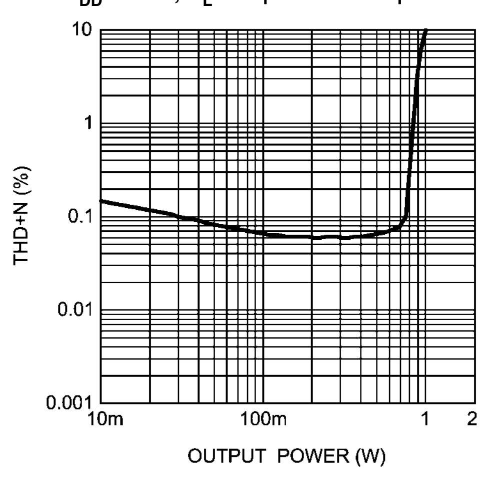
THD+N vs Frequency
V_{DD} = 3.3V, R_L = 15µH + 8Ω + 15µH



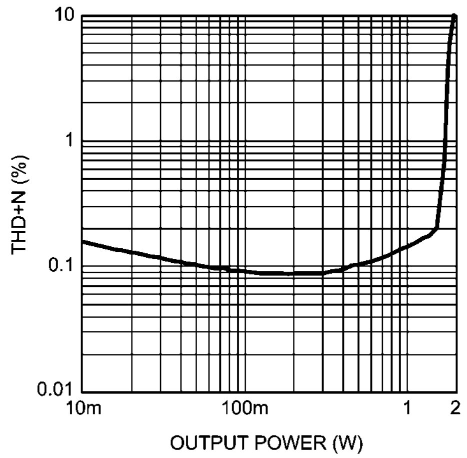
THD+N vs Output Power
V_{DD} = 2.7V, R_L = 15µH + 4Ω + 15µH



THD+N vs Output Power
V_{DD} = 2.7V, R_L = 15µH + 8Ω + 15µH



THD+N vs Output Power
V_{DD} = 3.3V, R_L = 15µH + 4Ω + 15µH



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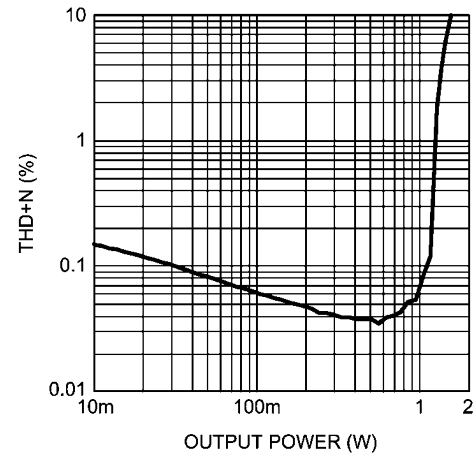
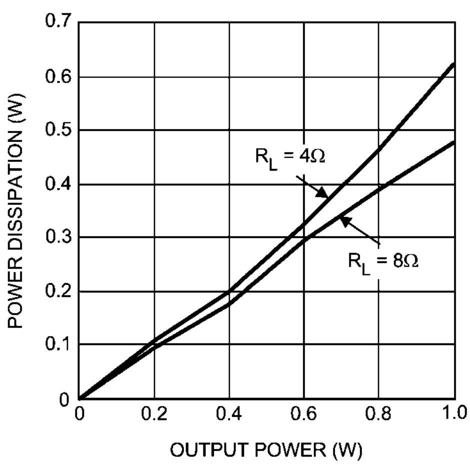
THD+N vs Output Power
V_{DD} = 3.3V, R_L = 15µH + 8Ω + 15µH



20123244

Power Dissipation vs Output Power
V_{DD} = 2.7V



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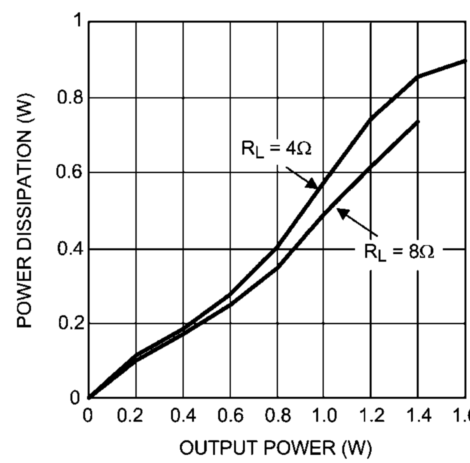
Power Dissipation vs Output Power
V_{DD} = 3.3V



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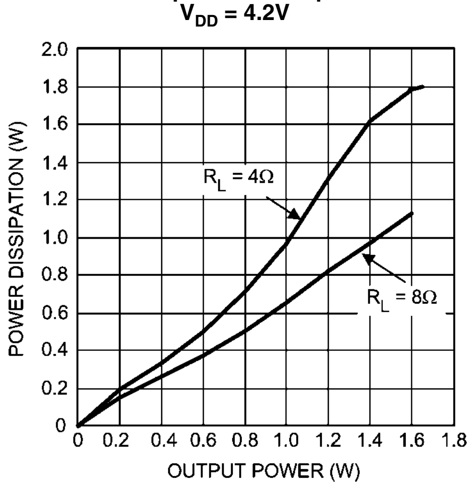
Power Dissipation vs Output Power
V_{DD} = 4.2V



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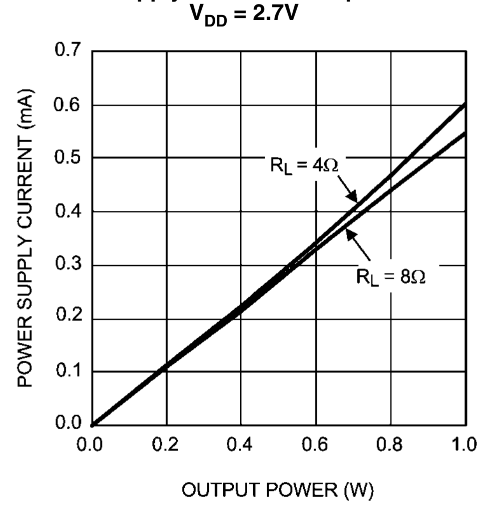
Power Supply Current vs Output Power
V_{DD} = 2.7V



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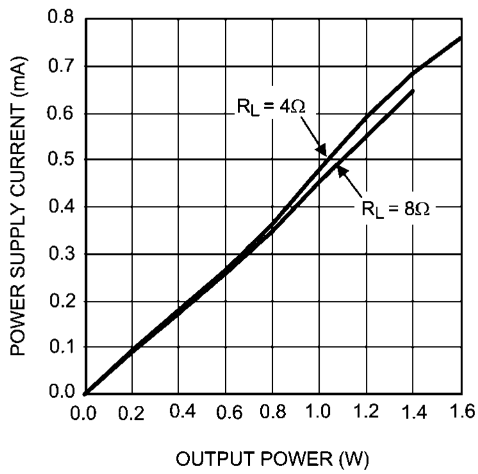
Power Supply Current vs Output Power
V_{DD} = 3.3V



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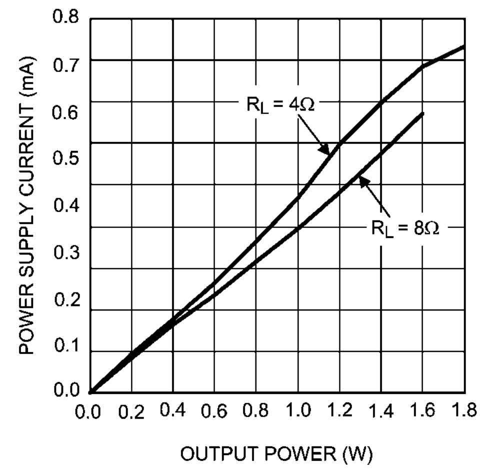
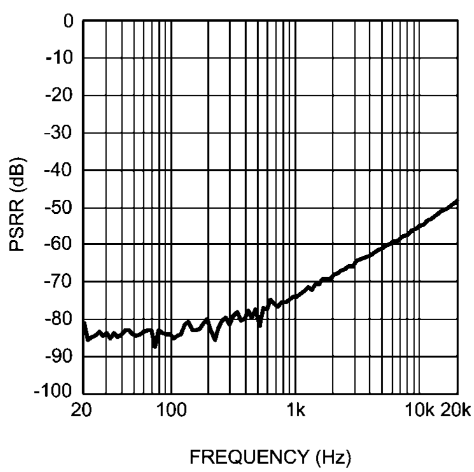
Power Supply Current vs Output Power
V_{DD} = 4.2V



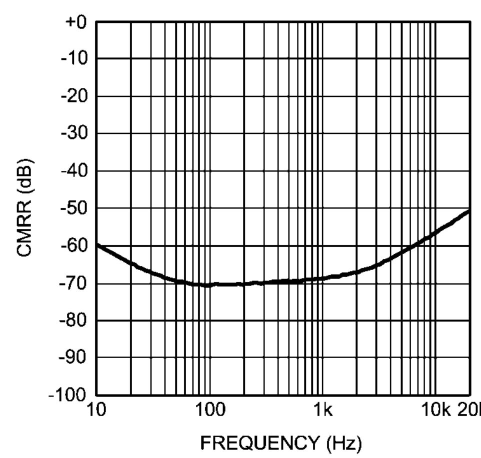
20123231

PSRR vs. Frequency
V_{DD} = 3.3V, R_L = 15µH + 8Ω + 15µH



20123232

CMRR vs Frequency
V_{DD} = 3.3V, R_L = 15µH + 8Ω + 15µH



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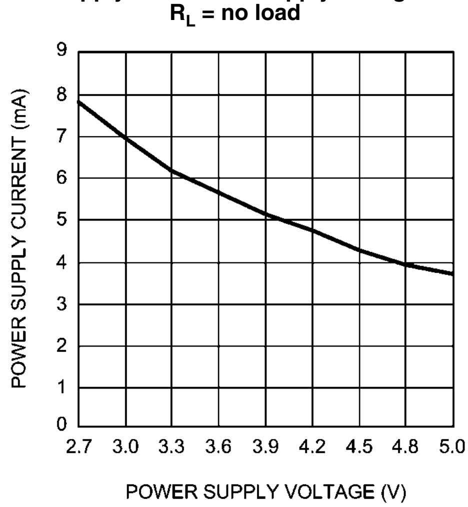
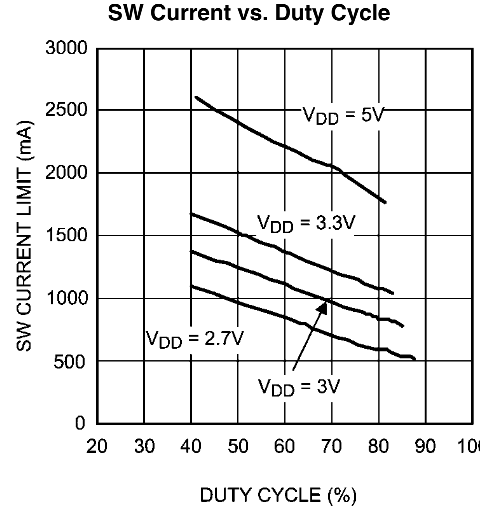
Supply Current vs. Supply Voltage
R_L = no load



20123233

SW Current vs. Duty Cycle



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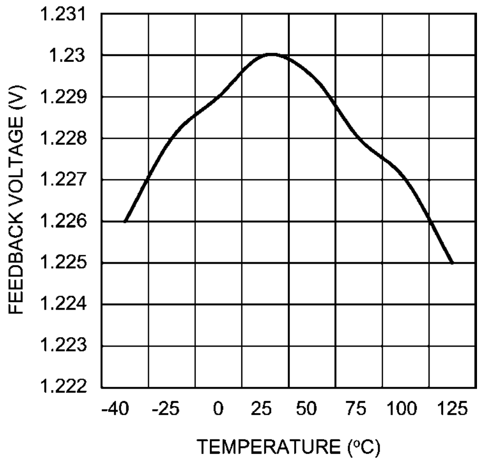
Feedback Voltage vs. Temperature



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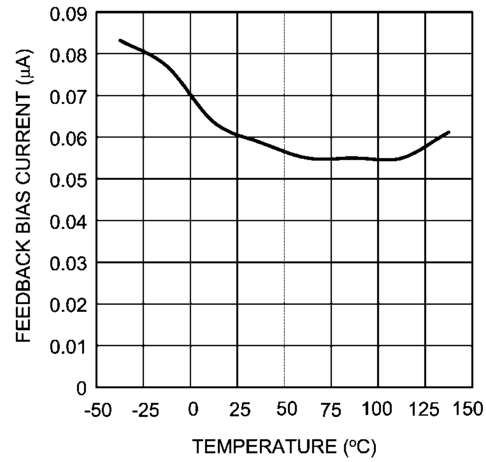
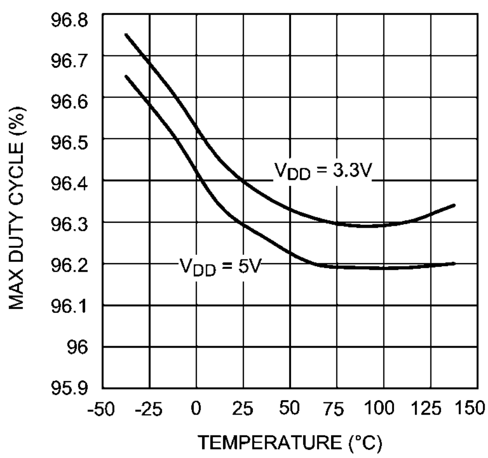
Feedback Bias Current vs. Temperature



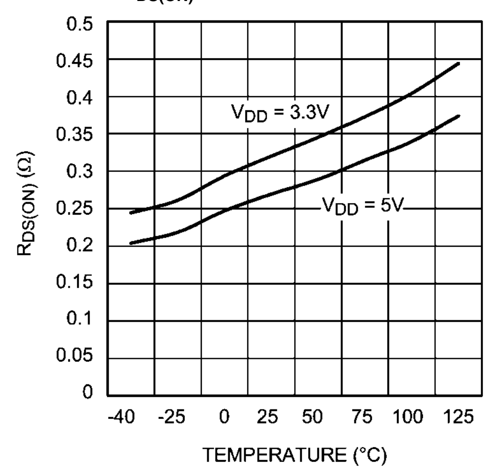
20123225

Max Duty Cycle vs. Temperature



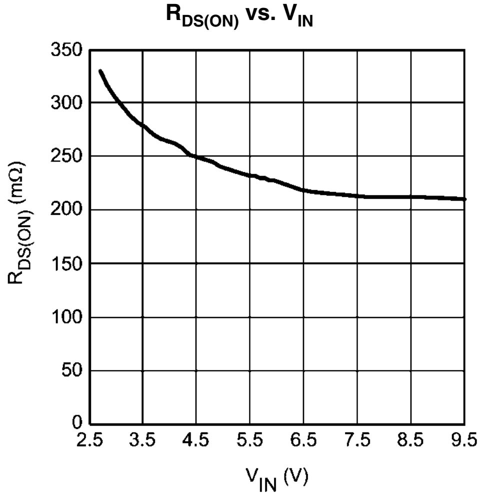
20123246

$R_{DS(ON)}$ vs. Temperature



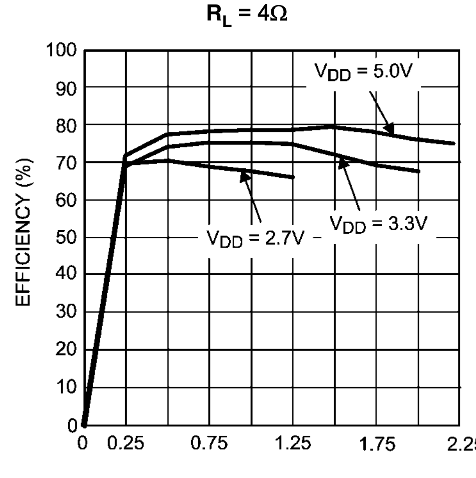
20123227

$R_{DS(ON)}$ vs. V_{IN}



20123228

Output Power vs. Efficiency
R_L = 4Ω



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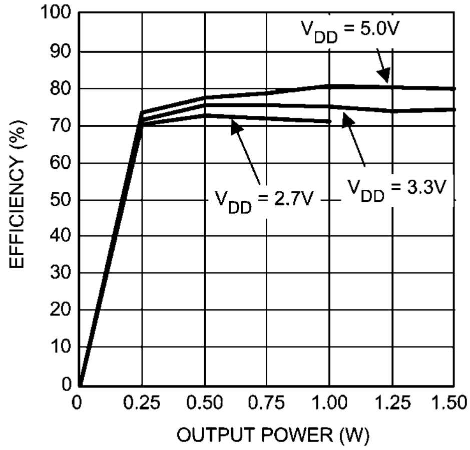
Output Power vs. Efficiency
$R_L = 8\Omega$



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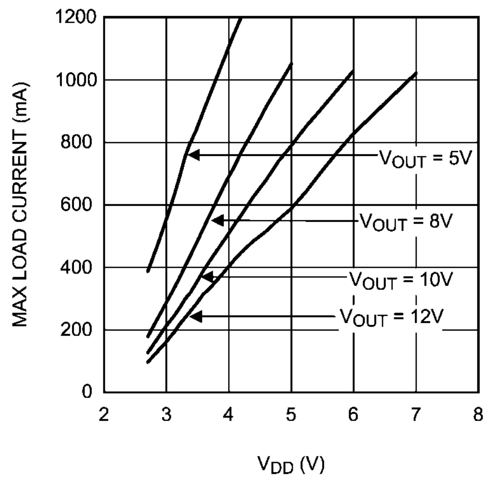
Boost Converter Max. Load Current vs. V_{DD}



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Application Information

GENERAL AMPLIFIER FUNCTION

The audio amplifier portion of LM48510 is a Class D featuring a filterless modulation scheme. The differential outputs of the device switch at 300kHz from PV_1 to GND. When there is no input signal applied, the two outputs (VO1 and VO2) switch with a 50% duty cycle, with both outputs in phase. Because the outputs of the Class D are differential, the two signals cancel each other. This results in no net voltage across the speaker, thus there is no load current during an idle state, conserving power.

With an input signal applied, the duty cycle (pulse width) of the Class D outputs changes. For increasing output voltages, the duty cycle of VO1 increases, while the duty cycle of VO2 decreases. For decreasing output voltages, the converse occurs, the duty cycle of VO2 increases while the duty cycle of VO1 decreases. The difference between the two pulse widths yields the differential output voltage.

OPERATING RATINGS

The LM48510 has independent power supplies for the Class D audio power amplifier (PV_1, V_1) and the Boost Converter (V_{DD}). The Class D amplifier operating rating is $2.4V \leq (PV_1, V_1) \leq 5.5V$ when being used without the Boost.

Note the output voltage (PV_1, V_1) has to be more than V_{DD}.

DIFFERENTIAL AMPLIFIER EXPLANATION

As logic supply voltages continue to shrink, designers are increasingly turning to differential analog signal handling to preserve signal to noise ratios with restricted voltage swing. The amplifier portion of the LM48510 is a fully differential amplifier that features differential input and output stages. A differential amplifier amplifies the difference between the two input signals. Traditional audio power amplifiers have typically offered only single-ended inputs resulting in a 6dB reduction in signal to noise ratio relative to differential inputs. The amplifier also offers the possibility of DC input coupling which eliminates the two external AC coupling, DC blocking capacitors. The amplifier can be used, however, as a single ended input amplifier while still retaining it's fully differential benefits. In fact, completely unrelated signals may be placed on the input pins. The amplifier portion of the LM48510 simply amplifies the difference between the signals. A major benefit of a differential amplifier is the improved common mode rejection ratio (CMRR) over single input amplifiers. The common-mode rejection characteristic of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in high noise applications.

AMPLIFIER DISSIPATION

In general terms, efficiency is considered to be the ratio of useful work output divided by the total energy required to produce it with the difference being the power dissipated, typically, in the IC. The key here is “useful” work. For audio systems, the energy delivered in the audible bands is considered useful including the distortion products of the input signal. Sub-sonic (DC) and super-sonic components (>22kHz) are not useful. The difference between the power flowing from the power supply and the audio band power being transduced is dissipated in the LM48510 and in the transducer load. The amount of power dissipation in the LM48510 is very low. This is because the ON resistance of the switches used to form the output waveforms is typically less than 0.25Ω. This leaves only the transducer load as a potential "sink" for the small excess of input power over audio band output power. The amplifier dissipates only a fraction of the excess power requiring no additional PCB area or copper plane to act as a heat sink.

BOOST CONVERTER POWER DISSIPATION

At higher duty cycles, the increased ON time of the FET means the maximum output current will be determined by power dissipation within the boost converter FET switch. The switch power dissipation from ON-state conduction is calculated by Equation 1.

$$P_{DMAX(SWITCH)} = DC \times I_{IND}(AVE)^2 \times R_{DS(ON)} \quad (1)$$

Where DC is the duty cycle.

There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.

SHUTDOWN FUNCTION

To reduce power consumption while not in use, the amplifier of LM48510 contains shutdown circuitry that reduces current draw to less than 0.01µA. It is best to switch between ground and supply (PV_1, V_1) for minimum current usage while in the shutdown state. While the LM48510 may be disabled with shutdown voltages in between ground and supply, the idle current will be greater than the typical 0.01µA value. Increased THD may also be observed with voltages less than V_{DD} on the SD_{AMP} pin when in PLAY mode.

The amplifier has an internal resistor connected between GND and SD_{AMP} pins. The purpose of this resistor is to eliminate any unwanted state changes when the SD_{AMP} pin is floating. The amplifier will enter the shutdown state when the SD_{AMP} pin is left floating or if not floating, when the shutdown voltage has crossed the threshold. To minimize the supply current while in the shutdown state, the SD_{AMP} pin should be driven to GND or left floating. If the SD_{AMP} pin is not driven to GND, the amount of additional resistor current due to the internal shutdown resistor can be found by Equation (2) below.

$$(V_{SD} - GND) / 300k\Omega \quad (2)$$

With only a 0.5V difference, an additional 1.7µA of current will be drawn while in the shutdown state.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch, and a pull-up resistor. One terminal of the switch is connected to GND. The other side is connected to the two shutdown pins and the terminal of the pull-up resistor. The remaining resistance terminal is connected to V_{DD}. If the switch is open, then the external pull-up resistor connected to V_{DD} will enable the LM48510. This scheme guarantees that the shutdown pins will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers, and switching DC-DC converters, is critical for optimizing device and system performance. Consideration to component values must be used to maximize overall system quality.

The best capacitors for use with the switching converter portion of the LM48510 are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency, which makes them optimum for high frequency switching converters.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden, AVX, and Murata.

The gain of the amplifier is set by the external resistors, Ri in Figure 1. The gain is given by Equation (3) below. Best THD +N performance is achieved with a gain of 2V/V (6dB).

$$A_V = 2 * 150k\Omega / R_i \ (V/V) \tag{3}$$

It is recommended that resistors with 1% tolerance or better be used to set the gain of the amplifier. The Ri resistors should be placed close to the input pins of the amplifier. Keeping the input traces close to each other and of the same length in a high noise environment will aid in noise rejection due to the good CMRR of the Class D. Noise coupled onto input traces which are physically close to each other will be common mode and easily rejected by the amplifier.

Input capacitors may be needed for some applications or when the source is single-ended (see Figure1). Input capacitors are needed to block any DC voltage at the source so that the DC voltage seen between the input terminals of the Class D is 0V. Input capacitors create a high-pass filter with the input resistors, R_i. The –3dB point of the high-pass filter is found using Equation (4) below.

$$f_C = 1 / (2\pi R_i C_i) \ (Hz) \tag{4}$$

The input capacitors may also be used to remove low audio frequencies. Small speakers cannot reproduce low bass frequencies so filtering may be desired . When the Class D is using a single-ended source, power supply noise on the ground is seen as an input signal by the +IN input pin that is capacitor coupled to ground. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, will filter out this noise so it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching.

POWER SUPPLY BYPASSING FOR AMPLIFIER

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor (Cs2, see Figure 1) location on both PV_1 and V_1 pin should be as close to the device as possible.

SELECTING INPUT CAPACITOR FOR AUDIO AMPLIFIER

One of the major considerations is the closedloop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

High value input capacitors are both expensive and space hungry in portable designs. Clearly, a certain value capacitor is needed to couple in low frequencies without severe attenuation. But ceramic speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a high value input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is affected by the value of the input coupling capacitor, C_i. A high value input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor value based on desired low frequency response, turn-on pops can be minimized.

SELECTING OUTPUT CAPACITOR (C_O) FOR BOOST CONVERTER

A single 4.7µF to 10µF ceramic capacitor will provide sufficient output capacitance for most applications. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used. Aluminum electrolytics with ultra low ESR such as Sanyo Os-con can be used, but are usually prohibitively expensive. Typical electrolytic capacitors are not suitable for switching frequencies above 500 kHz because of significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

In general, if electrolytics are used, it is recommended that they be paralleled with ceramic capacitors to reduce ringing, switching losses, and output voltage ripple.

SELECTING INPUT CAPACITOR (Cs1) FOR BOOST CONVERTER

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. A nominal value of 4.7µF is recommended, but larger values can be used. Since this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.

SETTING THE OUTPUT VOLTAGE (V_1) OF BOOST CONVERTER

The output voltage is set using the external resistors R1 and R2 (see Figure 1). A value of approximately 13.3kΩ is recommended for R2 to establish a divider current of approximately 92µA. R1 is calculated using the formula:

$$R1 = R2 \ X \ (V_1/1.23 - 1) \tag{5}$$

FEED-FORWARD COMPENSATION FOR BOOST CONVERTER

Although the LM48510's internal Boost converter is internally compensated, the external feed-forward capacitor C_{f1} is required for stability (see Figure 1). Adding this capacitor puts a zero in the loop response of the converter. The recommended frequency for the zero fz should be approximately 6kHz. C_{f1} can be calculated using the formula:

$$C_{f1} = 1 / (2\pi \ X \ R1 \ X \ fz) \tag{6}$$

SELECTING DIODES FOR BOOST

The external diode used in Figure 1 should be a Schottky diode. A 20V diode such as the MBR0520 is recommended.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5A. For applications exceeding 0.5A average but less than 1A, a Microsemi UPS5817 can be used.

DUTY CYCLE

The maximum duty cycle of the boost converter determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

$$\text{Duty Cycle} = V_1 + V_{DIODE} - V_{DD} \,/\, V_1 + V_{DIODE} - V_{SW}$$

This applies for continuous mode operation.

INDUCTANCE VALUE

The inductor is the largest sized component and usually the most costly. “How small can the inductor be?” The answer is not simple and involves trade-offs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

$$E = L/2 \text{ X } (Ip)2$$

Where Ip is the peak inductor current. An important point to observe is that the LM48510 will limit its switch current based on peak current. This means that since Ip(max) is fixed, increasing L will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in “continuous” mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. It should be noted that all boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays “continuous” over a wider load current range.

To better understand these trade-offs, a typical application circuit (5V to 12V boost with a 10µH inductor) will be analyzed. We will assume:

$$V_{IN} = 5V,\ V_{OUT} = 12V,\ V_{DIODE} = 0.5V,\ V_{SW} = 0.5V$$

Since the frequency is 0.6MHz (nominal), the period is approximately 1.66µs. The duty cycle will be 62.5%, which means the ON-time of the switch is 1.04µs. It should be noted that when the switch is ON, the voltage across the inductor is approximately 4.5V. Using the equation:

$$V = L\ (di/dt)$$

We can then calculate the di/dt rate of the inductor which is found to be 0.17 A/µs during the ON-time. Using these facts, we can then show what the inductor current will look like during operation:

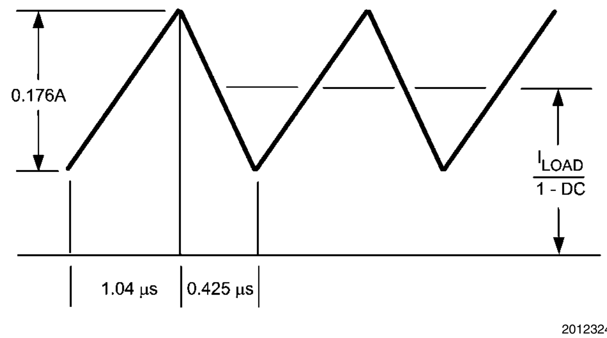

FIGURE 2. 10µH Inductor Current 5V - 12V Boost (LM48510)

During the 1.04µs ON-time, the inductor current ramps up 0.176A and ramps down an equal amount during the OFF-time. This is defined as the inductor “ripple current”. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values.

MAXIMUM SWITCH CURRENT

The maximum FET switch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in a graph in the typical performance characterization section which shows typical values of switch current as a function of effective (actual) duty cycle.

CALCULATING OUTPUT CURRENT OF BOOST CONVERTER (I_{AMP})

As shown in Figure 2 which depicts inductor current, the load current is related to the average inductor current by the relation:

$$I_{LOAD} = I_{IND}(AVG) \times (1 - DC) \qquad (7)$$

Where "DC" is the duty cycle of the application. The switch current can be found by:

$$I_{SW} = I_{IND}(AVG) + 1/2\ (I_{RIPPLE}) \qquad (8)$$

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

$$I_{RIPPLE} = DC \times (V_{IN}\text{-}V_{SW}) / (f \times L) \qquad (9)$$

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

$$I_{LOAD}(max) = (1–DC)x(I_{SW}(max)–DC(V_{IN}\text{-}V_{SW}))/2fL \qquad (10)$$

The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode.

DESIGN PARAMETERS V_{SW} AND I_{SW}

The value of the FET ON voltage (referred to as V_{SW} in equations 4 thru 7) is dependent on load current. A good approximation can be obtained by multiplying the $R_{DS(ON)}$ of the FET times the average inductor current.

FET on resistance increases at V_{IN} values below 5V, since the internal N-FET has less gate voltage in this input voltage range (see Typical Performance Characteristics curves). Above V_{IN} = 5V, the FET gate voltage is internally clamped to 5V.

The maximum peak switch current the device can deliver is dependent on duty cycle. For higher duty cycles, see Typical Performance Characteristics curves.

INDUCTOR SUPPLIERS

Recommended suppliers of inductors for the LM48510 include, but are not limited to Taiyo-Yuden, Sumida, Coilcraft, Panasonic, TDK and Murata. When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

PCB LAYOUT GUIDELINES

High frequency boost converters require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM48510 device. It is recommended that a four layer PCB be used so that internal ground planes are available.

Some additional guidelines to be observed:

1. Keep the path between L1, D1, and Co extremely short. Parasitic trace inductance in series with D1 and Co will increase noise and ringing.

2. The feedback components R1, R2 and C_{f1} must be kept close to the FB pin to prevent noise injection on the FB pin trace.

3. If internal ground planes are available (recommended) use vias to connect directly to ground at pin 2 of U1, as well as the negative sides of capacitors C_s1 and Co.

GENERAL MIXED-SIGNAL LAYOUT RECOMMENDATION

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

Power and Ground Circuits

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power / Ground Connection

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to place digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and crosstalk.

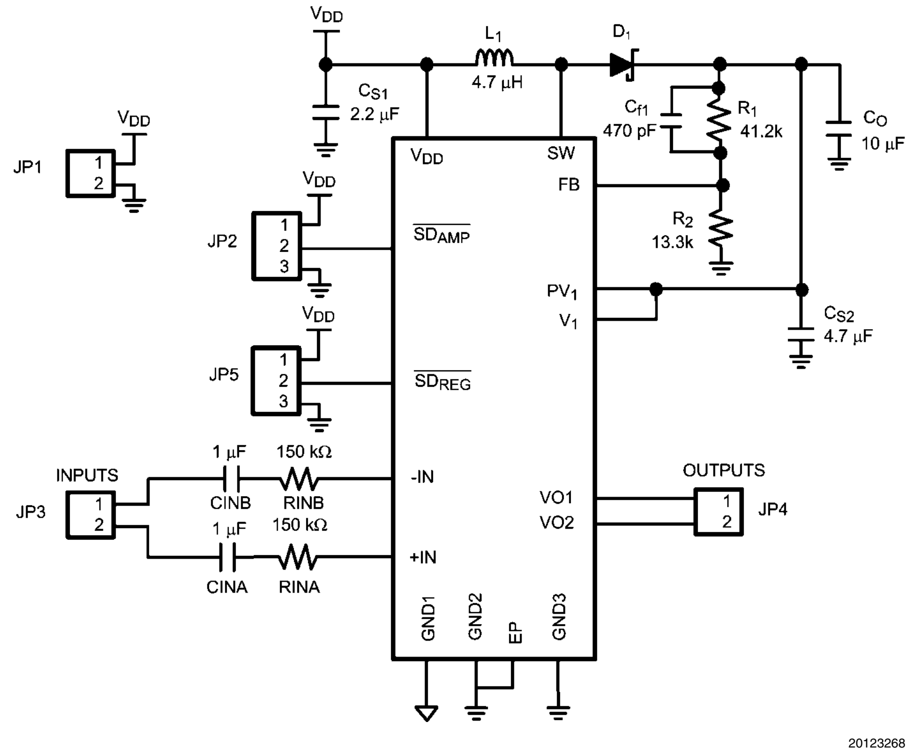

FIGURE 3. Demo Board Schematic Reference

Demonstration Board Layout

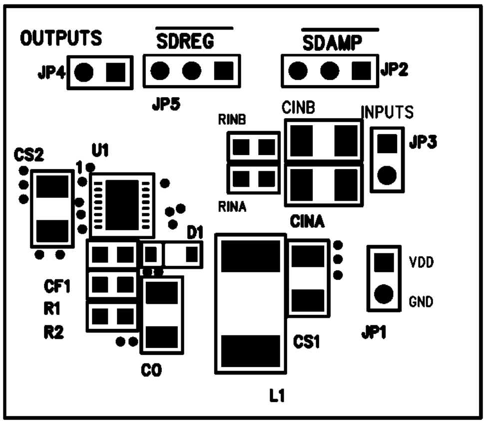

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FIGURE 4. Top Layer Silkscreen

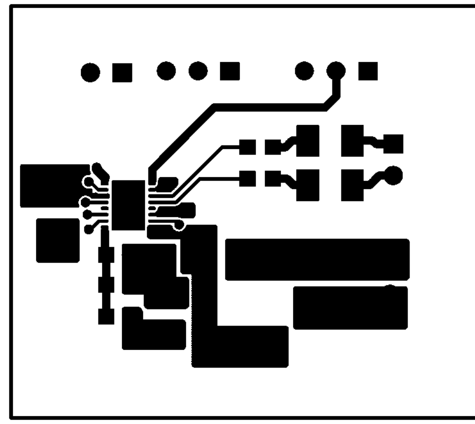

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FIGURE 5. Top Trace Layer

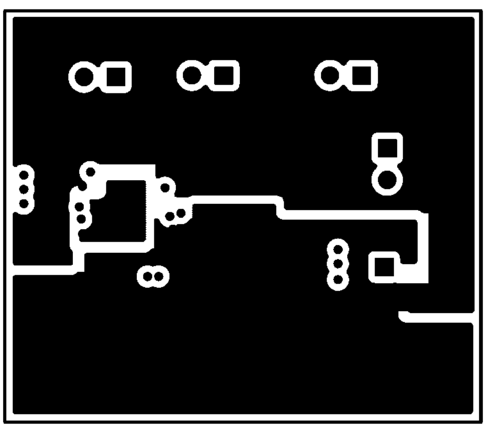

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FIGURE 6. GND Layer (middle 1)

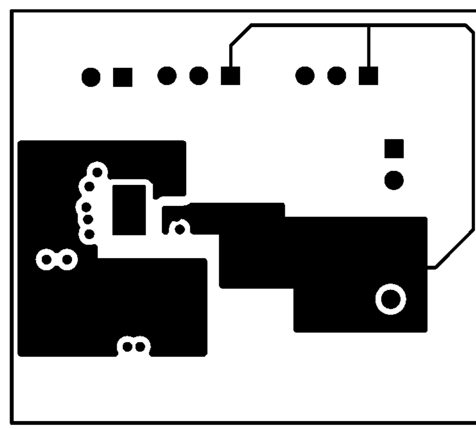

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FIGURE 7. Power Trace Layer (middle 2)

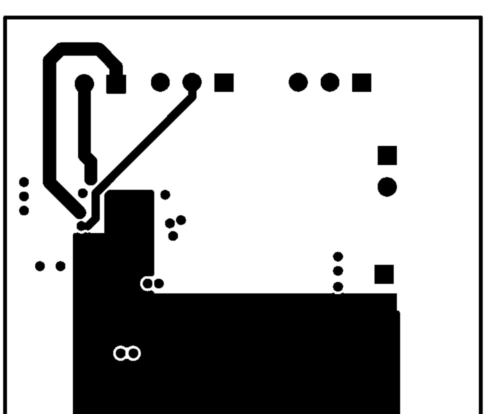

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FIGURE 8. Bottom Layer

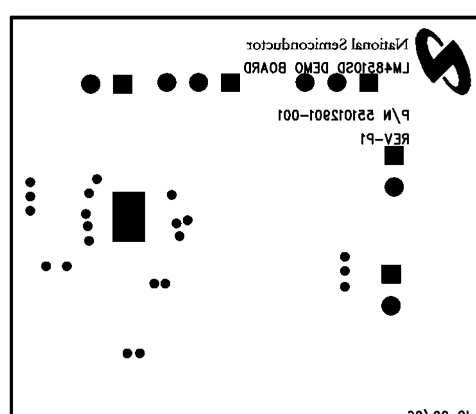

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FIGURE 9. Bottom Silkscreen

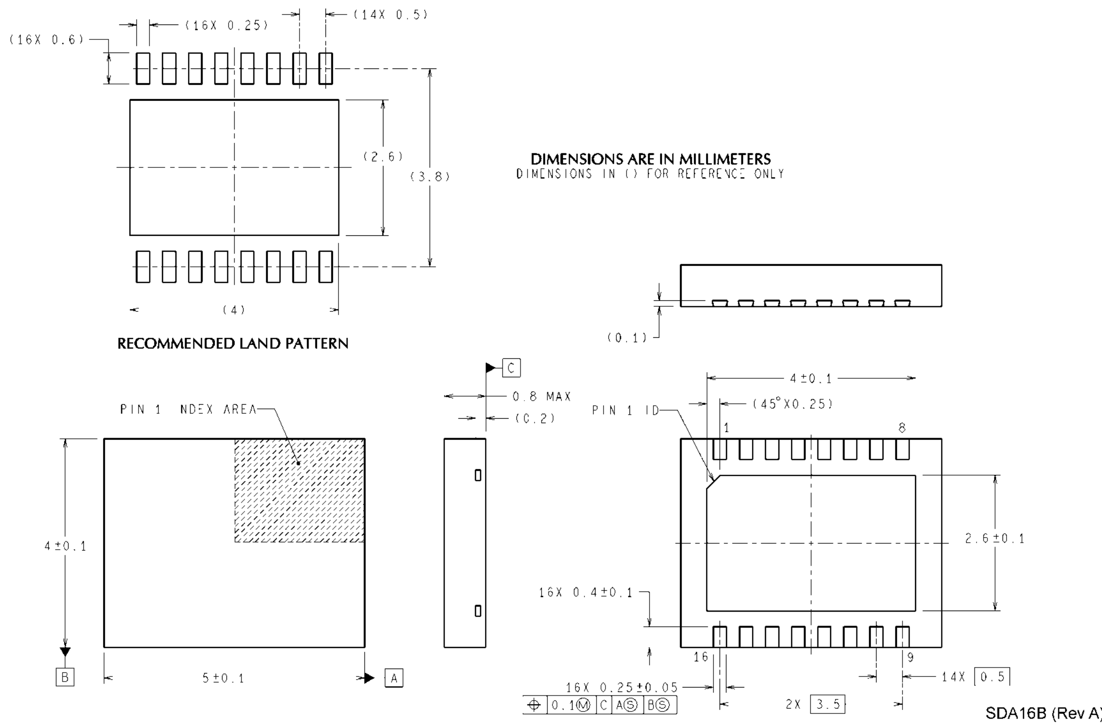
Build Of Material

Designator	Description	Footprint	Quantity	Value
Cf1	CHIP CAPACITOR GENERIC	CAP 0805	1	470pF
CINA	CHIP CAPACITOR GENERIC	CAP 1210	1	1µF
CINB	CHIP CAPACITOR GENERIC	CAP 1210	1	1µF
Co	CHIP CAPACITOR GENERIC	CAP 1210	1	10µF
Cs1	CHIP CAPACITOR GENERIC	CAP 1210	1	2.2µF
Cs2	CHIP CAPACITOR GENERIC	CAP 1210	1	4.7µF
D1	SCHOTTKY DIO	DIODE MBR0520 IR	1	
L1		IND_COILCRAFT-DO1813P	1	4.7µH
R1	CHIP RESISTOR GENERIC	RES 0805	1	41.2K
R2	CHIP RESISTOR GENERIC	RES 0805	1	13.3K
RINA	CHIP RESISTOR GENERIC	RES 0805	1	150K
RINB	CHIP RESISTOR GENERIC	RES 0805	1	150K

Revision History

Rev	Date	Description
1.0	11/16/06	Initial release.
1.1	03/07/07	Changed the Limit value on the V_{SDIH} and V_{SDIL} to 1.5 and 0.5 respectively.
1.2	10/15/07	Changed the typical value of Vfb = 1.24 to 1.23

Physical Dimensions inches (millimeters) unless otherwise noted



LLP Package
Order Number LM48510SD
NS Package Number SDA16B

Notes

Notes

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