March 2001

National Semiconductor

CLC452
Single Supply, Low Power, High Output, Current Feedback Amplifier

General Description

The CLC452 has a new output stage that delivers high output drive current (100mA), but consumes minimal quiescent supply current (3.0mA) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the −3dB frequency.

The CLC452 offers superior dynamic performance with a 130MHz small signal bandwidth, 400V/µs slew rate and 4.5ns rise/fall times ($2V_{STEP}$. The combination of low quiescent power, high output current drive, and high speed performance make the CLC452 well suited for many battery powered personal communication/computing systems.

The ability to drive low impedance, high capacitive loads, makes the CLC452 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC452 will drive a 100Ω load with only −75/−74dBc second/third harmonic distortion (A_V = +2, V_{OUT} = $2V_{PP}$, f =1MHz). With a 25Ω load, and the same conditions, it produces only −65/−77dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high resolution A/D converters, the CLC452 provides excellent −78/−85dBc second/third harmonic distortion (A_V = +2, V_{OUT} = $2V_{PP}$, f =1MHz, R_L = 1kΩ) and fast settling time.

Available in SOT23-5, the CLC452 is ideal for applications where space is critical.

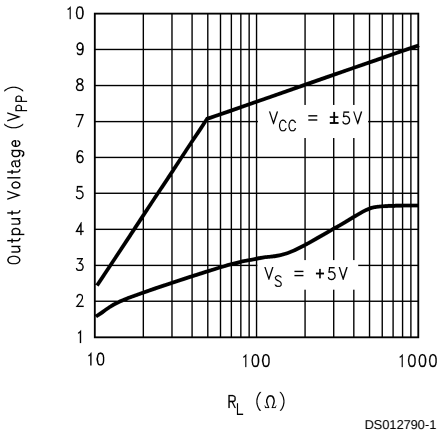
Features

- 100mA output current
- 3.0mA supply current
- 130MHz bandwidth (A_V = +2)
- −78/−85dBc HD2/HD3 (1MHz)
- 25ns settling to 0.05%
- 400V/µs slew rate
- Stable for capacitive loads up to 1000pF
- Single 5V to ±5V supplies
- Available in Tiny SOT23-5 package

Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery powered applications
- A/D driver

Maximum Output Voltage vs. R_L



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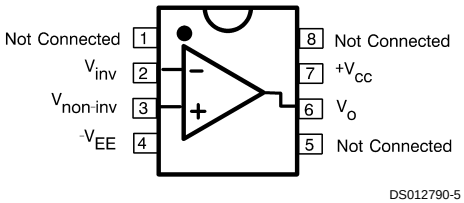
Connection Diagrams



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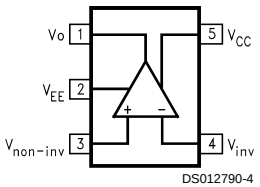
Pinout
DIP & SOIC



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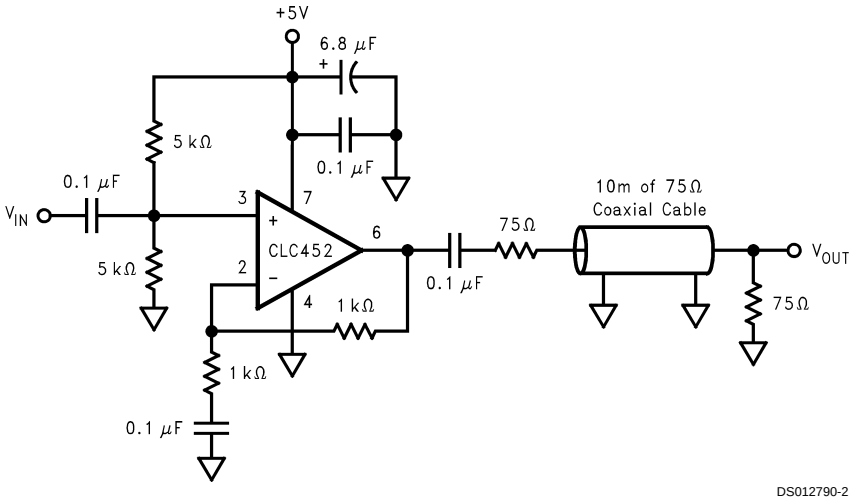
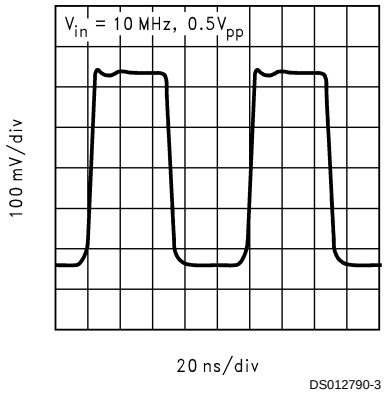
Pinout
SOT23-5

Typical Application



Single Supply Cable Driver



Response After 10m of Cable

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC452AJP	CLC452AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC452AJE	CLC452AJE	M08A
5-pin SOT	−40˚C to +85˚C	CLC452AJM5	A21	MA05A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}-(V_{EE})	+14V
Output Current (see note 3)	140mA
Common Mode Input Voltage	V_{EE} to V_{CC}
Maximum Junction Temperature	+150˚C
Storage Operating Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD Rating (human body model)	500V

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	105˚C/W	155˚C/W
SOIC	95˚C/W	175˚C/W
SOT23	140˚C/W	210˚C/W

+5V Electrical Characteristics

A_V = +2, V_S = +5V(Note 5), V_{CM} = V_{EE} + (V_S/2), R_L = 100Ω, R_f = 1kΩ, R_L tied to V_{CM}; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Ambient Temperature		CLC452AJ	+25˚C	+25˚C	0 to 70˚C	−40 to 85˚C	
Frequency Domain Response							
	-3dB Bandwidth	V_O <0.5V_{PP}	130	95	90	85	MHz
		V_O <2.0V_{PP}	95	80	77	75	MHz
	−0.1dB Bandwidth	V_O <0.5V_{PP}	30	25	20	20	MHz
	Gain Peaking	<200MHz, V_O <0.5V_{PP}	0	0.5	0.9	1.0	dB
	Gain Rolloff	<30MHz V_O <0.5V_{PP}	0.1	0.3	0.3	0.3	dB
	linear phase deviation	<30MHz, V_O = 0.5V_{PP}	0.1	0.2	0.3	0.3	deg
TIME DOMAIN RESPONSE							
	Rise and Fall Time	2V Step	4.5	6.0	6.4	6.8	ns
	Settling Time to ±0.05%	1V Step	25	-	-	-	ns
	Overshoot	2V Step	11	15	18	18	%
	Slew Rate	2V Step	400	300	275	260	V/µs
DISTORTION AND NOISE RESPONSE							
	2nd Harmonic Distortion	2V_{PP}, 1MHz	−75	−69	−67	−67	dBc
		2V_{PP},1MHz R_L = 1kΩ	−78	−70	−68	−68	dBc
		2V_{PP}, 5MHz	−65	−58	−56	−56	dBc
	3rd Harmonic Distortion	2V_{PP}, 1MHz	−74	−70	−68	−68	dBc
		2V_{PP}, 1MHz R_L=1kΩ	−85	−75	−73	−73	dBc
		2V_{PP}, 5MHz	−60	−55	−53	−53	dBc
	Equivalent Input Noise						
	Voltage (e_{ni})	>1MHz	2.8	3.5	3.8	3.8	nV/$\sqrt{Hz}$
	Non-Inverting Current (i_{bn})	>1MHz	7.5	10	11	11	pA/$\sqrt{Hz}$
	Non-Inverting Current (i_{bi})	>1MHz	10.5	14	15	15	pA/$\sqrt{Hz}$
Static, DC Performance							
	Input Offset Voltage (Note 4)		1	4	6	6	mV
	Average Drift		8	-	-	-	µV/˚C
	Input Bias Current (non-inverting) (Note 4)		6	18	22	24	µA
	Average Drift		40	-	-	-	nA/˚C
	Input Bias Current (inverting) (Note 4)		6	14	16	17	µA
	Average Drift		25	-	-	-	nA/˚C
	Power Supply Rejection Ratio	DC	48	45	43	43	dB
	Common-Mode Rejection Ratio	DC	51	48	46	46	dB

+5V Electrical Characteristics (Continued)

A_V = +2, V_S = +5V(Note 5), V_{CM} = V_{EE} + (V_S/2), R_L = 100Ω, R_f = 1kΩ, R_L tied to V_{CM}; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Static, DC Performance							
	Supply Current (Note 4)	R_L = ∞	3.0	3.4	3.6	3.6	mA
Miscellaneous Performance							
	Input Resistance (non-inverting)		0.39	0.28	0.25	0.25	MΩ
	Input Capacitance (non-inverting)		1.5	2.3	2.3	2.3	pF
	Input Voltage Range, High		4.2	4.1	4.0	4.0	V
	Input Voltage Range, Low		0.8	0.9	1.0	1.0	V
	Output Voltage Range, High	R_L = 100Ω	4.0	3.9	3.8	3.8	V
	Output Voltage Range, Low	R_L = 100Ω	1.0	1.1	1.2	1.2	V
	Output Voltage Range, High	R_L = ∞	4.1	4.0	4.0	3.9	V
	Output Voltage Range, Low	R_L = ∞	0.9	1.0	1.0	1.1	V
	Output Current (Note 3)		100	80	65	40	mA
	Output Resistance, Closed Loop	DC	70	105	105	140	mΩ

±5V Electrical Characteristics

A_V = +2, V_{CC} = ±5V, R_L =100Ω, R_f = 1kΩ; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max(Note 2)			Units
Ambient Temperature		CLC452AJ	+25˚C	+25˚C	0 to 70˚C	−40 to 85˚C	
Frequency Domain Response							
	-3dB Bandwidth	V_O <1.0V_{PP}	160	135	120	115	MHz
		V_O <4.0V_{PP}	75	60	57	55	MHz
	−0.1dB Bandwidth	V_O <1.0V_{PP}	30	25	25	20	MHz
	Gain Peaking	<200MHz, V_O <1.0V_{PP}	0	0.5	0.9	1.0	dB
	Gain Rolloff	<30MHz, V_O <1.0V_{PP}	0.1	0.2	0.3	0.3	dB
	Linear Phase Deviation	<30MHz, V_O <1.0V_{PP})	0.1	0.2	0.3	0.3	deg
	Differential Gain	NTSC, R_L = 150Ω	0.05	-	-	-	%
	Differential Phase	NTSC, R_L = 150Ω	0.08	-	-	-	deg
TIME DOMAIN RESPONSE							
	Rise and Fall Time	2V Step	3.2	4.2	4.5	5.0	ns
	Settling Time to ±0.05%	2V Step	20	-	-	-	ns
	Overshoot	2V Step	8	12	15	15	%
	Slew Rate	2V Step	540	400	370	350	V/µs
DISTORTION AND NOISE RESPONSE							
	2nd Harmonic Distortion	2V_{PP},1MHz	−77	−71	−69	−69	dBc
		2V_{PP},1MHz, R_L = 1kΩ	−78	−72	−70	−70	dBc
		2V_{PP},5MHz	−69	−63	−61	−61	dBc
	3rd Harmonic Distortion	2V_{PP}, 1MHz	−72	−68	−66	−66	dBc
		2V_{PP}, 1MHz, R_L = 1kΩ	−90	−80	−78	−78	dBc
		2V_{PP}, 5MHz	−58	−54	−52	−52	dBc
	Equivalent Input Noise						
	Voltage (e_{ni})	>1MHz	2.8	3.5	3.8	3.8	nV/$\sqrt{Hz}$
	Non-Inverting current (i_{bn})	>1MHz	7.5	10	11	11	pA/$\sqrt{Hz}$
	Inverting Current (i_{bi})	>1MHz	10.5	14	15	15	pA/$\sqrt{Hz}$

±5V Electrical Characteristics (Continued)

A_V = +2, V_{CC} = ±5V, R_L =100Ω, R_f = 1kΩ; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max(Note 2)			Units
Static, DC Performance							
	Input Offset Voltage		1	6	8	8	mV
	Average Drift		10	-	-	-	µV/˚C
	Input Bias Current (non-inverting)		3	18	23	25	µA
	Average Drift		40	-	-	-	nA/˚C
	Input Bias Current (inverting)		13	24	31	31	µA
	Average Drift		30	-	-	-	nA/˚C
	Power Supply Rejection Ratio	DC	48	45	43	43	dB
	Common-Mode Rejection Ratio	DC	53	50	48	48	dB
	Supply Current	R_L = ∞	3.2	3.8	4.0	4.0	mA
Miscellaneous Performance							
	Input Resistance (non-inverting)		0.52	0.35	0.30	0.30	MΩ
	Input Capacitance (non-inverting)		1.2	1.8	1.8	1.8	pF
	Common-Mode Input Range		±4.2	±4.1	±4.1	±4.0	V
	Output Voltage Range	R_L = 100Ω	±3.8	±3.6	±3.6	±3.5	V
	Output Voltage Range	R_L = ∞	±4.0	±3.8	±3.8	±3.7	V
	Output Current (Note 3)		130	100	80	50	mA
	Output Resistance, Closed Loop	DC	60	90	90	120	mΩ

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

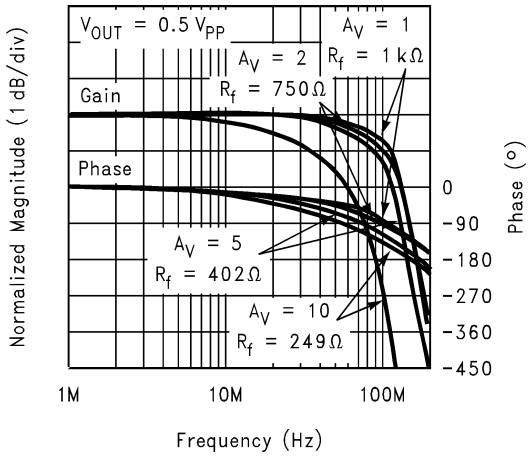
Note 3: The short circuit current can exceed the maximum safe output current.

Note 4: AJ-level: spec. is 100% tested at +25˚C.

Note 5: $V_S = V_{CC} - V_{EE}$

+5V Typical Performance Characteristics

Non-Inverting Frequency Response



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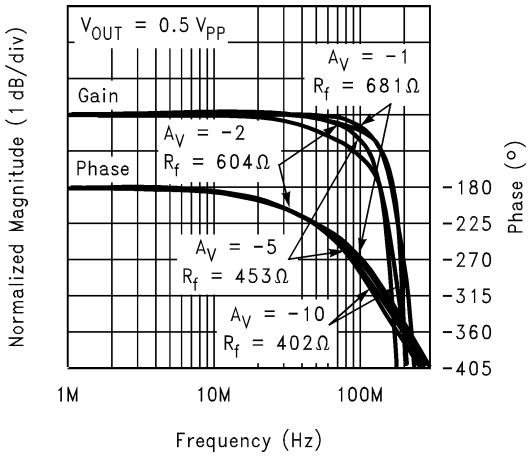
Inverting Frequency Response



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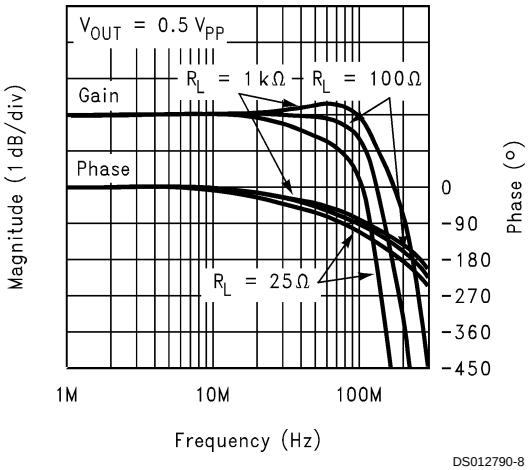
+5V Typical Performance Characteristics (Continued)

Frequency Response vs. R_L



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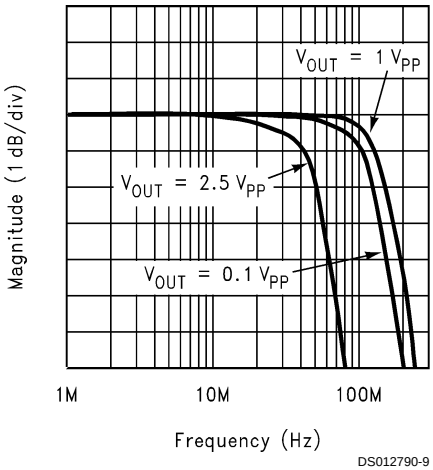
Frequency Response vs. V_O



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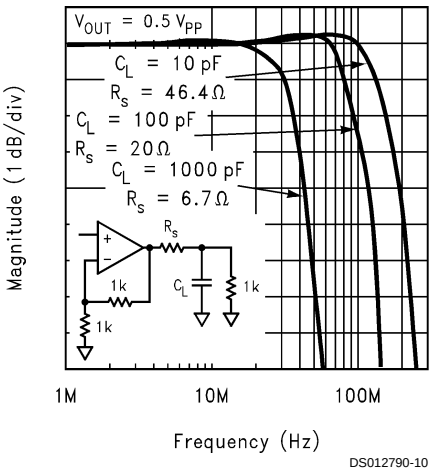
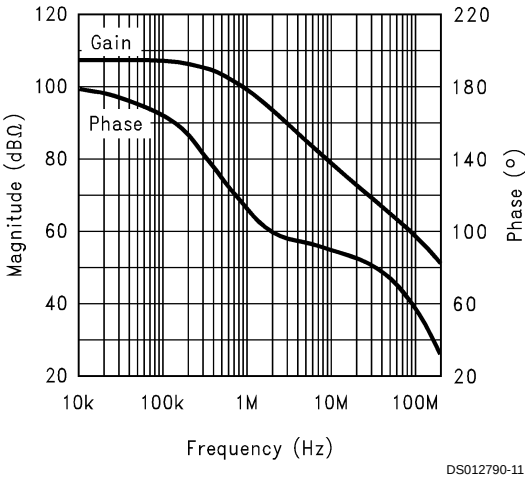
Frequency Response vs. C_L



DS012790-10

Open Loop Transimpedance Gain, Z(s)



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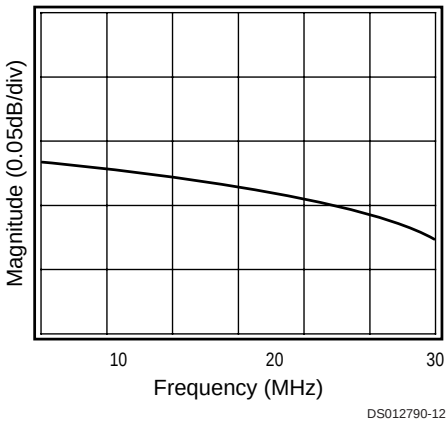
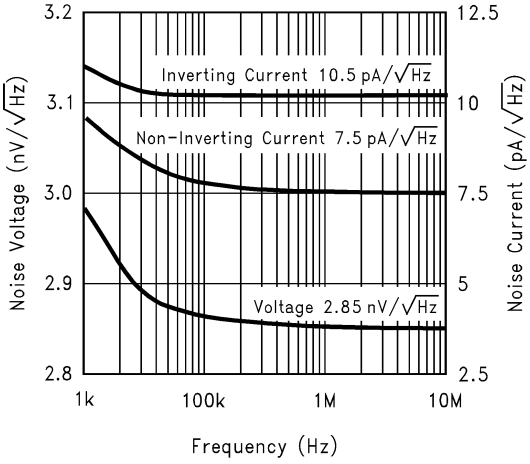
Gain Flatness



DS012790-12

Equivalent Input Noise



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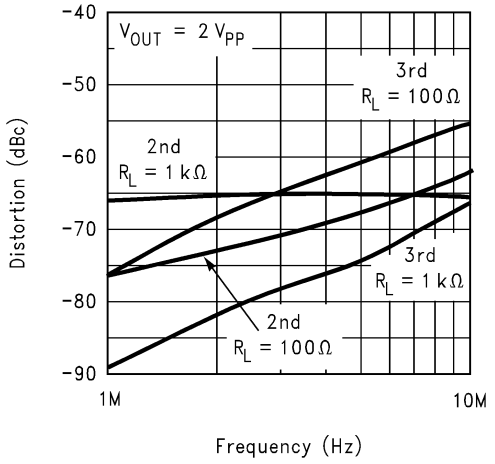
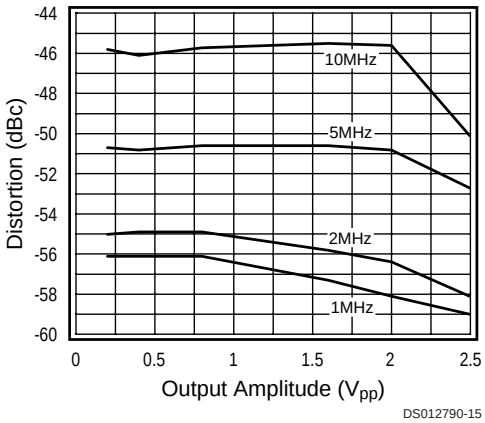
+5V Typical Performance Characteristics (Continued)

2nd & 3rd Harmonic Distortion



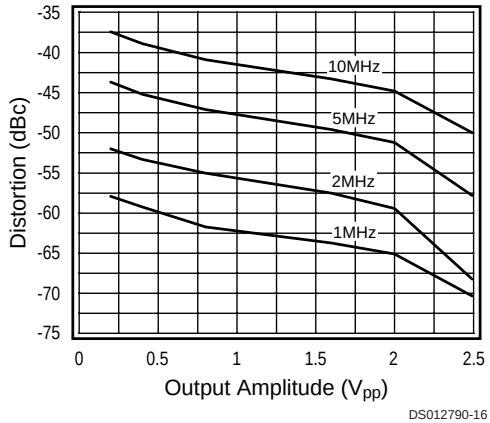
DS012790-14

2nd Harmonic Distortion, R_L = 25Ω



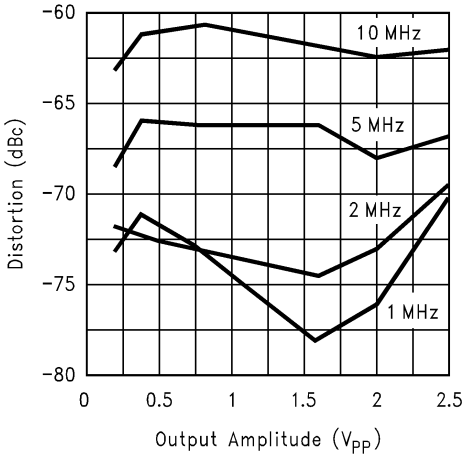
DS012790-15

3rd Harmonic Distortion, R_L = 25Ω



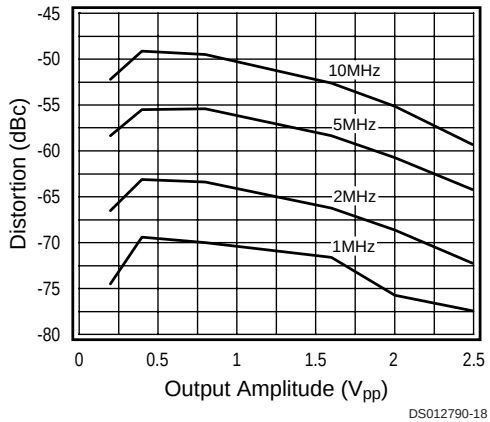
DS012790-16

2nd Harmonic Distortion, R_L = 100Ω



DS012790-17

3rd Harmonic Distortion, R_L = 100Ω



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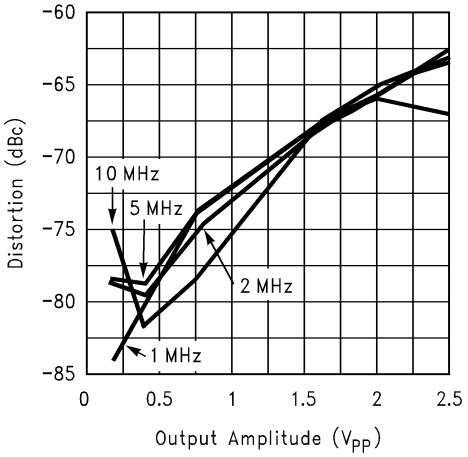
2nd Harmonic Distortion, R_L = 1kΩ



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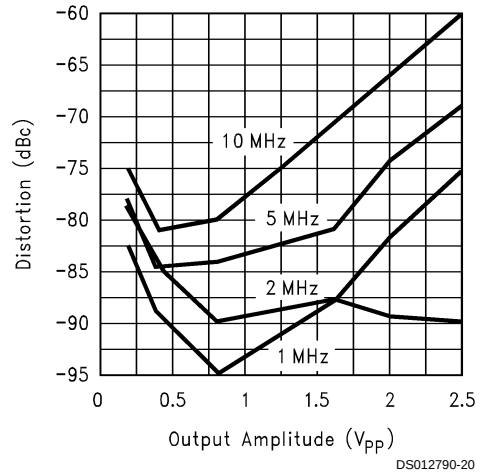
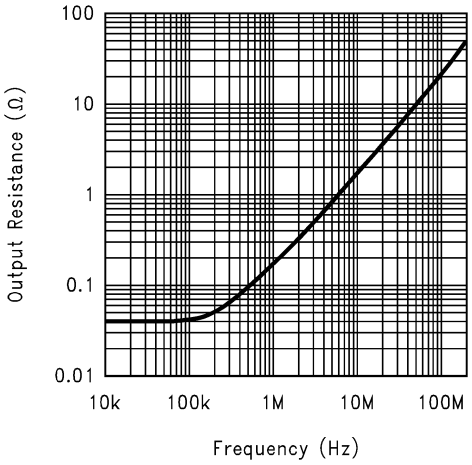
+5V Typical Performance Characteristics (Continued)

3rd Harmonic Distortion, R_L = 1kΩ



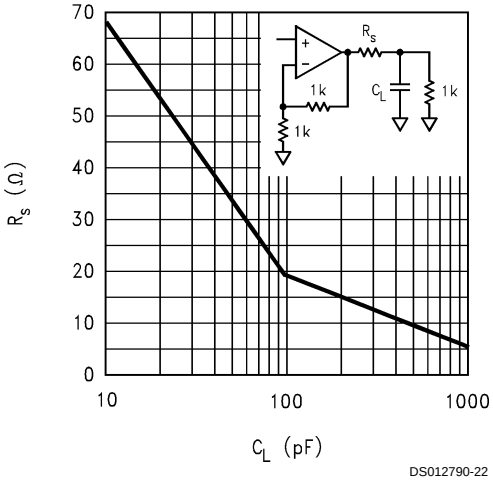
DS012790-20

Closed Loop Output Resistance



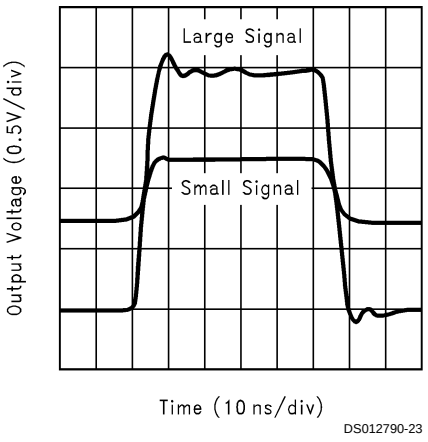
DS012790-21

Recommended R_S vs. C_L



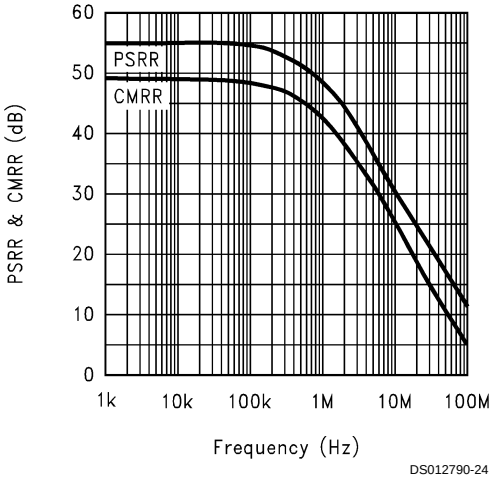
DS012790-22

Large & Small Signal Pulse Response



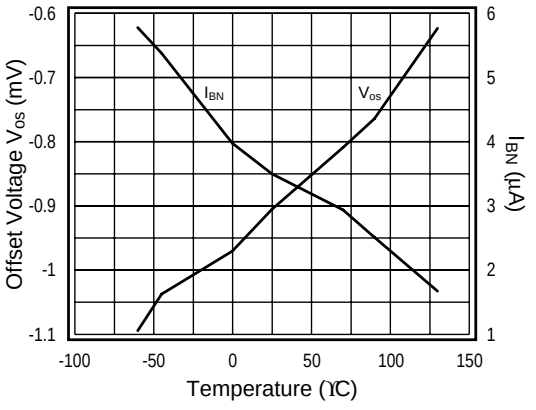
DS012790-23

PSRR & CMRR



DS012790-24

I_{BN}, V_{OS} vs. Temperature



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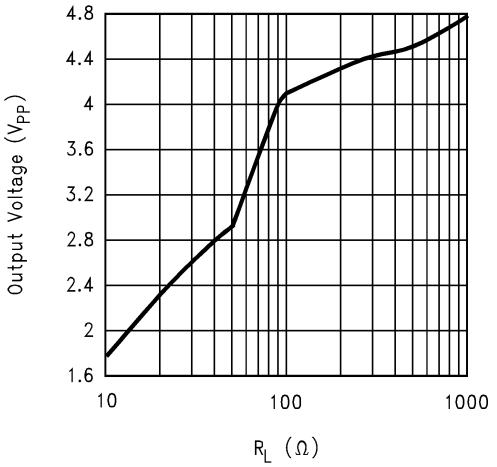
+5V Typical Performance Characteristics (Continued)

Maximum Output Voltage vs. R_L



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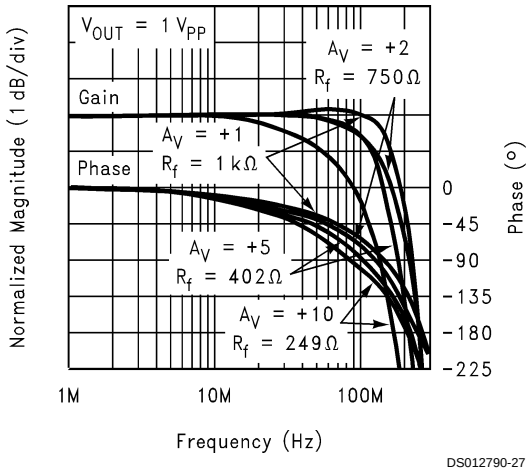
±5V Typical Performance Characteristics

Non-Inverting Frequency Response



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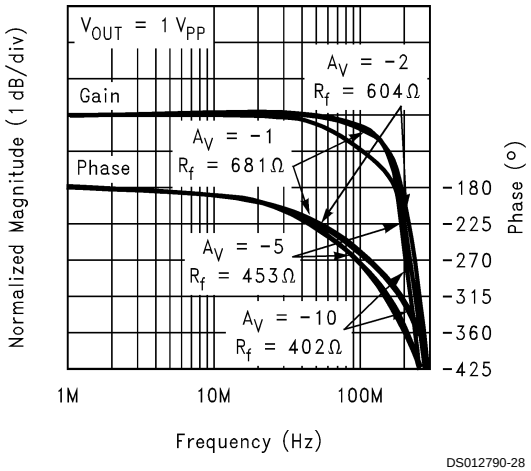
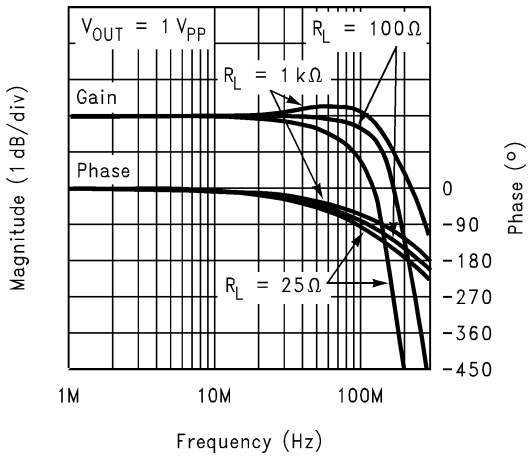
Inverting Frequency Response



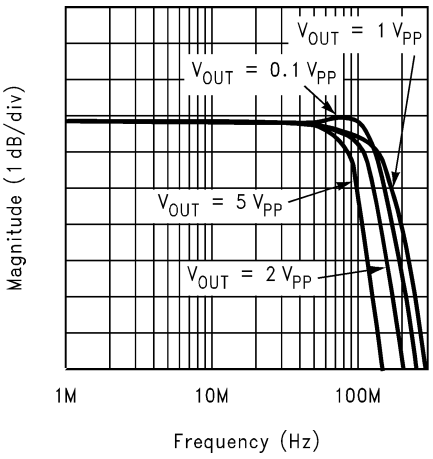
DS012790-28

Frequency Response vs. R_L



DS012790-29

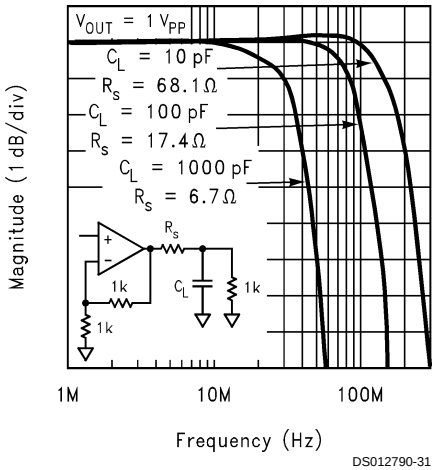
Frequency Response vs. V_O



DS012790-30

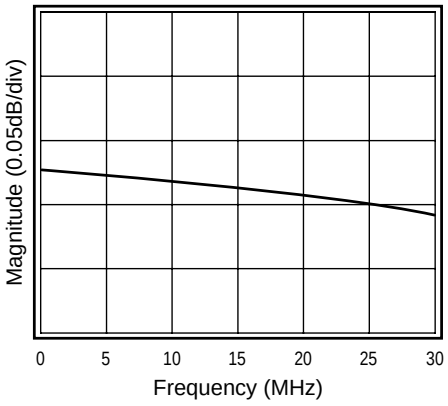
±5V Typical Performance Characteristics (Continued)

Frequency Response vs. C_L



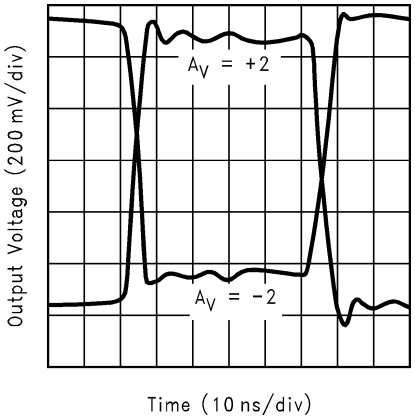
DS012790-31

Gain Flatness



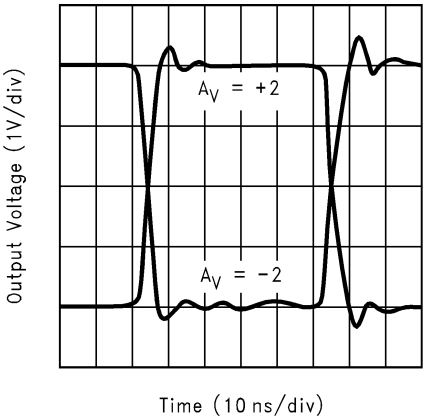
DS012790-32

Small Signal Pulse Response



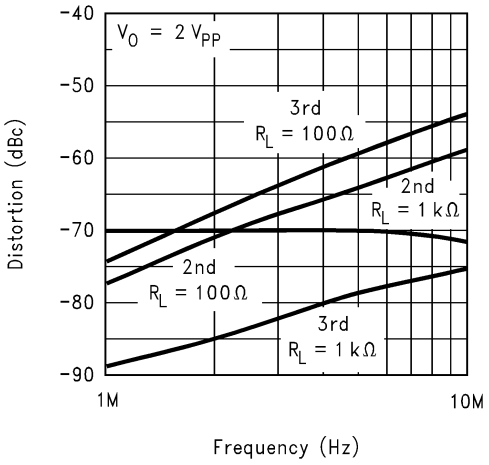
DS012790-33

Large Signal Pulse Response



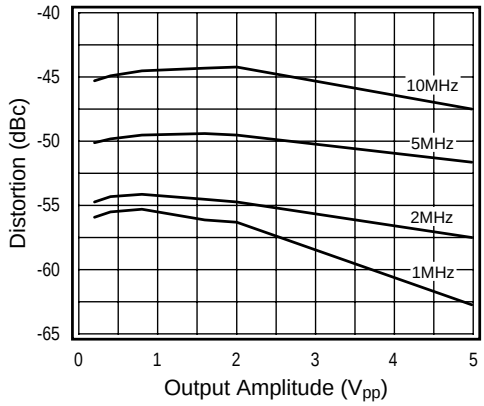
DS012790-34

2nd & 3rd Harmonic Distortion



DS012790-35

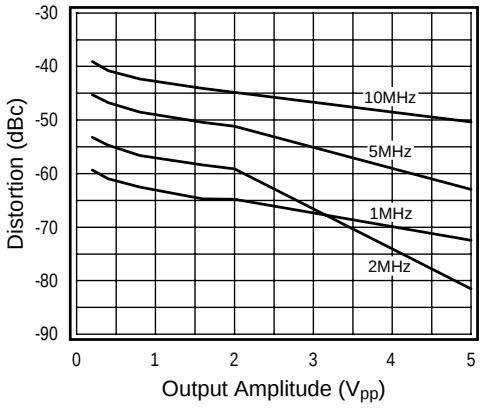
2nd Harmonic Distortion, R_L = 25Ω



DS012790-36

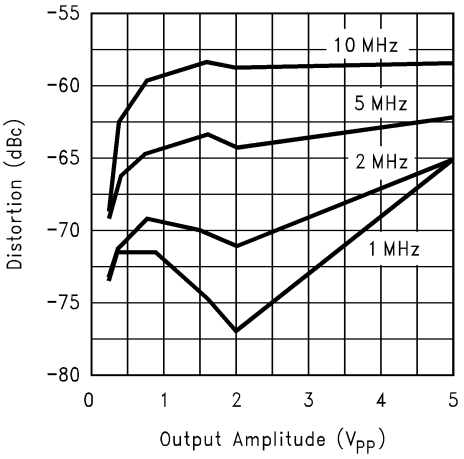
±5V Typical Performance Characteristics (Continued)

3rd Harmonic Distortion, R_L = 25Ω



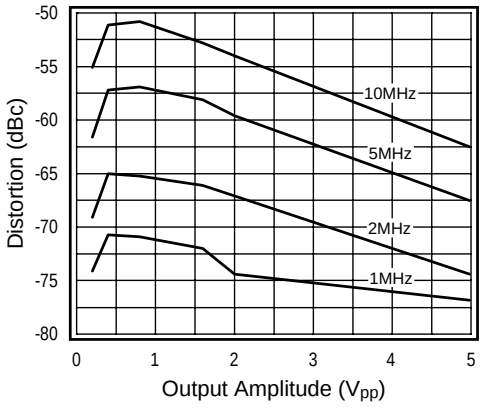
DS012790-37

2nd Harmonic Distortion, R_L = 100Ω



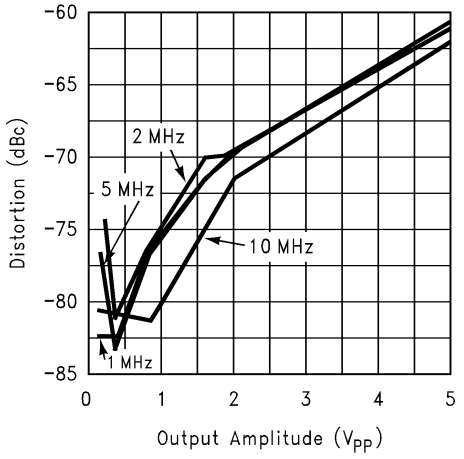
DS012790-38

3rd Harmonic Distortion, R_L = 100Ω



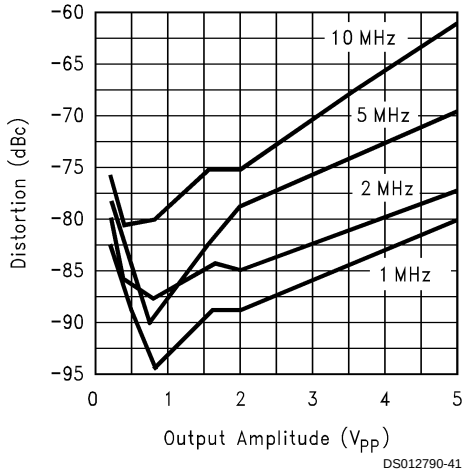
DS012790-39

2nd Harmonic Distortion, R_L = 1kΩ



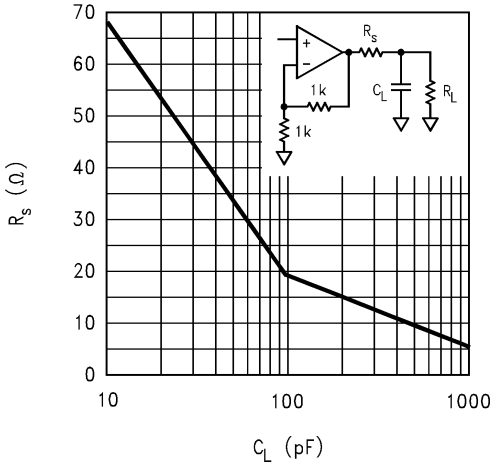
DS012790-40

3rd Harmonic Distortion, R_L = 1kΩ



DS012790-41

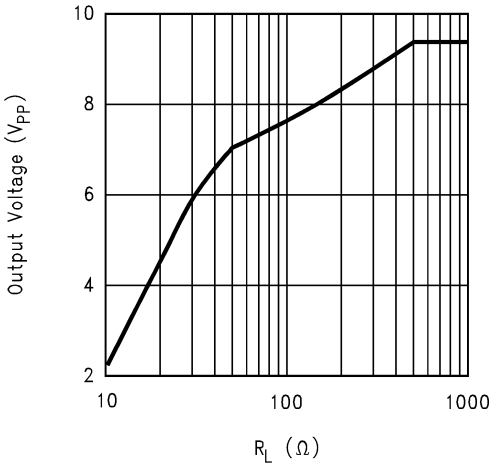
Recommended R_S vs. C_L



DS012790-42

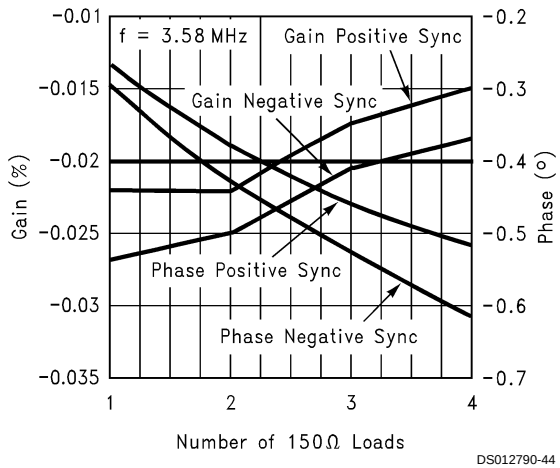
±5V Typical Performance Characteristics (Continued)

Maximum Output Voltage vs. R_L



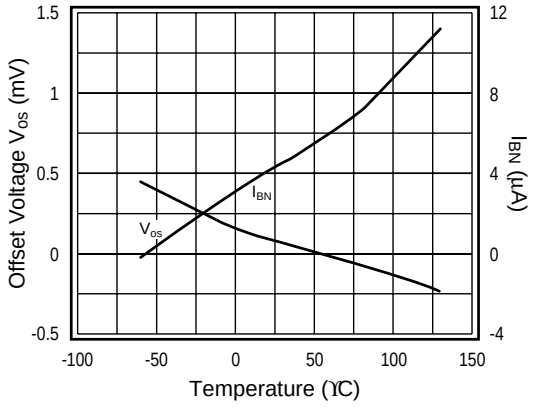
DS012790-43

Differential Gain & Phase



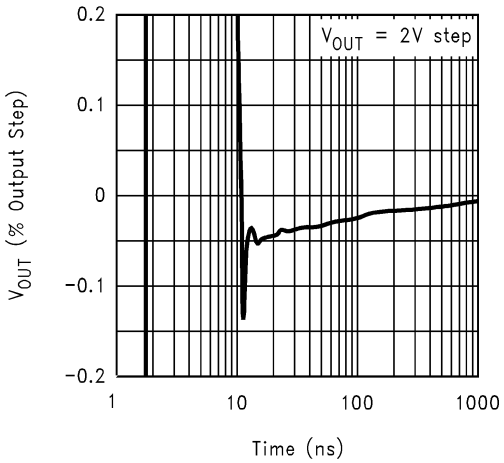
DS012790-44

I_{BN}, V_{OS} vs. Temperature



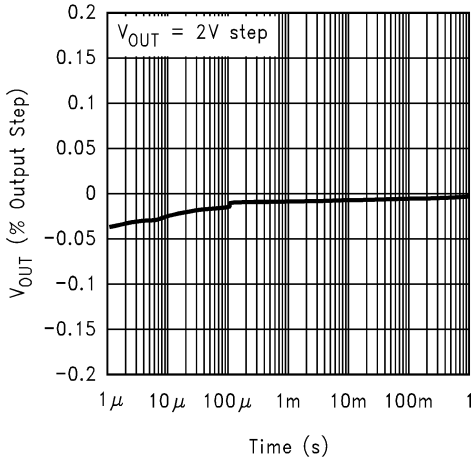
DS012790-45

Short Term Settling Time



DS012790-46

Long Term Settling Time



DS012790-47

Application Division

CLC452 Operation

The CLC452 is a current feedback amplifier built in an advanced complementary bipolar process. The CLC452 operates from a single 5V supply or dual ±5V supplies. Operating from a single supply, the CLC452 has the following features:

- Provides 100mA of output current while consuming 15mW of power
- Offers low −78/−85dB 2nd and 3rd harmonic distortion
- Provides BW >80MHz and 1MHz distortion < −70dBc at V_O=2.0V_{PP}

The CLC452 performance is further enhanced in ±5V supply application as indicated in the **±5V Electrical Characteristics** table and **±5V Typical Performance** plots.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Interdependence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}}$$

where:

- A_V is the closed loop DC voltage gain
- R_f is the feedback resistor
- Z(jω) is the CLC450's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the −3dB corner frequency, the interaction between R_f and Z(jω) dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases loop bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Refer to the **Feedback Resistor Selection** section for more details on selecting a feedback resistor value.

Design Information

Single Supply Operation (V_{CC}=+5V, V_{EE} = GND)

The specifications given in the **+5V Electrical Characteristics** table for single supply operation are measured with a common mode voltage (V_{CM}) of 2.5V. V_{CM} is the voltage around which the inputs are applied and the output voltage are specified.

Operating a single +5V supply, The Common Mode Input Range (CMIR) of the CLC452 is typically +0.8V to +4.2V. The typical output range with R_L =100Ω is +1.0V to +4.0V.

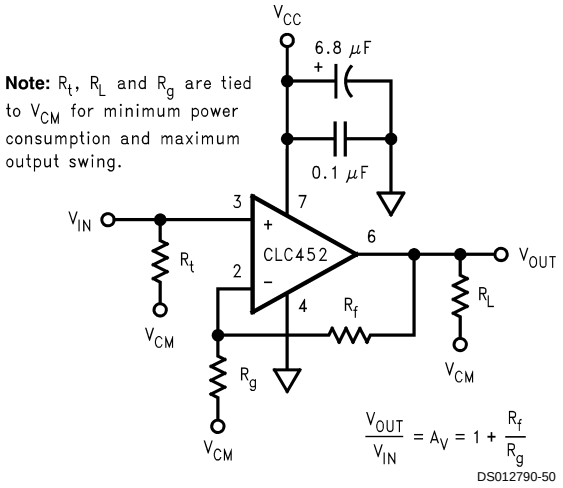


FIGURE 1. Non-Inverting Configuration

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation

Figure 1 and *Figure 2* show the recommended non-inverting and inverting configurations for input signals that remain above 0.8V DC.

Application Division (Continued)

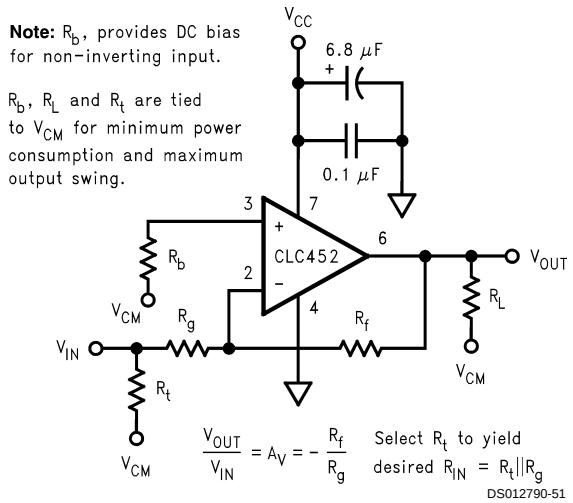


FIGURE 2. Inverting Configuration

AC Coupled Single Supply Operation

Figure 3 and *Figure 4* show possible non-inverting and inverting configurations for input signals that go below 0.8V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$ (For $V_{CC} = +5V$).

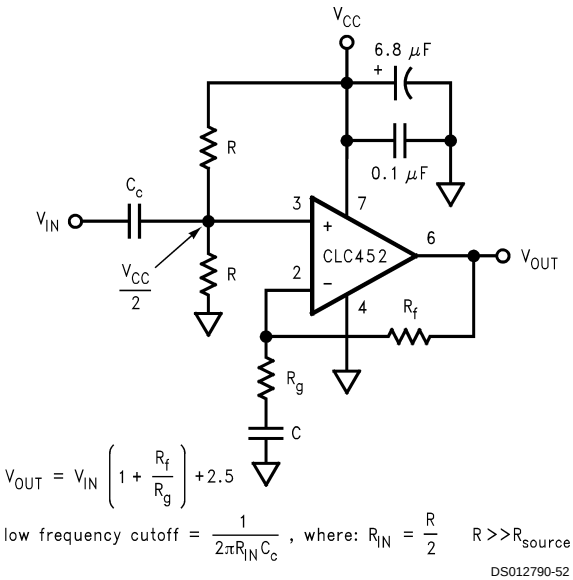


FIGURE 3. AC Coupled Non-Inverting Configuration

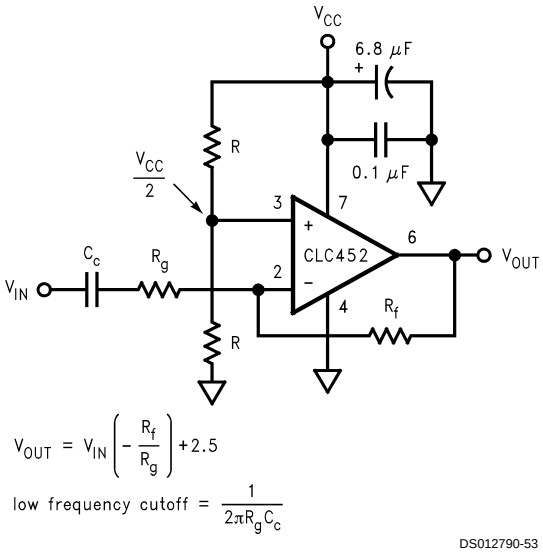


FIGURE 4. AC Coupled Inverting Configuration

Dual Supply Operation

The CLC452 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in *Figure 5* and *Figure 6*.

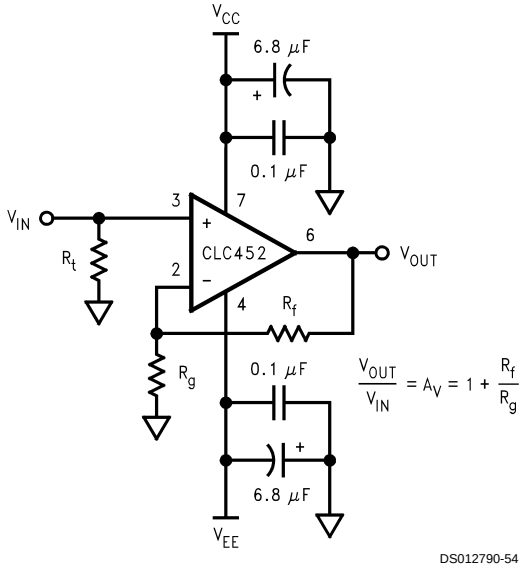


FIGURE 5. Dual Supply Non-Inverting Configuration

Application Division (Continued)

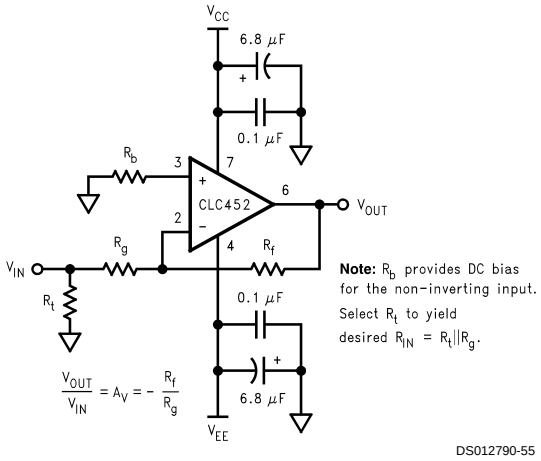


FIGURE 6. Dual Supply Inverting Configuration

Feedback Resistor Selection

The feedback resistor, R_f, affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC452, at a gain of +2V/V, is achieved with R_f equal to 1kΩ. The frequency response plots in the **Typical Performance** sections illustrate the recommended R_f provide the maximum bandwidth with minimal peaking. Within limits, R_f can be adjusted to optimize the frequency response.

- Decrease R_f to peak frequency response and extend bandwidth
- Increases R_f to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended R_f is doubled, then the bandwidth will be cut in half.

Unity Gain Operation

The recommended R_f for unity gain (+1V/V) operation is 1kΩ. R_g is left open. Parasitic capacitance at the inverting node may require a slight increase in R_f to maintain a flat frequency response.

Bandwidth vs. Output Amplitude

The bandwidth of the CLC452 is at a maximum for output voltages near 1Vpp. The bandwidth decreases for smaller and larger output amplitudes. Refer to the **Frequency Response vs. V_o** plots.

Load Termination

The CLC452 can source and sink near equal amounts of current. For optimum performance, the load should be tied to V_{cm}.

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load application, a small series resistor at the output of the CLC452 will improve stability and settling performance. The **Frequency Response vs. C_L** and **Recommended $R_s$vs. C_L** plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

Transmission Line Matching

One method for matching the characteristic impedance (Z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. *Figure 7* shows typical inverting and non-inverting circuit configurations for matching transmission lines.

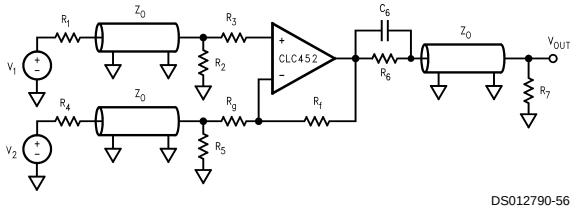


FIGURE 7. Transmission Line Matching

Non-inverting gain application:

- Connect R_g directly to ground.
- Make R_1,R_2, R_6, R_7 equal to Z_o.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain application:

- Connect R_3 directly to ground.
- Make the resistors R_4, R_6, and R_7 equal to Z_o
- Make $R_5 || R_g = Z_o$

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Power Dissipation

Follow these steps to determine the power consumption of the CLC452:

1. Calculate the quiescent (no-load) power:
   $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage:
   $P_o = (V_{CC} - V_{load})(I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power: $P_t = P_{amp} + P_o$

The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in *Figure 8*. The power derating cure for any CLC452 package can be derived by utilizing the following equation:

$$\frac{(150° - T_{amb})}{\theta_{JA}}$$

Where

- T_{amb} = Ambient temperature (°C)

Application Division (Continued)

- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (˚C/W)

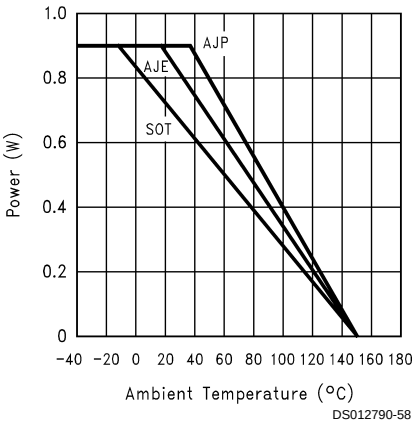


FIGURE 8. Power Derating Curves

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC452 (730013-DIP, 730027-SOIC, 730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow The steps below as a bias for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.
-

Evaluation Board Information

Data sheet are available for the CLC730013/CLC730027 and CLC730068 evaluation boards. The velitation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of National's high speed amplifiers. This table for the CLC452 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

Components Needed to Evaluate the CLC452 on the Evaluation Board:

- R_f, R_g — Use this product data sheet to select values.
- R_{in}, R_{out} - Typically 50Ω (Refer to the **Basic Operation** section of the evaluation board data sheet for details)
- R_f — Optional resistor for inverting gain configurations (Select R_f to yield desired input impedance = $R_g \| R_f$
- C_1, C_2-0.1µF ceramic capacitors
- C_3, C_4-6.8µF tantalum capacitors

Components not used:

- C_5, C_6, C_7, C_8
- R_1 thru R_8

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE modes are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The **readme** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

Application Circuits

Single Supply Cable Driver

The typical application shown on the front page shows the CLC452 driving 10m of 75Ω coaxial cable. The CLC452 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o.

Single Supply Lowpass Filter

Figure 9 and *Figure 10* illustrate a lowpass filter and design equation. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine R_1, R_2, C_1 and C_2 based on the desired Q and corner frequency.

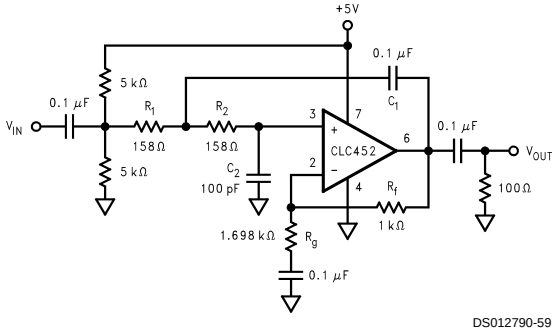


FIGURE 9. Lowpass Filter Topology

Application Division (Continued)

$$\text{Gain} = K = 1 + \frac{R_f}{R_g}$$

$$\text{Corner frequency} = \omega_c = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + (1 - K)\sqrt{\frac{R_1 C_1}{R_2 C_2}}}$$

$$\text{For } R_1 = R_2 = R \text{ and } C_1 = C_2 = C$$

$$\omega_c = \frac{1}{RC}$$

$$Q = \frac{1}{(3 - K)}$$

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FIGURE 10. Design Equations

This example illustrates a lowpass filter with Q = 0.707 and corner frequency f_c = 10MHz. AQ of 0.707 was chosen to achieve a maximally flat, Butterworth response. *Figure 11* indicates the filter response.

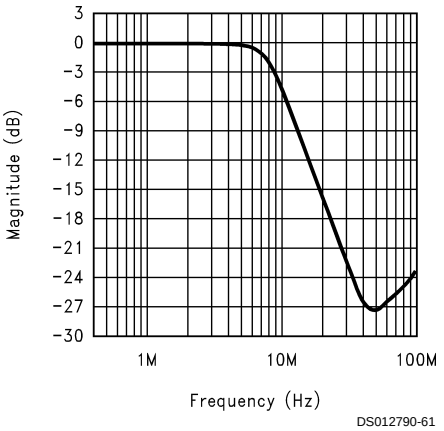


FIGURE 11. Lowpass Response

Twisted Pair Driver

The high output current and low distortion, of the CLC452, make it well suited for driving transformers. *Figure 12* illustrates a typical twisted pair driver utilizing the CLC452 and a transformer. The transformer provides the signal and its inversion for the twisted pair.

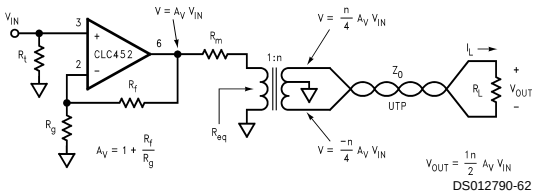


FIGURE 12. Twisted Pair Driver

To match the line's characteristic impedance (Z_o) set:

- $R_L = Z_O$
- $R_m = R_{eq}$

Where R_{eq} is the transformed value of the load impedance, (R_L), and is approximated by:

$$R_{eq} = R_L/n^2$$

Select the transformer so that it loads the line with a value close to Z_o, over the desired frequency range. The output impedance, R_o, of the CLC452 varies within frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of R_o

$$\text{Return Loss (dB)} = -20\log_{10}\left|n^2 \cdot \frac{R_0}{Z_0}\right|$$

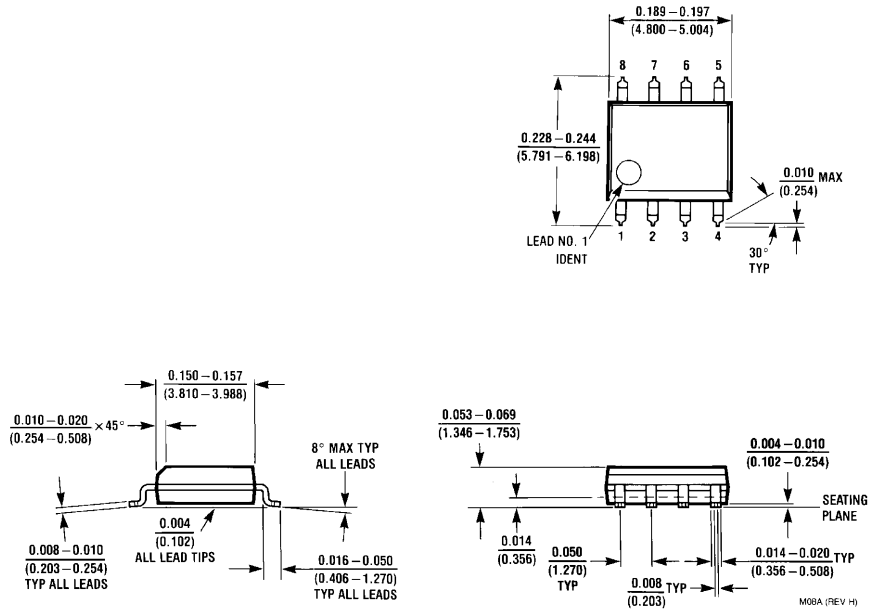
The load current (I_i) and voltage (V_O) are related to the CLC452's maximum output voltage and current by:

$$\left|V_0\right| \leq n \bullet V_{max}$$

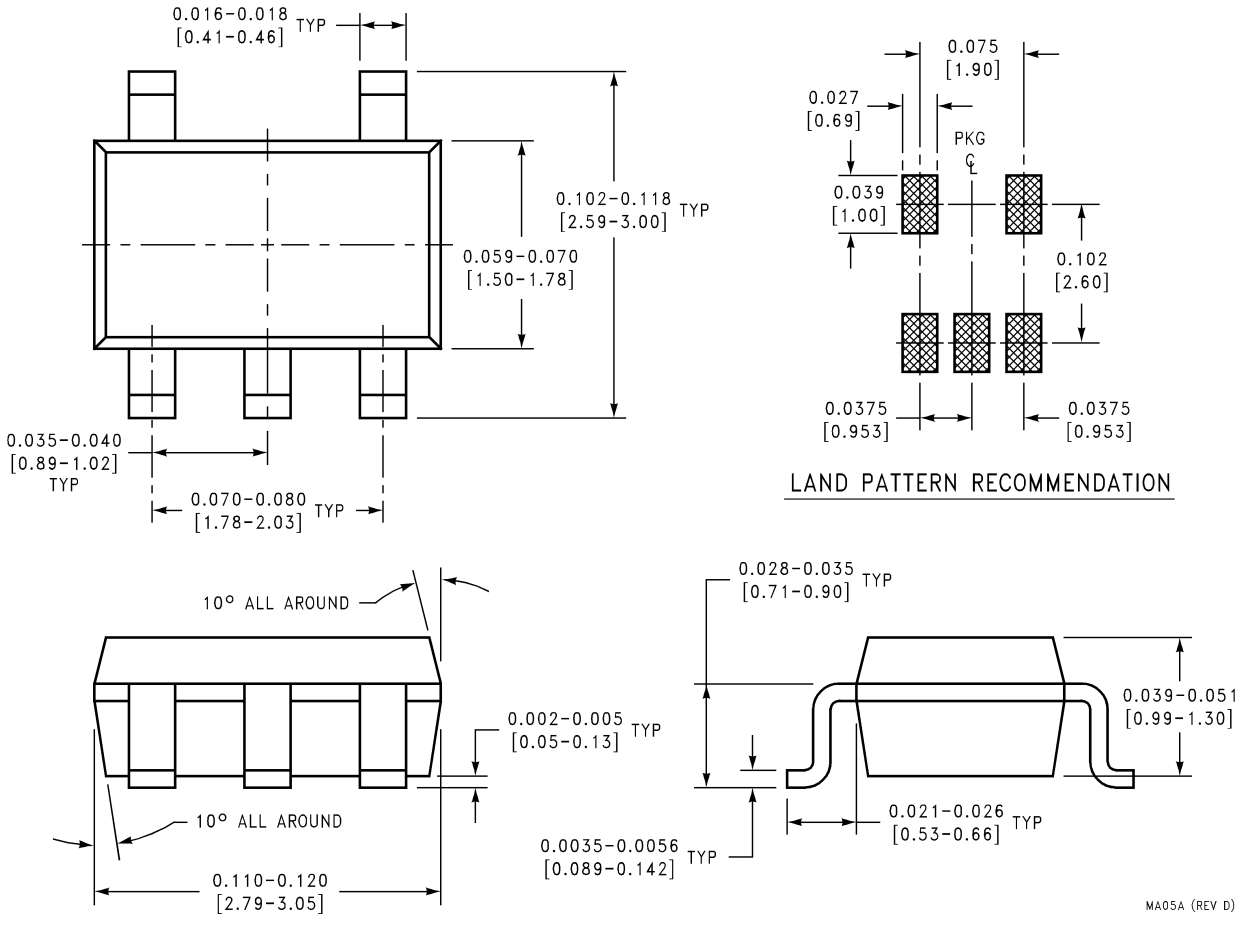
$$\left|I_L\right| \leq \frac{I_{max}}{n}$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

Physical Dimensions inches (millimeters) unless otherwise noted

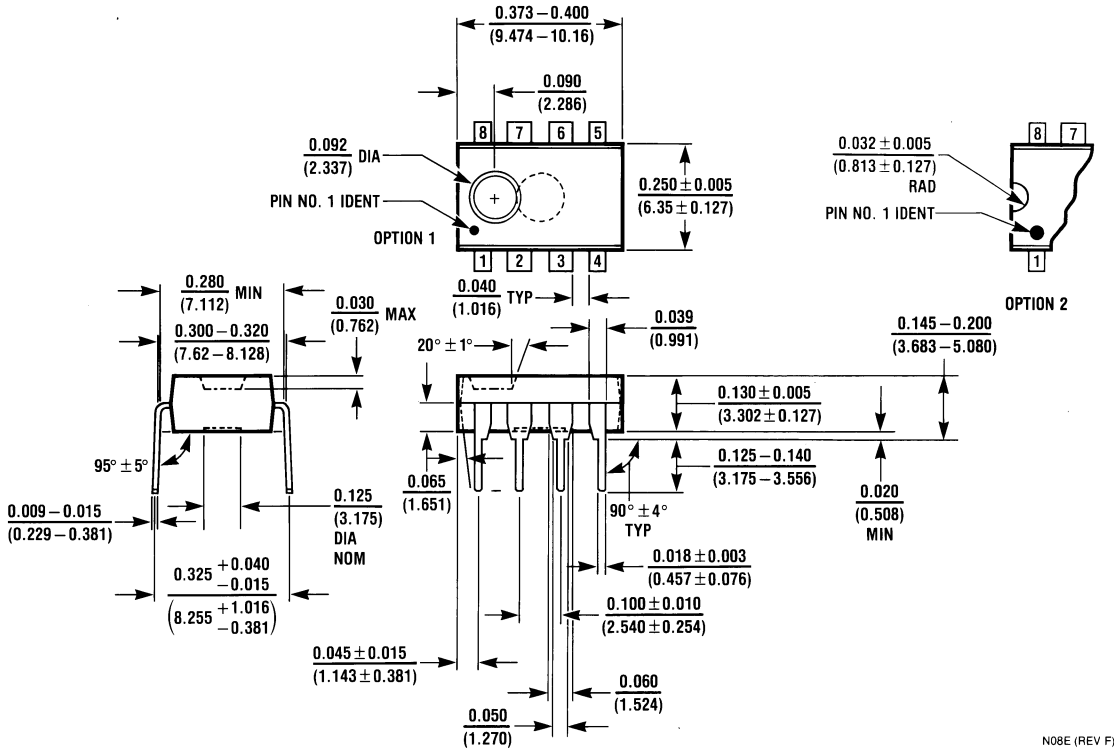


8-Pin SOIC
NS Package Number M08A



5-Pin SOT23
NS Package Number MA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Pin MDIP
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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