Rochester Electronics®

Datasheet

11373

Octal D-Type Transparent Latches with 3-State Outputs

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

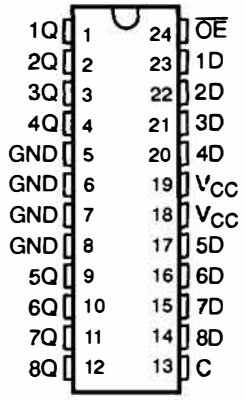
FOR REFERENCE ONLY

54AC11373, 74AC11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

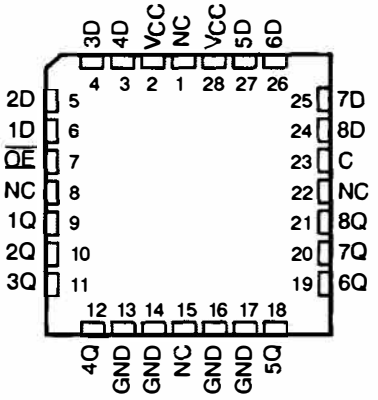
SCAS213 – D2957, MAY 1987 – REVISED APRIL 1993

- **Eight Latches In a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11373 . . . JT PACKAGE
74AC11373 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54AC11373 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'AC11373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output enable $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

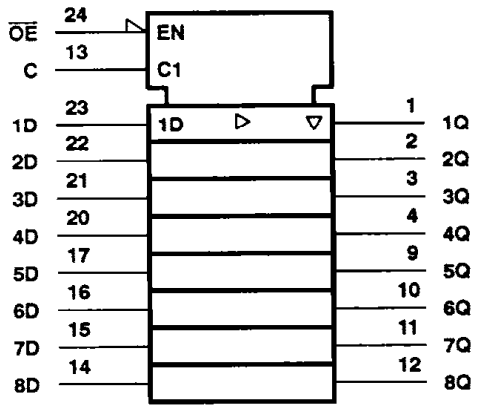
The 54AC11373 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11373 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

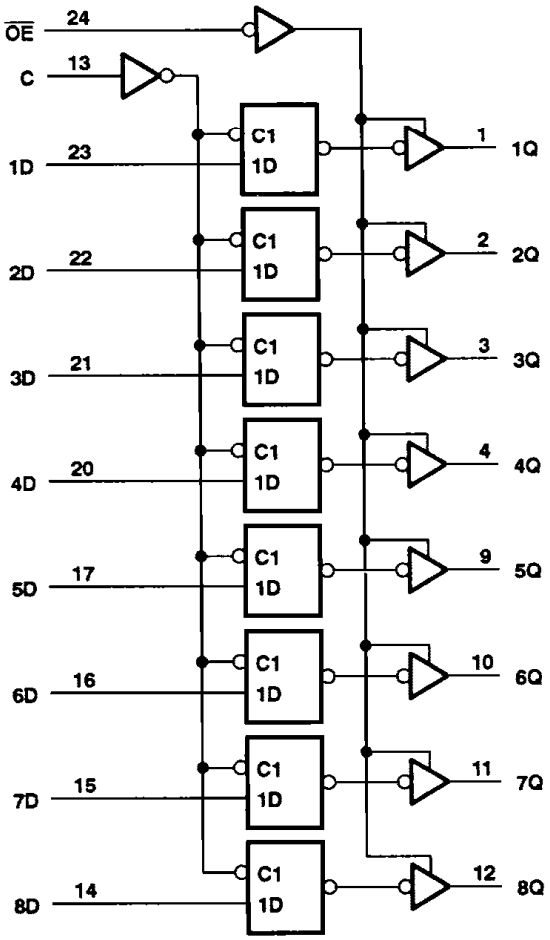
INPUTS			OUTPUT
$\overline{OE}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11373			74AC11373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OC}$	0		5	0		5	ns/V
		Data, C	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54AC11373		74AC11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	5.5		5.5		5.5		ns
t_{su}	Setup time, data before enable C↓	4		4		4		ns
t_h	Hold time, data after enable C↓	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54AC11373		74AC11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	4		4		4		ns
t_{su}	Setup time, data before enable C↓	3.5		3.5		3.5		ns
t_h	Hold time, data after enable C↓	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	9	13.1	1.5	15.7	1.5	14.8	ns
t_{PHL}			1.5	8	10.6	1.5	12.4	1.5	11.7	
t_{PLH}	C	Any Q	1.5	10	14.5	1.5	17.4	1.5	16.3	ns
t_{PHL}			1.5	9.5	12.8	1.5	15.2	1.5	14.2	
t_{PZH}	$\overline{OE}$	Any Q	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
t_{PZL}			1.5	8.5	11.6	1.5	14.1	1.5	13.1	
t_{PHZ}	$\overline{OE}$	Any Q	1.5	9.5	12	1.5	13.1	1.5	12.7	ns
t_{PLZ}			1.5	7.5	10.2	1.5	11.3	1.5	10.8	

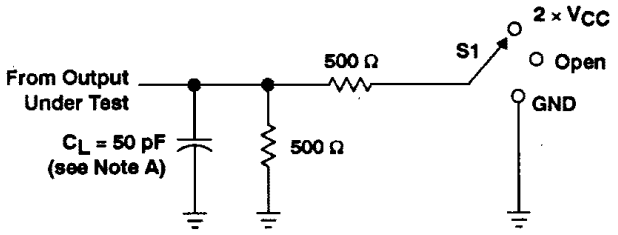
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	6	8.9	1.5	11.7	1.5	10.3	ns
t_{PHL}			1.5	5.5	7.6	1.5	9.1	1.5	8.4	
t_{PLH}	C	Any Q	1.5	6.5	10	1.5	12.1	1.5	11.3	ns
t_{PHL}			1.5	6.5	9.1	1.5	11	1.5	10.2	
t_{PZH}	$\overline{OE}$	Any Q	1.5	6.5	9.5	1.5	11.6	1.5	10.8	ns
t_{PZL}			1.5	6	8.6	1.5	10.9	1.5	9.7	
t_{PHZ}	$\overline{OE}$	Any Q	1.5	8.5	10.6	1.5	11.5	1.5	11.1	ns
t_{PLZ}			1.5	6	8.2	1.5	9.1	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

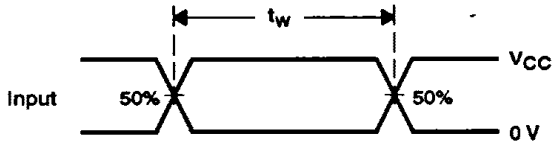
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		36	

PARAMETER MEASUREMENT INFORMATION

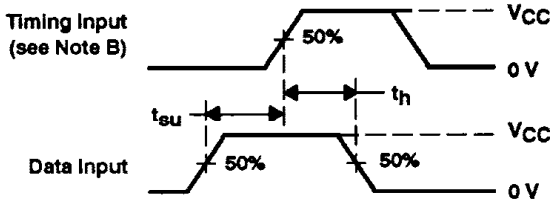


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



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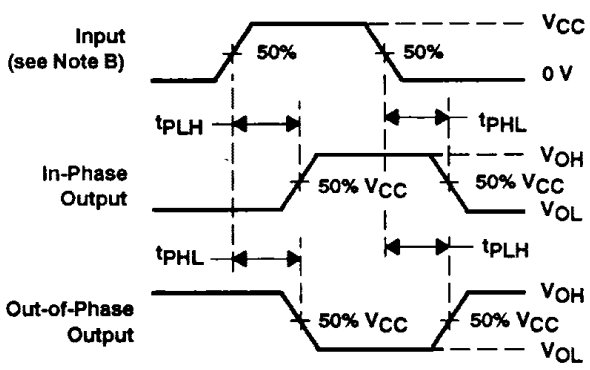
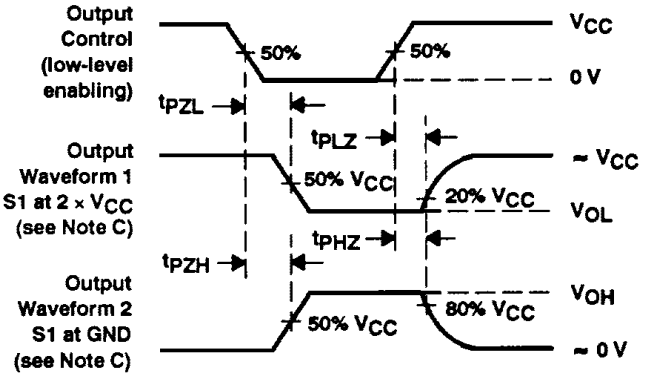


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms