features

- **Integrated, Single-Chip Solution for Battery Charge Control and Power Supply Management**
- **Linear Charger for Single-Cell Li-Ion or Li-Polymer Packs**
- **Integrated Control over Precharge, Constant-Current, and Constant-Voltage Charging Phases**
- **Programmable Charge Termination by Minimum Current and Time**
- **Battery Temperature Sensing**
- **Pack Wake-Up and Damaged Cell Detect Functions**
- **Safety Charge Timers During Precharge and Constant-Current Charging**
- **Programmable Charging Current**
- **Six Programmable Low-Dropout Linear Voltage Regulators**
- **Over 65-dB Power Supply Rejection Ratio (PSRR) From 10 Hz to 10 kHz**
- **System Over- and Under-Voltage Shutdown**
- **Power On/Off and Reset Control Logic**
- **Three Individually Selectable LED Backlight Drivers**
- **Vibrator and Ringer Drivers**
- **Internal 8-Bit Analog-to-Digital Converter With Auxiliary Inputs**
- **I^2C Control Interface and Three-Wire SPI Interface**
- **48-Terminal Plastic TQFP (PFB) or MicroStar Junior BGA™ (GQE) Package**

description

The TWL2214CA device is a single-chip battery and power management solution for wireless handsets, pagers, personal digital assistants (PDAs), and other battery-powered devices. For battery charging, the device incorporates a linear charger for single-cell Li-Ion and lithium polymer battery packs. Prior to charging, the TWL2214CA device initiates battery pack wake-up and damaged cell detect functions. For deeply discharged batteries, the device performs precharge conditioning by trickle charge to a user-defined current setting. Once an acceptable pack voltage is detected, the TWL2214CA device applies a constant-current fast charge at a current level that is determined by the combination of an external sense resistor and user-programmable sense voltage. When the battery reaches the selected charge regulation voltage, the TWL2214CA device maintains regulation until charging is terminated by a minimum current or a timer. During the entire charge cycle, the TWL2214CA device monitors temperature by external thermistor and suspends charging if temperature exceeds a programmed range. Three programmable safety timers limit the precharge, constant current, and total charge times.

For power management, the TWL2214CA device includes six low-dropout linear voltage regulators. One regulator is driven from the device power-on/-off logic and incorporates a microcontroller reset function. Five low-noise regulators include individually programmable output voltage and enable-disable. The TWL2214CA device can be powered from a battery or from an ac adapter. When an adapter is present, it supplies power to the device, allowing the system to function without a battery.

The TWL2214CA device also includes individually selectable drivers for three separate backlight LEDs, a ringer, and a vibrator motor. An internal 8-bit analog-to-digital converter (ADC) is accessible from external terminals. All TWL2214CA programming and status are accessed by the system microcontroller via the I^2C/SPI serial interface.

The TWL2214CA device is packaged in the Texas Instruments 48-terminal plastic thin quad flatpack (TQFP) (PFB) or the MicroStar Junior BGA™ (GQE) package.

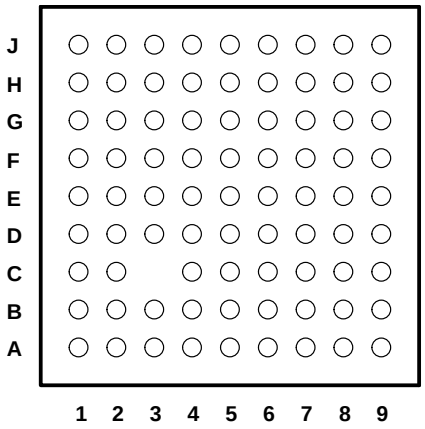
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

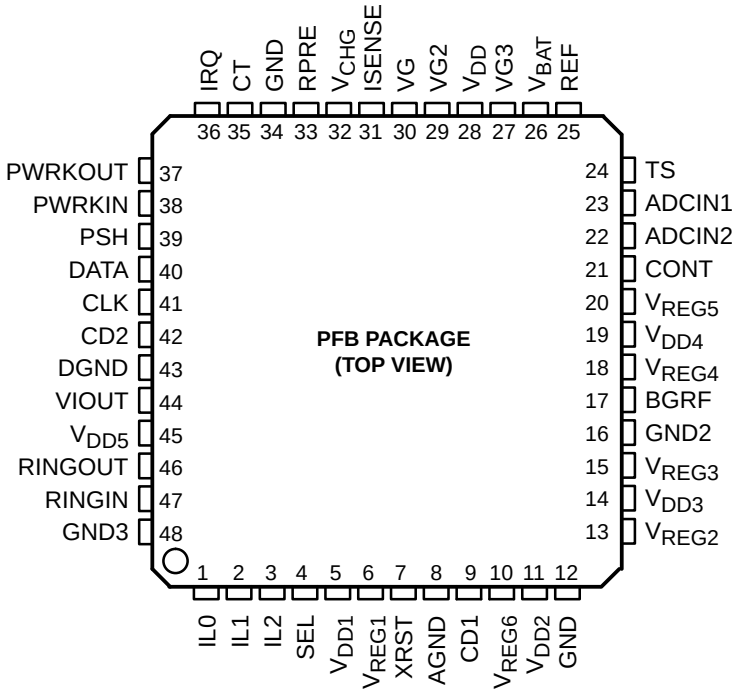
MicroStar Junior BGA is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	DEVICE NAME	PACKAGE	OUTPUT VOLTAGE		INTERFACE
			REGULATOR 1	REGULATOR 6	
–40°C to 85°C	TWL2214CAPFBR	TQFP	2.8 V	3 V	I^2C
–40°C to 85°C	TWL2214CAGQER	MicroStar Junior BGA™	2.8 V	3 V	I^2C/SPI

GQE PACKAGE
(BOTTOM VIEW)

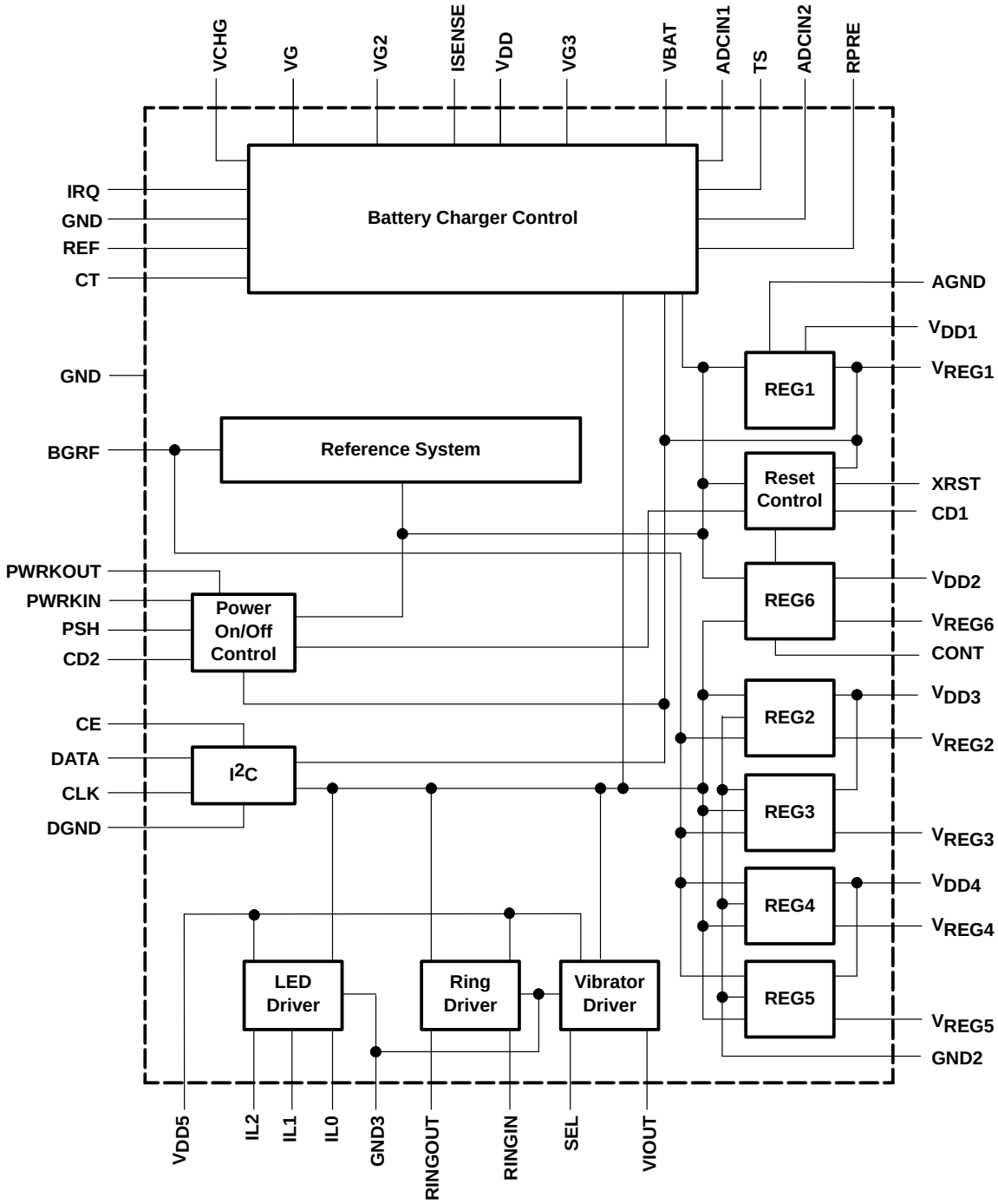




DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	OPERATING FACTOR ABOVE 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
GQE	1176 mW	11.8 mW/°C	647 mW	471 mW
PFB	1962 mW	15.7 mW/°C	1256 mW	1020 mW

block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	GQE NO.	PFB NO.		
ADCIN1	J8	23	I	ADC input
ADCIN2	J7	22	I	ADC input
AGND	C4, D3, D4, E3, E4	8	I/O	Regulator 1 ground
BGRF	J4	17	I/O	Band gap output bypass capacitance
CD1	F1	9	I/O	XRST output delay adjustment capacitance
CD2	A5	42	I/O	Regulator 1 off delay adjustment capacitance
CE	A8		I	Clock enabled
CLK	B5	41	I	I^2C/SPI bus serial clock input
CONT	H6	21	I	Regulator 6 is always on after power up except when CONT = H; regulator 6 is enabled through I^2C interface.
CT	B9	35	I/O	External oscillator timing cap
DATA	A6	40	I/O	I^2C/SPI bus serial address/data input output; this is a bidirectional terminal.
DGND	A4	43	I/O	Digital ground
GND	C8, G2	12, 34	I/O	Ground
GND2	H4	16	I/O	Ground for V_{REG2}, V_{REG3}, V_{REG4}, and V_{REG5}
GND3	B2	48	I/O	Ground for vibrator, LED, and ringer
IL0	B1	1	O	160-mA LED driver output
IL1	C2	2	O	20-mA LED driver output
IL2	C1	3	O	10-mA LED driver output
IRQ	B8	36	O	Interrupt signal for external controller regarding to charger start/stop action
ISENSE	E9	31	I	Current sense input for charger function
PSH	B6	39	I	Power hold signal from controller
PWRKIN	A7	38	I	Power-up start
PWRKOUT	B7	37	O	Power-up signal for CPU
REF	H9	25	O	Voltage reference during charge cycle, 3 V, I_O = 3 mA
RINGIN	A2	47	I/O	Input for ring driver
RINGOUT	B3	46	O	Ring driver output
RPRE	C9	33	I/O	Precharge current sense resistor
SEL	D2	4	I	Input for vibrator output voltage change
TS	H8	24	I	Battery temperature sense input voltage
V_{BAT}	G8	26	I/O	Battery voltage sense input or output for precharge, wakeup
V_{CHG}	D9	32	I	DC voltage input for charger
V_{DD}	F8	28	I	Device dc supply feedback for charger function
V_{DD1}	D1	5	I	Device dc supply input and regulator 1 input
V_{DD2}	G1	11	I	Input to regulator 6
V_{DD3}	J2	14	I	Input for regulators 2 and 3
V_{DD4}	J5	19	I	Input for regulators 4 and 5
V_{DD5}	A3	45	I	Input for vibrator, PN diode connection of ringer
VG	E8	30	O	Gate control of an external P-FET for charger regulation
VG2	F9	29	O	Gate control of an external P-FET for battery blockage

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	GQE NO.	PFB NO.		
VG3	G9	27	O	Gate control of an external P-FET for charging action
VIOUT	B4	44	I/O	Vibrator output
V_{REG1}	E2	6	O	Regulator 1 output
V_{REG2}	H2	13	O	Regulator 2 output
V_{REG3}	J3	15	O	Regulator 3 output
V_{REG4}	H5	18	O	Regulator 4 output
V_{REG5}	J6	20	O	Regulator 5 output
V_{REG6}	F2	10	O	Regulator 6 output
XRST	E1	7	O	Reset output

detailed description

power-on/-off control

The timing of the delayed power-on reset is controlled by the power-on/-off control circuit. There are two different conditions to power-on the device: manual power on and automatic power on.

manual power on

During the power-off state, after the power key is pressed, the PWRKIN signal becomes high and the output of V_{REG1} (regulator 1 output) is enabled. When the V_{REG1} output reaches 90% of its nominal output voltage, the TWL2214CA device starts the delayed reset process by charging the reset timing capacitor (CD1). When the voltage of CD1 reaches 1.2 V, the XRST signal is released by the TWL2214CA device and pulled high by an external pull-up resistor. The reset process is completed, and the external controller operates in normal condition. While PWRKIN remains high, the power-on condition remains active. Before PWRKIN goes low, the external controller must drive PSH high to retain power; otherwise, the TWL2214CA device starts the delay power-off process by charging timing capacitor CD2. After the voltage of CD2 reaches 1.2 V and no valid PSH signal is received, the device is powered off.

automatic power on

During the power-off state, after the adapter is attached, the output of V_{REG1} is automatically enabled. When V_{REG1} reaches 90% of its nominal output voltage, the TWL2214CA device starts the delayed reset process by charging the reset timing capacitor (CD1). When the voltage of the CD1 reaches 1.2 V, the XRST signal is released by the TWL2214CA device and pulled high by an external pull-up resistor. The reset process is completed and the external controller operates in normal condition. The external controller must drive PSH to high in time to retain power; otherwise, the TWL2214CA device starts the delay power-off process by charging timing capacitor CD2. After voltage of CD2 reaches 1.2 V and if no valid PSH signal is received, the device is powered off.

During the on state, the device generates an output signal PWRKOUT with an inverted polarity to PWRKIN. An external controller can use PWRKOUT to sense whether the power key has been pressed.

detailed description (continued)

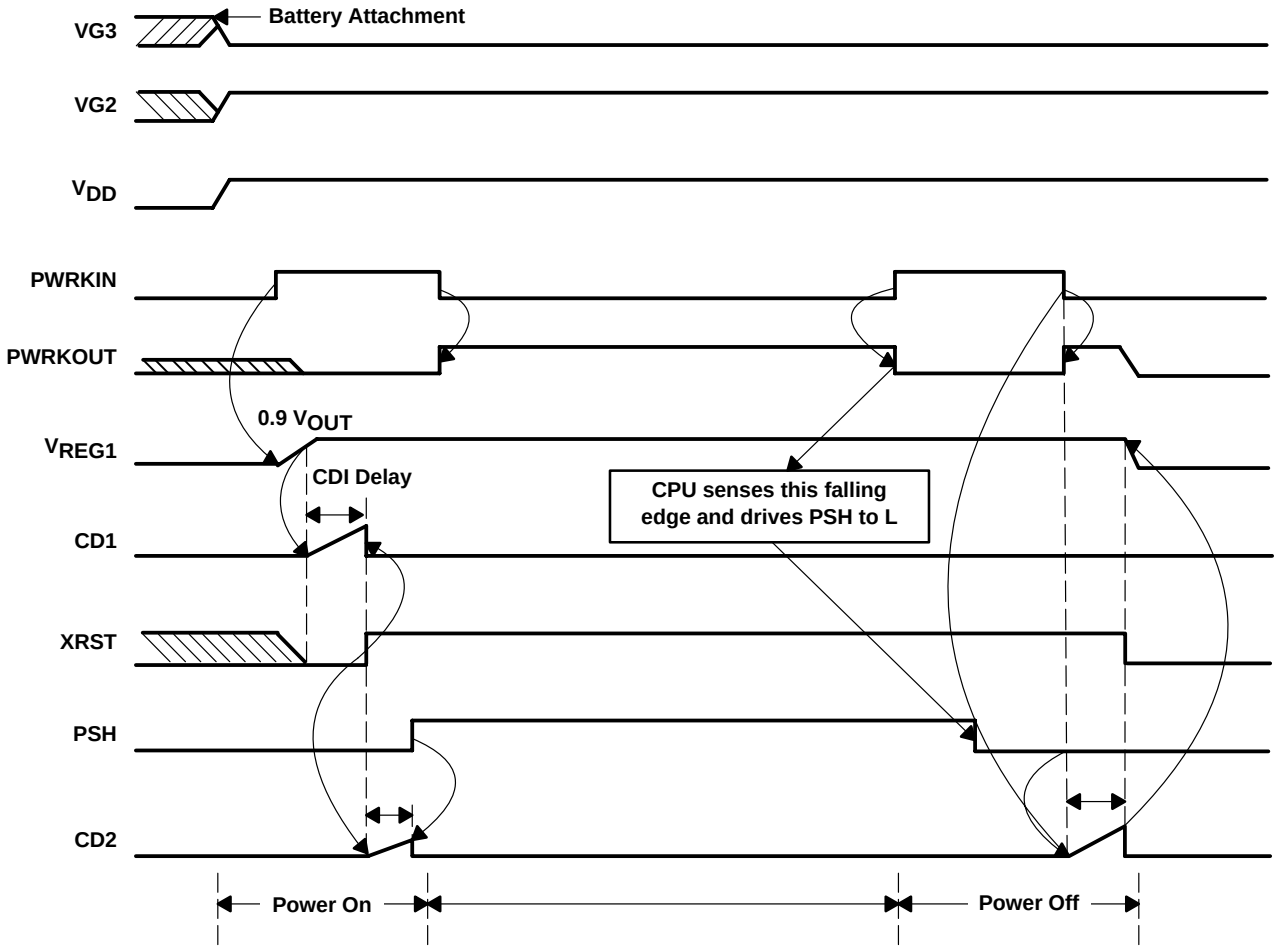


Figure 1. Power-On/-Off Sequence

detailed description (continued)

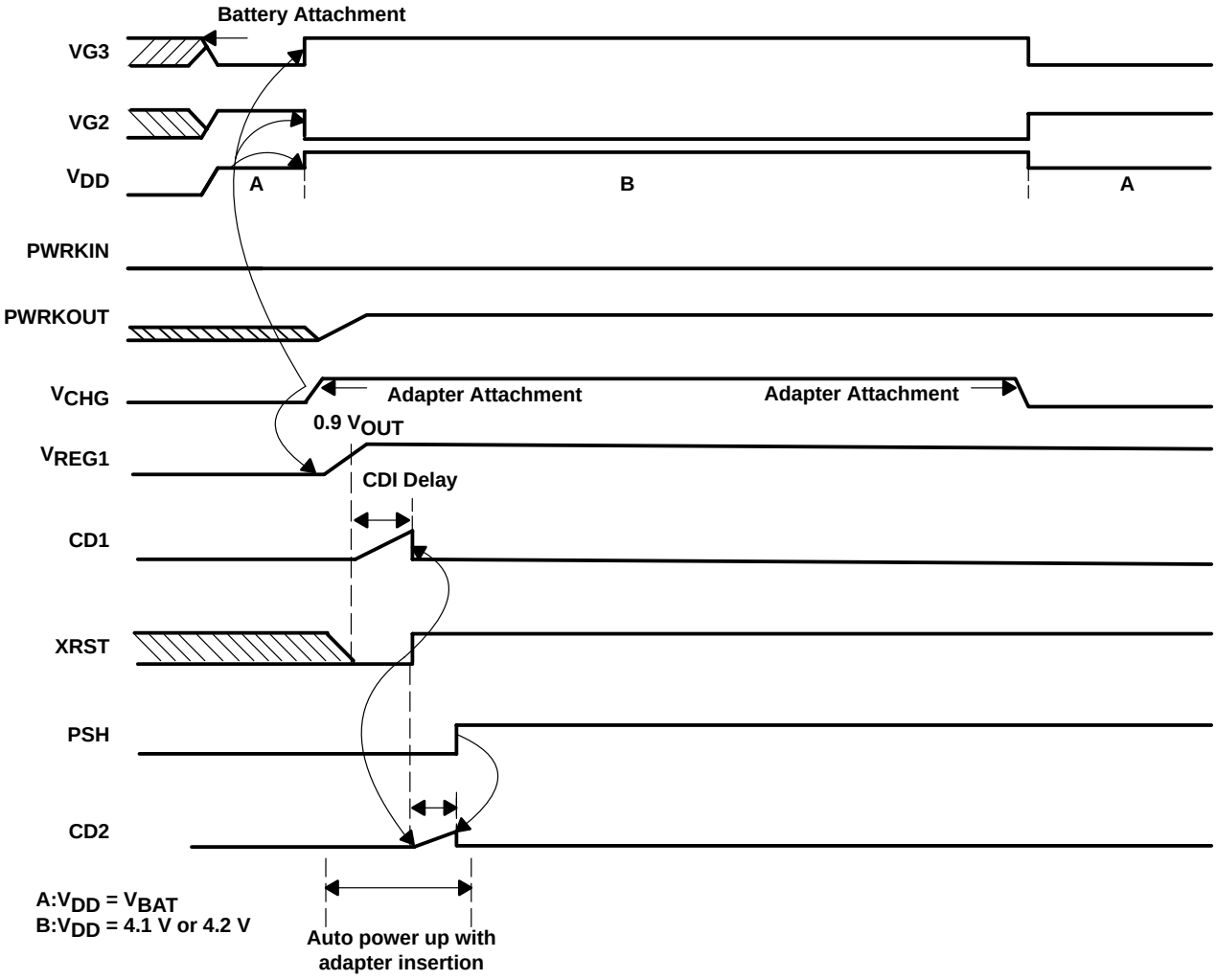


Figure 2. Adapter Powered (With Battery)

detailed description (continued)

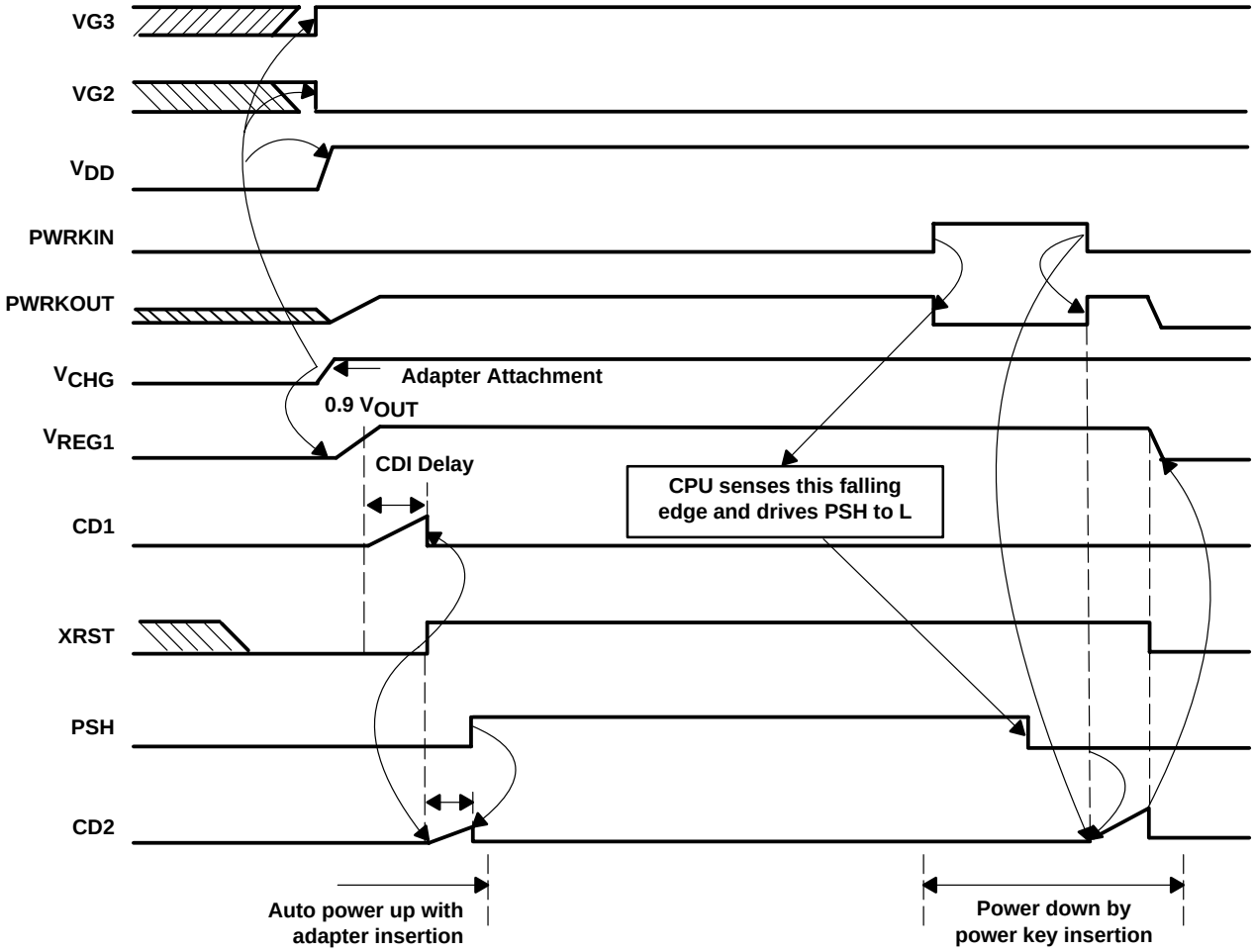


Figure 3. Adapter Powered (Without Battery)

reset controller

The reset controller performs two major functions: one is to control the timing of delayed power-on reset, and the other is to monitor the V_{REG1} level.

The delay reset process is started when V_{REG1} reaches 90% of its nominal output voltage level. The delay time of the reset output (XRST) can be adjusted by an external timing capacitor (CD1).

During the system active state when V_{REG1} drops below $0.9 \times V_{nominal}$ – hysteresis, XRST is driven low. If V_{REG1} reaches 90% of its nominal output voltage level again, the delayed reset process is started over.

detailed description (continued)

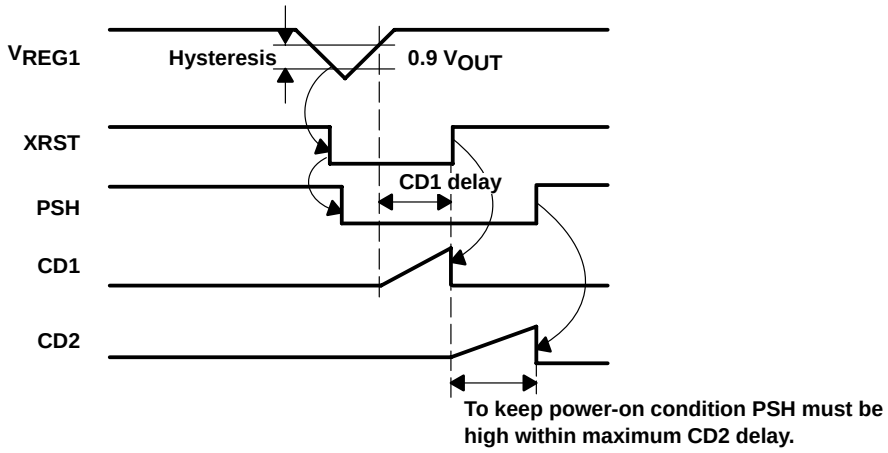


Figure 4. V_{REG1} Monitoring of Reset Control

regulator 1

This regulator is automatically enabled after the power-on process is complete. It stays enabled until the power-off condition occurs. Regulator 1 supplies power to the microprocessor. The nominal output voltage is 2.8 V and the maximum output current is 150 mA. Regulator 1 requires an output capacitor in the range of 4.7 μF to10 μF with an ESR less than 6 Ω.

regulator 6

This regulator output voltage can be enabled by I^2C by attaching CONT (terminal 21 or H6) to V_{DD}. Attaching CONT to GND makes this regulator automatically enabled with power on. The output voltage is programmed by I^2C. The maximum output current of 100 mA requires an output capacitor in range of 4.7 μF to 10 μF, with ESR in the range of 1 Ω to 6 Ω. The output voltage ranges from 2.5 V to 3 V.

regulators 2, 3, 4, and 5

Regulators 2, 3, 4, and 5 are output voltages programmed and enabled by I^2C. The output voltage ranges from 2.3 V to 3 V in 100-mV steps. The maximum output current for regulators 2 and 3 is 80 mA, for regulator 4 it is 120 mA, and for regulator 5 it is 150 mA. The default output voltage for all regulators is 3 V. These regulators have very low output noise (maximum 30 μV_{RMS}); they are suitable for powering up the RF block, which requires an output capacitor in the range of 4.7 μF to 10 μF with an ESR less than 6 Ω.

vibrator driver

The TWL2214CA device has incorporated a vibrator driver with selectable output voltage and current. This integrated vibrator driver has the same features as the other LDO regulators. The vibrator is enabled by I^2C. The output voltage can be selected by tying SEL (terminal 4 or D2) to V_{DD} or GND. If SEL is tied to V_{DD}, the output voltage is set to 3 V. If SEL is tied to GND, the output voltage is set to 1.3 V.

LED driver

The TWL2214CA device provides the capability of driving three LEDs. These drivers, enabled by I^2C, can drive currents of 160 mA, 20 mA, and 10 mA individually with a maximum voltage drop of 0.8 V.

ringer driver

The TWL2214CA device provides the capability of driving a ringer. It is enabled by I^2C and uses an N-channel FET with a maximum resistance of 3 Ω.

dual-interface serial bus: DISB

The DISB is a three-wire interface bus that incorporates both Phillips I^2C and three-wire SPI. The SPI interface used here is different from the standard SPI interface; it combines both transmit and receive channels into one bidirectional port. It also incorporates the slave addressing topology to work like a bus and control many devices at the same time. The interface does not have a selection pin to choose between the two protocols. It uses the clock enable line to distinguish the communication format of the interface. When clock enable is high, the clock and data lines work as a standard I^2C interface. However, on the falling edge of clock enable, the device expects the SPI protocol defined in the following section. The protocol includes a slave address identifier that allows the lines to be connected to many devices similar to that of I^2C serial bus. Speed also improves when eliminating the master wait period to receive an acknowledge from the slave device.

battery charger control

This block provides the necessary signals to control the external circuits that perform the charger function. The charging activities include battery pack wake-up, precharge, fast charge, and battery temperature monitoring. This block also provides 2 ADC inputs for general measurement purposes. The input voltage level is from 0 V to 2 V. This block also includes an oscillator generator circuit, which generates the clocks for the device. The nominal frequency of the main clock is 500 kHz. It requires an external capacitor of 470 pF.

reference system

This block provides voltage reference and bias current for the internal circuitry.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

V_{CHG} to GND . . . . . –0.3 V to 12 V
All other terminals relative to GND . . . . . –0.3 V to 6.5 V
Operating ambient temperature . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –25°C to 150°C
Storage temperature range, T_{STG} . . . . . –55°C to 150°C
Soldering temperature (for 10 seconds) . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	MAX	UNIT
V_{CHG}	4.5	6	V
V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}	3.3	4.3	V
High-level logic input, PWRKIN, SEL, CONT	$0.7V_{DD1}$	V_{DD1}	V
Low-level logic input, PWRKIN, SEL, CONT	GND	$0.3V_{DD1}$	V
High-level logic input, PSH and CE	$0.7V_{REG1}$	V_{REG1}	V
Low-level logic input, PSH and CE	GND	$0.3V_{REG1}$	V
Precharge current		100	mA
Operating free-air temperature, T_A	–40	85	°C

logic level output

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH} of terminals PWRKOUT, IRQ, CE	I_{OH} = –2 mA	$0.8V_{REG1}$	V_{REG1}	V
V_{OL} of terminals PWRKOUT, IRQ, CE	I_{OL} = 2 mA	GND	$0.22V_{REG1}$	V
V_{OL} of DATA	I_{OL} = 2 mA	GND	$0.22V_{REG1}$	V
V_{OH} of XRST	I_{OH} = –2 mA (open drain with 100 kΩ internal pullup)		V_{REG1}	V
V_{OL} of XRST	I_{OL} = 2 mA (open drain 100 kΩ internal pullup)	GND	$0.22V_{REG1}$	V

electrical characteristics, T_A = –25°C to 85°C (unless otherwise noted)

regulator 1 (C_O = 4.7 μF with ESR = 2 Ω)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD1}	Input voltage		3.3		4.3	V
V_{REG1}	Output voltage	$I_O = I_{MAX}$	2.68	2.8	2.91	V
I_O	Output current	V_{DD1} = 3.8 V			150	mA
I_{OS}	Short circuit	V_{DD1} = 3.8 V			550	mA
	Load regulation	I_O = 1 mA to I_{MAX}, V_{DD1} = 3.8 V			80	mV
	Line regulation	V_{DD1} = 3.3 V to 4.3 V, $I_O = I_{MAX}$			20	mV
	Dropout voltage	$I_O = I_{MAX}$		100	300	mV
PSRR	Ripple rejection	f = 10 Hz to 10 kHz, V_{DD1} = 3.8 V		65		dB
$I_{(Standby)}$	Standby current	I_O = 1.5 mA (regulator 1 and internal bias circuitry are active)		105	120	μA

regulator 6 (C_O = 4.7 μF with ESR = 2 Ω)

This 100-mA LDO can be enabled with serial interface I²C or by CONT (terminal 21 or H6). The output range is from 2.5 V to 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD2}	Input voltage		3.3		4.3	V
V_{REG6}	Output voltage	CONT = Low	2.88	3	3.12	V
		CONT = High (see Note 1 and function register 4)	$0.96V_p$	V_p	$1.04V_p$	V
I_O	Output current				100	mA
	Short circuit				330	mA
	Load regulation	I_O = 1 mA to I_{MAX}, V_{DD2} = 3.8 V			70	mV
V_S	Line regulation	V_{DD2} = 3.3 V to 4.3 V, $I_O = I_{MAX}$			20	mV
	Dropout voltage	$I_O = I_{MAX}$		100	300	mV
PSRR	Ripple rejection	f = 10 Hz to 10 kHz, V_{DD2} = 3.8 V		65		dB
t_{ON}	Turnon time	See Note 2			150	μs
t_{OFF}	Turnoff time	See Note 3		2	5	ms
$I_{(Quiescent)}$	Quiescent current	I_O = 1.5 mA		15	30	μA

NOTES: 1. I²C/SPI programmable, $V_{(p)}$ is the programmed voltage. Refer to function registers 2 and 3 for programming information.
2. Output enable to output voltage = 0.9 × nominal value
3. Output disable to output voltage = 0.5 V

electrical characteristics, T_A = –25°C to 85°C (unless otherwise noted) (continued)

regulators 2, 3, 4, and 5 (C_O = 4.7 μF with ESR = 2 Ω)

Regulators 2, 3, 4, and 5 provide programmable output. The output range, 2.3 V to 3 V, can be programmed in 100-mV steps.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		3.3		4.3	V
V_O	Output voltage	See Note 1	$0.96V_p$	V_p	$1.04V_p$	V
I_O	Output current	Regulator 2			80	mA
		Regulator 3			80	
		Regulator 4			120	
		Regulator 5			150	
	Short-circuit current	Regulator 2			300	mA
		Regulator 3			300	
		Regulator 4			400	
		Regulator 5			500	
	Load regulation	Regulator 2, I_O = 1 mA to I_{MAX}			70	mV
		Regulator 4, I_O = 1 mA to I_{MAX}			50	
		Regulators 3 and 5, I_O = 1 mA to I_{MAX}			50	
	Line regulation	V_I = 3.3 V to 4.3 V			20	mV
$V_{DROPOUT}$	Dropout voltage	$I_O = I_{MAX}$			300	mV
PSRR	Ripple rejection	f = 10 Hz to 10 kHz, $V_{DD3} = V_{DD4}$ = 3.8 V		65		dB
N	Output noise	f = 10 Hz to 100 kHz, $I_O = I_{MAX}$, V_I = 3.3 V		45		μVrms
t_{ON}	Turnon time	See Note 2			80	μs
t_{OFF}	Turnoff time	No load, See Note 3		1	5	ms
$I_{(Quiescent)}$	Quiescent current	I_O = 1 mA		120	150	μA

regulator 1 voltage DET

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage at XRST (see Note 4)	$V_{REG1} \le V_{TH} - V_{HY}$		0	0.3	V
		$V_{REG1} \ge V_{TH}$		V_{REG1}		
V_{HY}	Hysteresis voltage		80	100	120	mV
	Time delay voltage at CD1		1.15	1.2	1.25	V
	Time delay current at CD1		0.7	1	1.3	μA

NOTE 4: V_{TH} is 90% of the nominal V_{REG1}.

LED driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output current at IL0	V_{IL0} = 0.8 V			160	mA
	Output current at IL1	V_{IL1} = 0.8 V			20	mA
	Output current at IL2	V_{IL2} = 0.8 V			10	mA
I_{LKG}	Leakage current	Off			1	μA

electrical characteristics, T_A = –25°C to 85°C (unless otherwise noted) (continued)

vibrator driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD5}	Input voltage		3.3		4.3	V
V_O	Output voltage	SEL = H	2.88	3	3.12	V
I_O	Output current	SEL = H			85	mA
V_O	Output voltage	SEL = L	1.17	1.3	1.43	V
I_O	Output current	SEL = L			140	mA
V_S	Line regulation	V_{DD5} = 3.3 V to 4.3 V, I_{OUT} = I_{MAX}			20	mV
	Load regulation	I_{OUT} = 1 mA to I_{MAX}, V_{DD5} = 3.8 V			80	mV
$I_{(Quiescent)}$	Quiescent current	I_{OUT} = 0			80	μA
I_L	Current limit	V_O = 0, V_{DD5} = 3.3 V to 4.3 V			490	mA

ring driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	On resistance	I_{OUT} = 100 mA at 25°C			3	Ω
I_{LKG}	Leakage current	Off			1	μA

battery charger control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CHG} input			4.2		6.5	V
V_{DD1}	System V_{DD}	V_{BREG} = 4.1 V	4.059	4.1	4.141	V
		V_{BREG} = 4.2 V (see *function control register*)	4.158	4.2	4.242	
V_{REF}		Required 0.1-μF capacitor ESR of 2 Ω , load = 1 mA maximum	2.91	3	3.09	V
$V_{(current\ sense)}$	Current sense voltage	Set maximum current, 100 to 200, 20-mV steps with I^2C, See CSV register		V_{SENSE}		mV
VG	VGH	IGH = 0 mA		V_{CHG}		V
	VGL	IGL = 0 mA		0		V
IG	IGH	VG = 2 V	149	178.5	197	μA
	IGL		214	218	226	
VG2	VG2H	IG2H = 0 mA		V_{BAT}		V
	VG2L	IG2L = 0 mA		0		
IG2	IG2H	VG2 = V_{BAT} – 0.3 V	–2.8	–4.03	–4.65	mA
	IG2L	VG2 = 0.3 V	3.2	5.02	5.70	
VG3	VG3H	IG3H = 0 mA		V_{DD1}		V
	VG3L	IG3L = 0 mA		0		
IG3	IG3H	VG3 = V_{DD1} – 0.3 V	–2.7	–3.87	–4.65	mA
	IG3L	VG3 = 0.3 V	2.95	4.43	5.3	

electrical characteristics, T_A = –25°C to 85°C (unless otherwise noted) (continued)

battery charger control (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT} regulation (CV)		V_{BREG}† = 4.1 V	4.059	4.1	4.141	V
		V_{BREG} = 4.2 V	4.158	4.2	4.242	
V_{BAT}	Low voltage cutoff			1.9		V
	High voltage cutoff			4.45		
	Fast charge voltage			3.2		
	Precharge voltage	(see Note 5)	1.9	2.05	2.2	
	Pack wake-up voltage		4.214	4.30	4.386	
I_{CC}	Operating current			20		mA

† V_{BREG} is the regulated battery voltage programmed by setting bit 1 of CSV register.

NOTES: 5. Precharge current set by $I_{PRE} = \frac{V_{PRE}}{R_{PR}} \times 45$ where $V_{PRE} = 1.2\ V \pm 10\%$

ADC specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Output impedance <100 kΩ		8		bit
Integral nonlinearity	Confirm monotonous (see Note 6)	–1		1	LSB
Low-level input	ADC output = 00H	0		0.1	V
High-level input	ADC output = FFH	1.9	2	2.1	V
Input capacitance			3		pF
ADC CLK		450	500	550	kHz
AD conversion time, t_C	From the start of SETUP		16		CLK
Power-up time	From the ADEN up selection			10	µs

NOTE 6: LSB = $\frac{2V}{255}$ = 7.8 mV

DISB interface

The TWL2214CA device supports both I^2C bus and SPI bus serial interfaces. The interface uses serial data (DATA) and serial clock (CLK) to carry information between the devices. The CE terminal (A8) in the GQE package selects I^2C or SPI. The device that initiates a transfer, generates clock signals, and terminates a transfer is the master. The TWL2214CA device operates as a slave device. The slave address for this device is fixed at E4h for write operations and E5h for read operations. The LSB of this slave address is simply an R/$\overline{W}$ flag. DATA is a bidirectional line connected to V_{REG1} via a 10-kΩ pullup resistor. Data can be transferred at a rate up to 400K bits/s for I^2C and up to 2M bits/s for SPI with one clock pulse generated for each data bit transferred. MSB is transferred first. When the bus is free, both DATA and CLK are high. Data transfer can only be initiated when the bus is free. The bus must return to the free state when the transfer is complete. Failure to return to the free state may cause an error.

SPI bus protocols

The TWL2214CA serial bus is SPI-compatible when a negative transition is generated on the CE input (A8) in the GQE package.

Unlike I^2C, in this mode, the slave device does not send an acknowledge bit for all data received. The data frame includes 2 start bits, 1 byte of slave address, 1 byte of register address, 1 byte of data, and half clock cycle of hold time. The total frame length, therefore, includes 26 full clock cycles and the rising edge of the 27^{th} clock cycle. After the rising edge of the 27^{th} clock cycle, CLK remains high.

The following requirements must be satisfied for the interface:

1. CE goes low after the falling edge of CLK and remains low for no longer than 35 clock cycles. The data line must remain unchanged prior to the initial trailing edge of the CLK line. Failure to comply triggers the I^2C start condition and the SPI interface fails.
2. Input data is sampled on the rising edge of the CLK when CE is set to low.
3. Input data is latched into the device on the last (26^{th}) rising edge of the CLK.
4. If CE goes high before completing the transmission, data is ignored and the register is not updated.
5. Output data is updated on the falling edge of the CLK when CE is set to low.
6. The first two bits in the data line are dead bits to allow enough time for the communication mode option selection of the SPI.
7. During a read operation the direction of data line changes after the register address is received.

SPI bus protocols (continued)

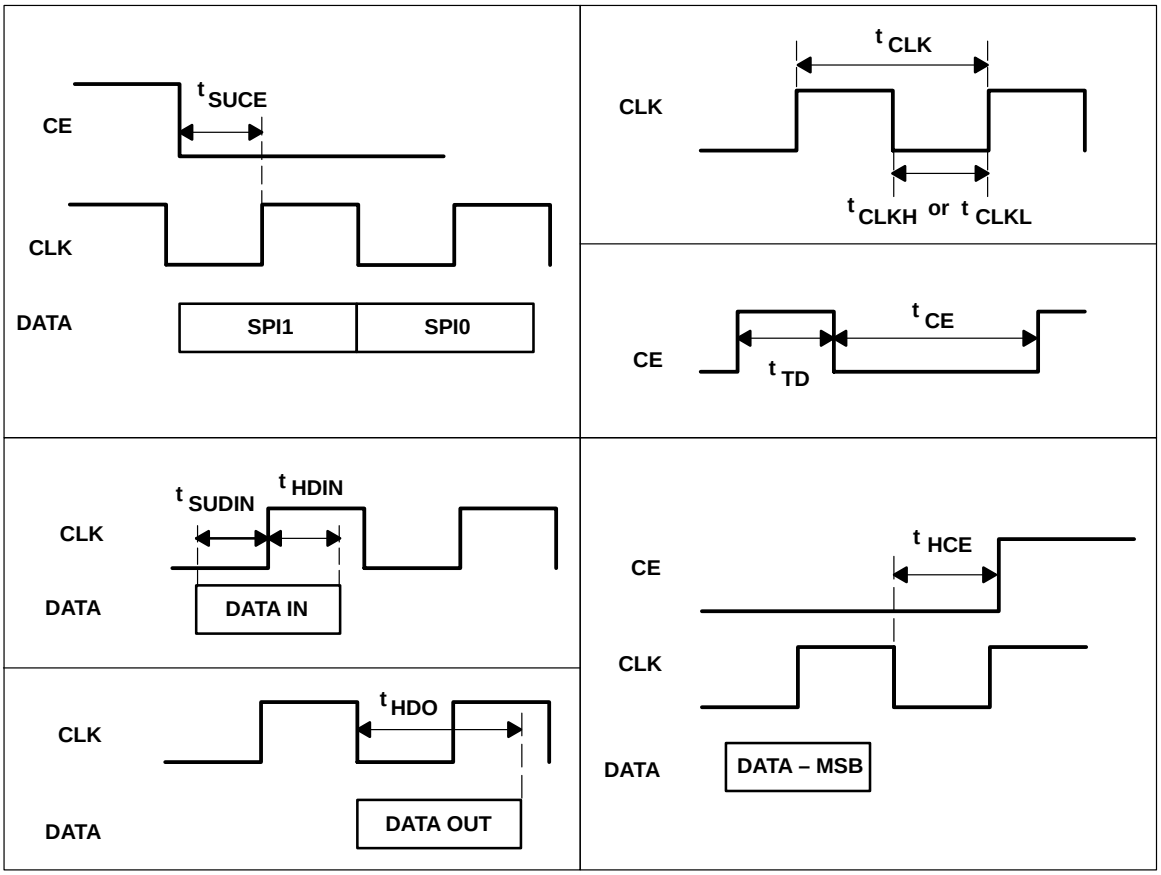


Figure 5. SPI Protocol Timing

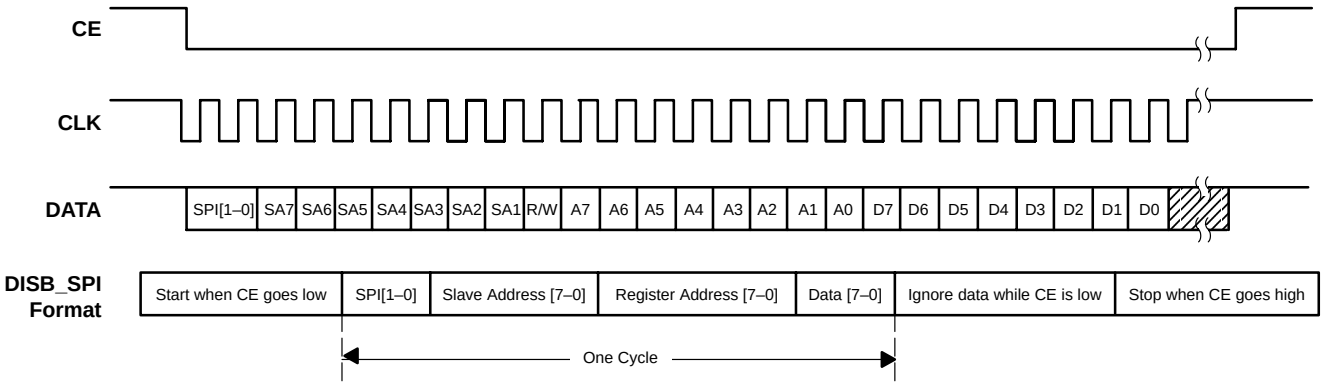


Figure 6. SPI Read and Write

SPI timing requirements (see Figure 5)

PARAMETER		MIN	MAX	UNIT
t_{CLK}	Clock period	500		ns
t_{CLKL}	Clock low time	200		ns
t_{CLKH}	Clock high time	200		ns
t_{TD}	Interframe transfer delay	5		t_{CLK}
t_{CE}	CE low transition period	27	35	t_{CLK}
t_{SUCE}	Clock enable setup time	50		ns
t_{HCE}	Clock enable hold time	0		ns
t_{SUDIN}	Input data setup time	50		ns
t_{HDIN}	Input data hold time	50		ns
t_{HDO}	Output data hold time	t_{CLK}–50	t_{CLK}	ns
t_r	Clock or data rise time		20	ns
t_f	Clock or data fall time		20	ns

I²C bus protocols

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TWL2214CA device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TWL2214CA device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TWL2214CA device must leave the data line high to enable the master to generate the stop condition.

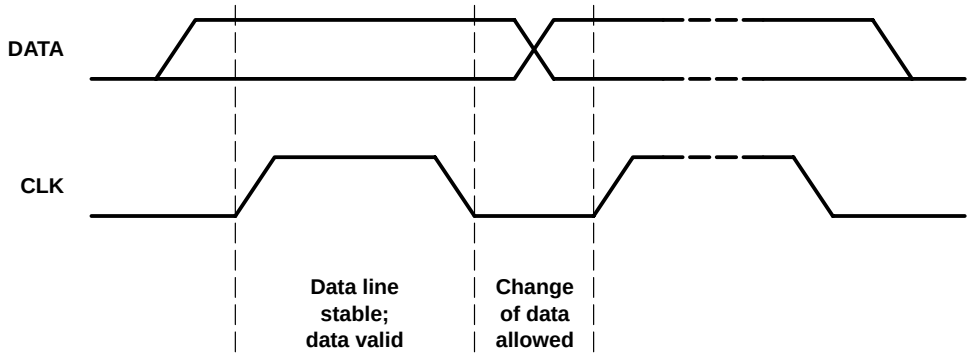


Figure 7. Bit Transfer on the I²C Bus

I²C bus protocols (continued)

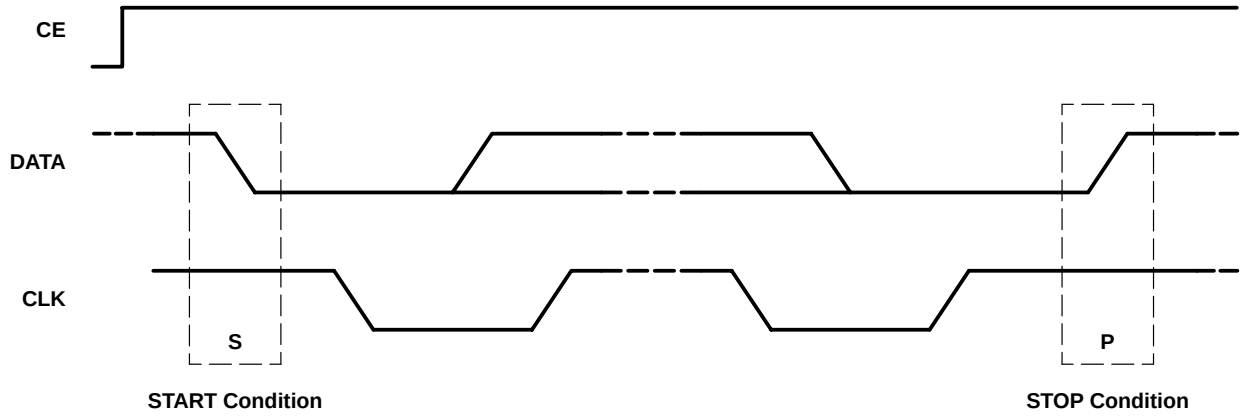
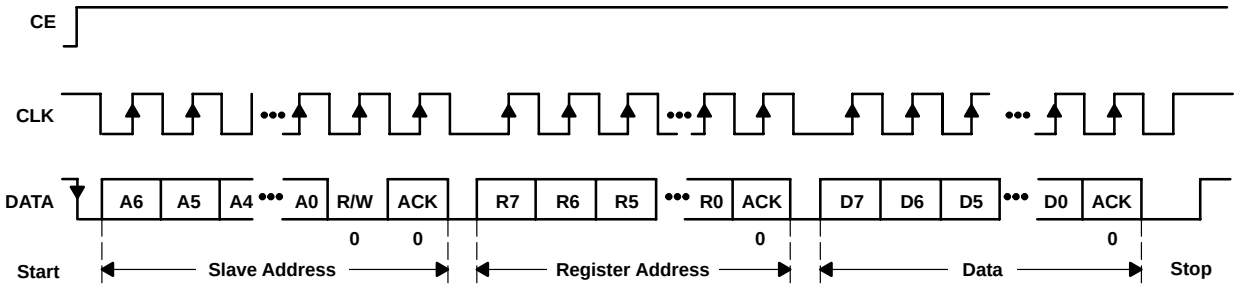
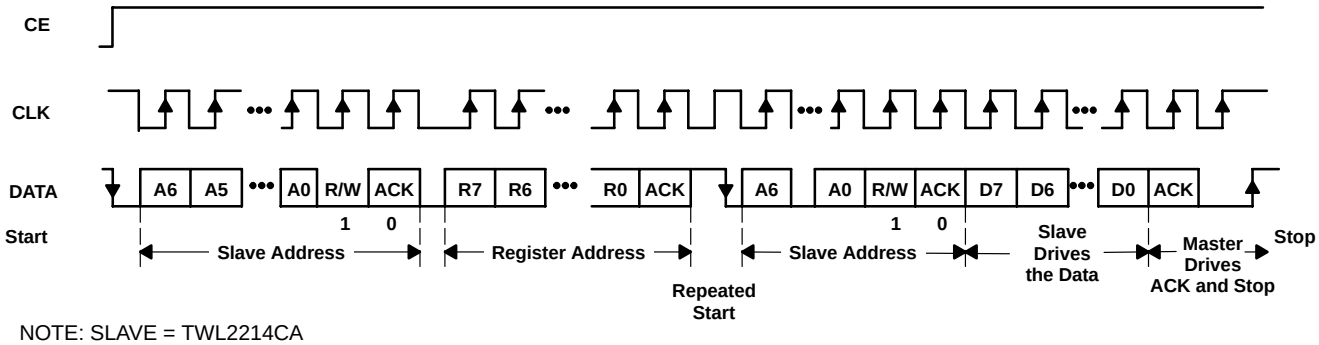


Figure 8. START and STOP Conditions



NOTE: SLAVE = TWL2214CA

Figure 9. I²C Bus Write to TWL2214CA Device



NOTE: SLAVE = TWL2214CA

Figure 10. I²C Read From TWL2214CA Protocol A

I²C bus protocols (continued)

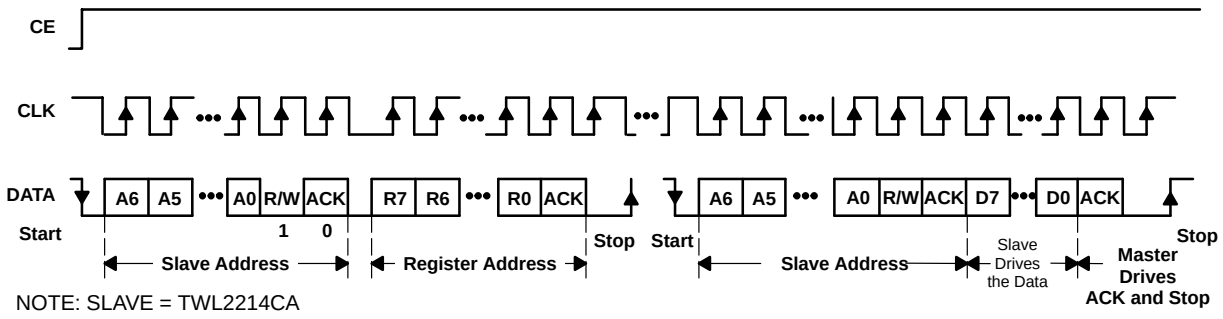
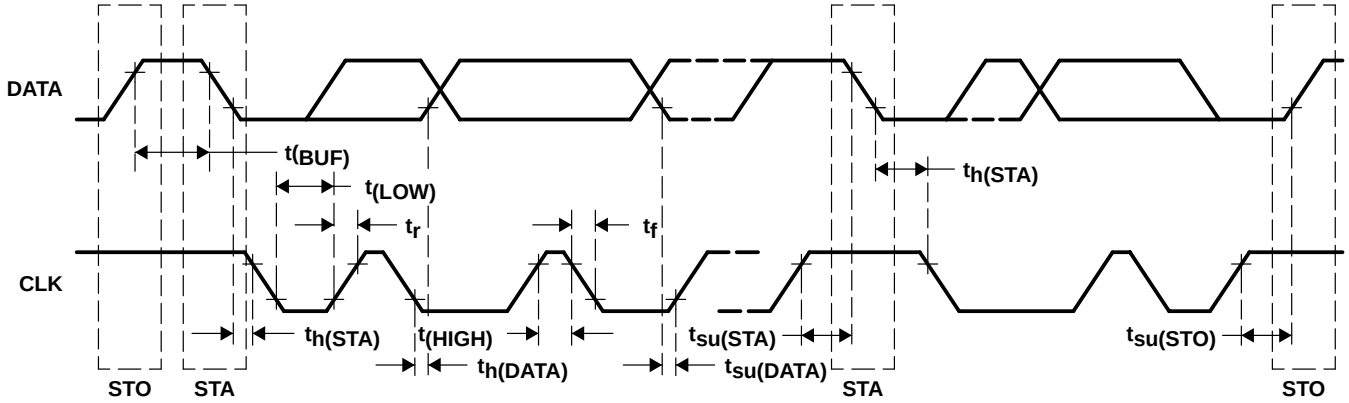


Figure 11. I²C Read From TWL2214CA Protocol B

I²C timing



	MIN	MAX	UNIT
Clock frequency, f_{MAX}		400	kHz
Clock high time, $t_{wH(HIGH)}$	600		ns
Clock low time, $t_{wL(LOW)}$	1300		ns
DATA and CLK rise time, t_R		300	ns
DATA and CLK fall time, t_F		300	ns
Hold time (repeated) START condition (after this period the first clock pulse is generated), $t_{h(STA)}$	600		ns
Setup time for repeated START condition, $t_{h(DATA)}$	600		ns
Data input hold time, $t_{h(DATA)}$	0		ns
Data input setup time, $t_{su(DATA)}$	100		ns
STOP condition setup time, $t_{su(STO)}$	600		ns
Bus free time, $t_{(BUF)}$	1300		ns

Figure 12. I²C Bus Timing Diagram

register map

charger

REGISTER	ADDRESS (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PTR: Precharge timer register	10h (R/W)	0 = Disable 1 = Enable	00000 = 0 minutes ⋮ 11111 = 136 minutes in 4-minute steps					Don't care	
	Default	0	0	0	0	0	0		
CCTR: CC charge timer register	11h (R/W)	0 = Disable 1 = Enable	00000 = 0 minutes ⋮ 11111 = 273 minutes in 8-minute steps					Don't care	
	Default	0	0	0	0	0	0		
TCTR: Total charge timer (CC+CV) register	12h (R/W)	0000 = 0 hours ⋮ 1111 = 15 hours in 1-hour steps				Don't Care			
	Default	1	1	1	1				
VBOTRH+: Battery over temperature register at High+	13h (R/W)	00h = 0 V ⋮ FFh = 2 V							
	Default	00h = 0 V							
VBOTRH–: Battery over temperature register at High–	14h (R/W)	00h = 0 V ⋮ FFh = 2 V							
	Default	00h = 0 V							
VBOTRL: Battery over temperature register at low	15h (R/W)	00h = 0 V ⋮ FFh = 2 V							
	Default	00h = 0 V							
CSV: Charge current sensing voltage and termination current ratio	16h (R/W)	Sensing voltage 000 = 100 mV ⋮ 101 = 200 mV in 20-mV steps			Termination current ratio 000 = 10% ⋮ 100 = 50% in 10% steps			0 = 4.1 V 1 = 4.2 V	Don't care
	Default	0	0	0	0	0	0	0	
ADBV: Battery voltage	17h (R)	VABV = 2 V × 2.5 × Value/256							
ADBT: Battery temperature voltage	18h (R)	VADBAT = 2 V × Value/256							
ADCIN1: Voltage	19h (R)	VADCIN1 = 2 V × Value/256							
ADCIN2: Voltage	1Ah (R)	VADCIN2 = 2 V × Value/256							

charger (continued)

REGISTER	ADDRESS (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
FCR1: Function control	1Bh (R/W)	CHGSTR 0 = 1 = Charger Start See Note 7	ADC status 0 = Disable 1 = Enable See Notes 7 and 8	ADC function 0 = Single 1 = Periodically See Notes 7 and 8	ADBV 0 = Disable 1 = Enable See Notes 7 and 9	VTS 0 = Disable 1 = Enable See Notes 7 and 10	ADCIN1 0 = Disable 1 = Enable See Notes 7 and 10	ADCIN2 0 = Disable 1 = Enable See Notes 7 and 10	IRQ 0 = IRQ is L 1 = IRQ is H
	Default	0	0	0	0	0	0	0	0
SR: STATUS register	1Ch (R)	VEXT 1 = VCCHG in range	BATERR 1 = Battery error	VBOT 1 = Battery overvoltage	CTERM 1 = Charge current goes below termination out	NOCHG 1 = Charge condition, reset CHGSTR to 0. See Note 11	PCHG 1 = Precharge mode	CCTO 1 = CC charge timeout	TCTO 1 = Total charge time (CC+CV) out

NOTES: 7. After the TWL2214CA device has finished charging, these values are set to 0.
8. During CHGSTR H, ADC enables and periodically keeps functioning.
9. During charging mode ADVB is enabled automatically.
10. Charging mode is not necessary to set enable for function.
11. External microprocessor must set CHGSTR bit to 0 when NOCHG = 1

regulator, LED, VIBRATOR

REGISTER	ADDRESS (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
FCR2: Function register 2	20h (R/W)	REG2				REG3			
		0 = Disable 1 = Enable	000 = 3 V ⋮ 111 = 2.3 V in 100-mV steps			0 = Disable 1 = Enable	000 = 3 V ⋮ 111 = 2.3 V in 100-mV steps		
	Default	0	0	0	0	0	0	0	0
FCR3: Function register 3	21h (R/W)	REG4				REG5			
		0 = Disable 1 = Enable	000 = 3 V ⋮ 101 = 2.5 V in 100-mV steps			0 = Disable 1 = Enable	000 = 3 V ⋮ 101 = 2.5 V in 100-mV steps		
	Default	0	0	0	0	0	0	0	0
FCR4: Function register 4	22h (R/W)	REG6				Don't care			
		0 = Disable 1 = Enable See Note 12	000 = 3 V ⋮ 101 = 2.5 V in 100-mV steps						
	Default	0	0	0	0				
FCR5: Function register 5	23h (R/W)	Vibrator	Ringer	IL2	IL1	IL0	VG3_EN	Don't care	
		0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable		
	Default	0	0	0	0	0	0 See Note 13		

NOTES: 12. CONT = H, REG6 is dependent on D7 to enable. CONT = L, REG6 is independent of D7, always on after power up.
13. VG3_EN = 1, forces VG3 signal to Low. VG3_EN = 0, VG3 signal is at normal condition. Control of this bit is valid only when the adapter is connected.

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APPLICATION INFORMATION

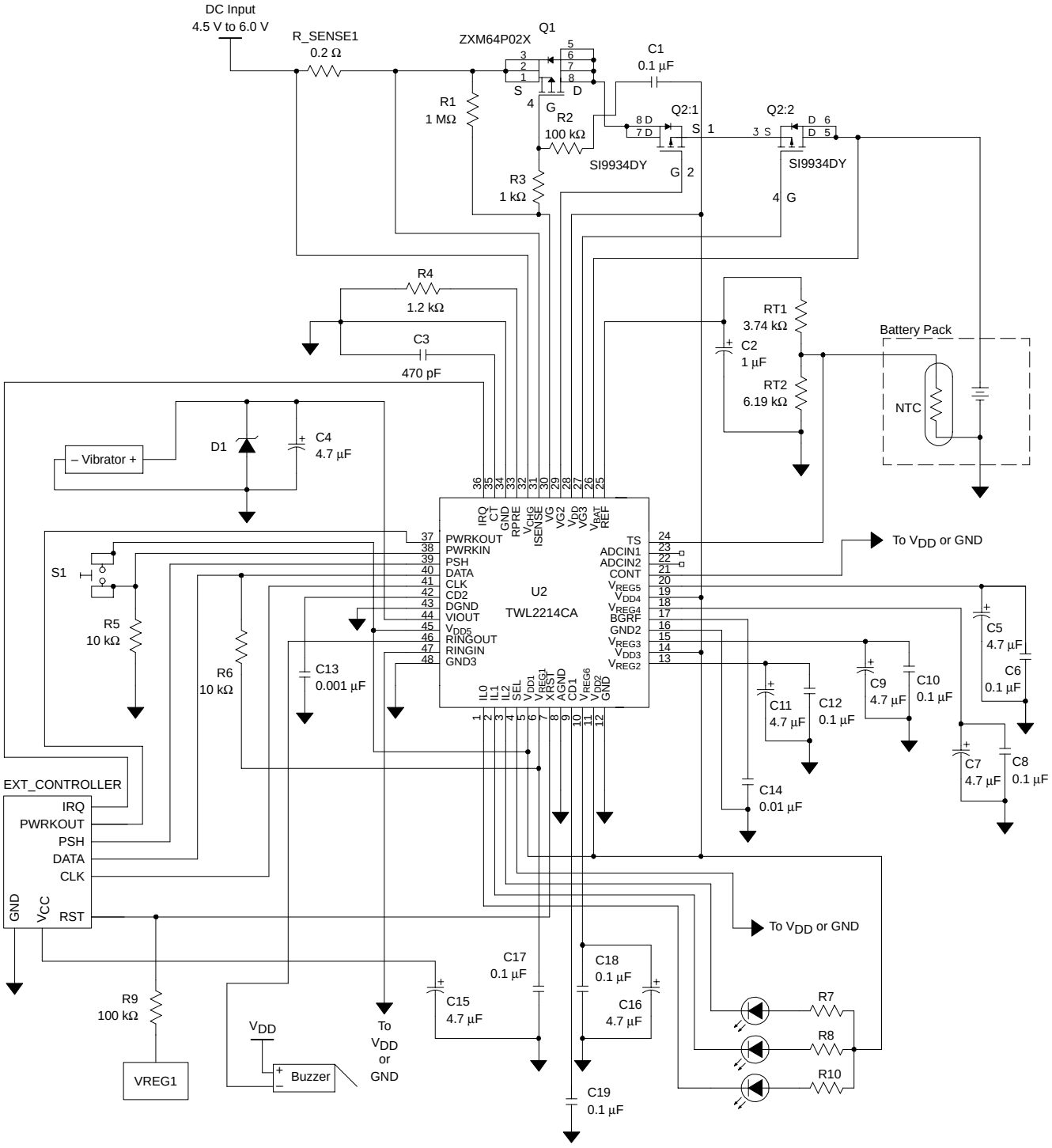


Figure 13. Typical Application Circuit (PFB)

APPLICATION INFORMATION

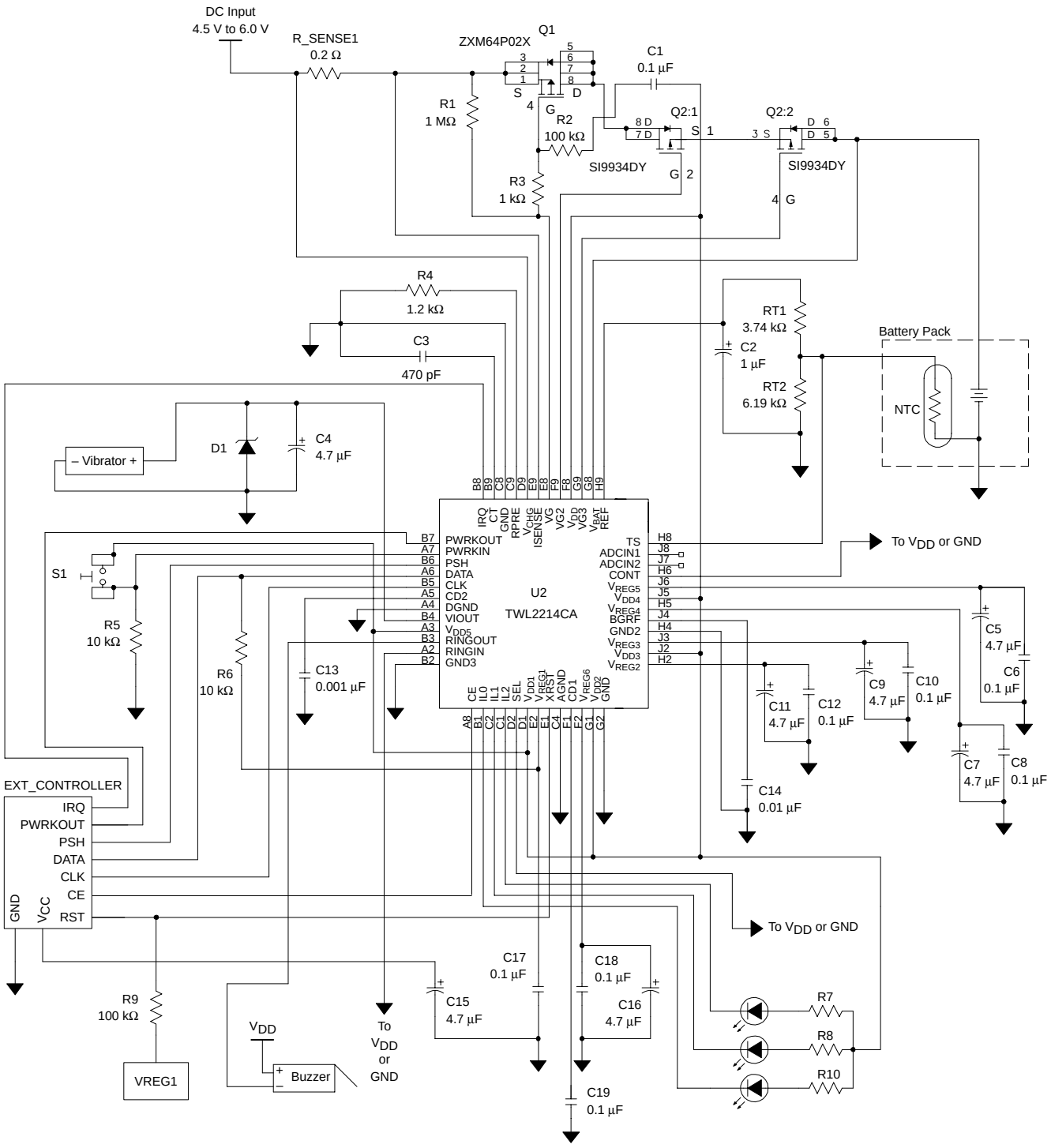
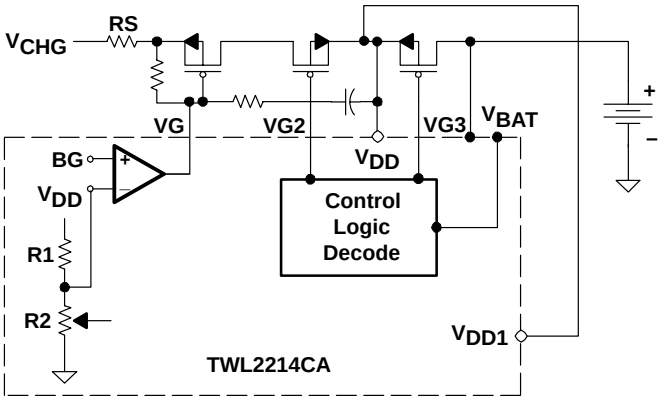


Figure 14. Typical Application Circuit (GQE)

APPLICATION INFORMATION

device power supply control (V_{DD1})

The TWL2214CA device receives device power by regulating the V_{CHG} input to 4.1 V or 4.2 V, whenever V_{CHG} is available; otherwise, the device uses the V_{BAT} input directly as device dc supply. The regulated voltage from V_{CHG} is programmable through the I^2C interface.



BG: Band Gap Voltage
R1: Fixed
R2: Programmable

Figure 15. Device Power Supply

Condition 1: V_{CHG} is on (VG = Active, VG2 = On, VG3 = Off)

V_{DD1} = 4.1 V or 4.2 V

The TWL2214CA device sets R2 value according to the programmed voltage level (4.1 V or 4.2 V).

Condition 2: V_{CHG} is off and V_{BAT} applied (VG = High, VG2 = Off, VG3 = On)

V_{DD1} = VBAT

battery charger

The TWL2214CA device provides a charger function for single cell Li-Ion battery packs. The charging activity starts with the battery pack wake-up cycle. If the wake-up cycle completes successfully, the charger starts the precharge function and slowly charges the battery to 3.2 V. If the battery is charged to 3.2 V within the time limit, the charger goes into the fast charge mode. The fast charge mode has two phases: 1) constant current (CC) mode and 2) constant voltage (CV) mode. The charger starts CC mode with the maximal charging current until the battery voltage reaches the regulated voltage level; the charger is then switched to CV mode. During the CV mode, the TWL2214CA device monitors the charging current; once it is below the programmed termination current level, the charger activity is terminated. The termination current level can be programmed at 10%, 20%, 30%, 40%, or 50% of the maximum charging current at the CC mode.

APPLICATION INFORMATION

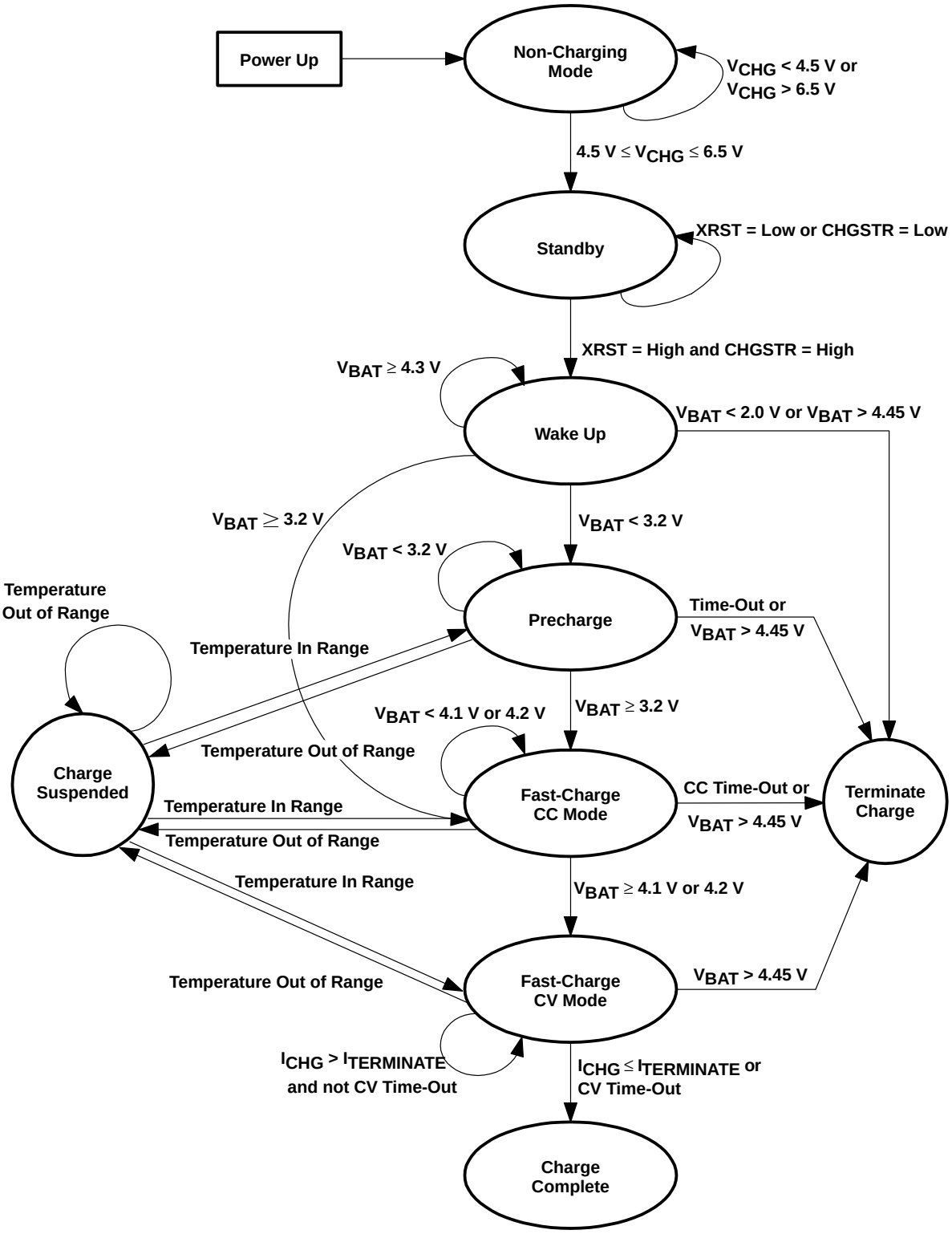


Figure 16. Charger State Diagram

APPLICATION INFORMATION

control register—FCR1 (1BH)

BIT	NAME	DESCRIPTION
7	CHGSTR	Set this bit to 1 to start the charger operation. This bit is cleared if the charger is terminated. (Refer to status register table below for terminated conditions)
6	ADC ENABLE	Set this bit to 1 to enable ADC operation, 0 to stop.
5	ADC FUNCTION	Set this bit to 1 to have ADC operate continuously. Set to 0 to have ADC to operate one cycle only.
4	ADBV	Set this bit to 1 to enable the V_{BAT} input channel to ADC. Clear this bit to 0 to disable the input channel.
3	VTS	Set this bit to 1 to enable the VTS input channel to ADC. Clear this bit to 0 to disable the input channel.
2	ADCIN1	Set this bit to 1 to enable the ADCIN1 input channel.
1	ADCIN2	Set this bit to 1 to enable the ADCIN2 input channel.
0	IRQ	Status of IRQ terminal (refer to IRQ operation section).

ADC has four input channels (ADBV, VTS, ADCIN1, and ADCIN2). Each channel can be enabled or disabled individually. The selected channel must be enabled before ADC FUNCTION and ADC ENABLE bits are enabled, the channel is included in the ADC operation.

IRQ control/status

The TWL2214CA device uses IRQ signal to inform the external controller about the exception condition of the V_{CHG} input and the charger status. Bit 0 reflects the state of the IRQ signal. IRQ occurs in the following five conditions:

1. V_{CHG} returns to operating range from nonoperating range.
2. V_{CHG} goes out of range from operating range.
3. Battery error—occurs only during the charging cycle.
4. Battery temperature out of range—occurs only during the charging cycle. The charger is suspended temporarily. IRQ is cleared when the temperature returns to normal and the charger resumes automatically.
5. Charge complete.

The controller must clear the IRQ signal by writing 0 to bit 0 in the interrupt service routine, except in the VBOT condition. The controller may miss the next interrupt if it fails to write the 0. In the VBOT condition, the TWL2214CA device clears the IRQ when the condition goes away.

APPLICATION INFORMATION

status register description—SR (1CH)

SR shows the status of the charger. The external controller reads the SR to track the state of the charging condition.

BIT	NAME	DESCRIPTION
7	Vext	When Vext = 1, the V_{CHG} input is in the operating range. Otherwise the V_{CHG} is out of range.
6	BATERR	This bit is set to 1 indicating battery error. Four cases cause battery error: precharge timeout, constant-current mode timeout, V_{BAT} < 2.9 V, or V_{BAT} > 4.45 V.
5	VBOT	During the charging cycle, if the battery temperature exceeds or falls below the nominal range, this sets to 1. The charger is suspended temporarily. VBOT is cleared when the temperature returns to nominal range and the charger function resumes automatically.
4	CTERM	The charger is terminated normally because the charging current is below the preset termination current value.
3	NOCHG	No charge condition. This condition is detected only during the wake-up state of the charging function. After the 8-second wake-up period expires, if V_{BAT} is above 4.3 V, the NOCHG flag is set. The cause of this is a missing or completely charged battery. The TWL2214CA device does not deactivate the charger by setting CHGSTR = 0. The external processor must turn off the CHGSTR bit by setting it to 0.
2	PCHG	Set to 1 to indicate the charger is in precharge state.
1	CCTO	Set to 1 to indicate the charging time has exceeded the time limit allowed during CC mode. This is a fatal error. The TWL2214CA device clears CHGSTR bit, sets the BATERR flag, and makes IRQ go high to interrupt the external controller.
0	TCTO	Set to 1 to indicate the charging time has exceeded the overall time limit allowed during CV mode. This is treated as normal termination of the charger function. The TWL2214CA device clears bit 7 (CHGSTR) of the control register and sets IRQ to 1 to interrupt the external controller.

APPLICATION INFORMATION

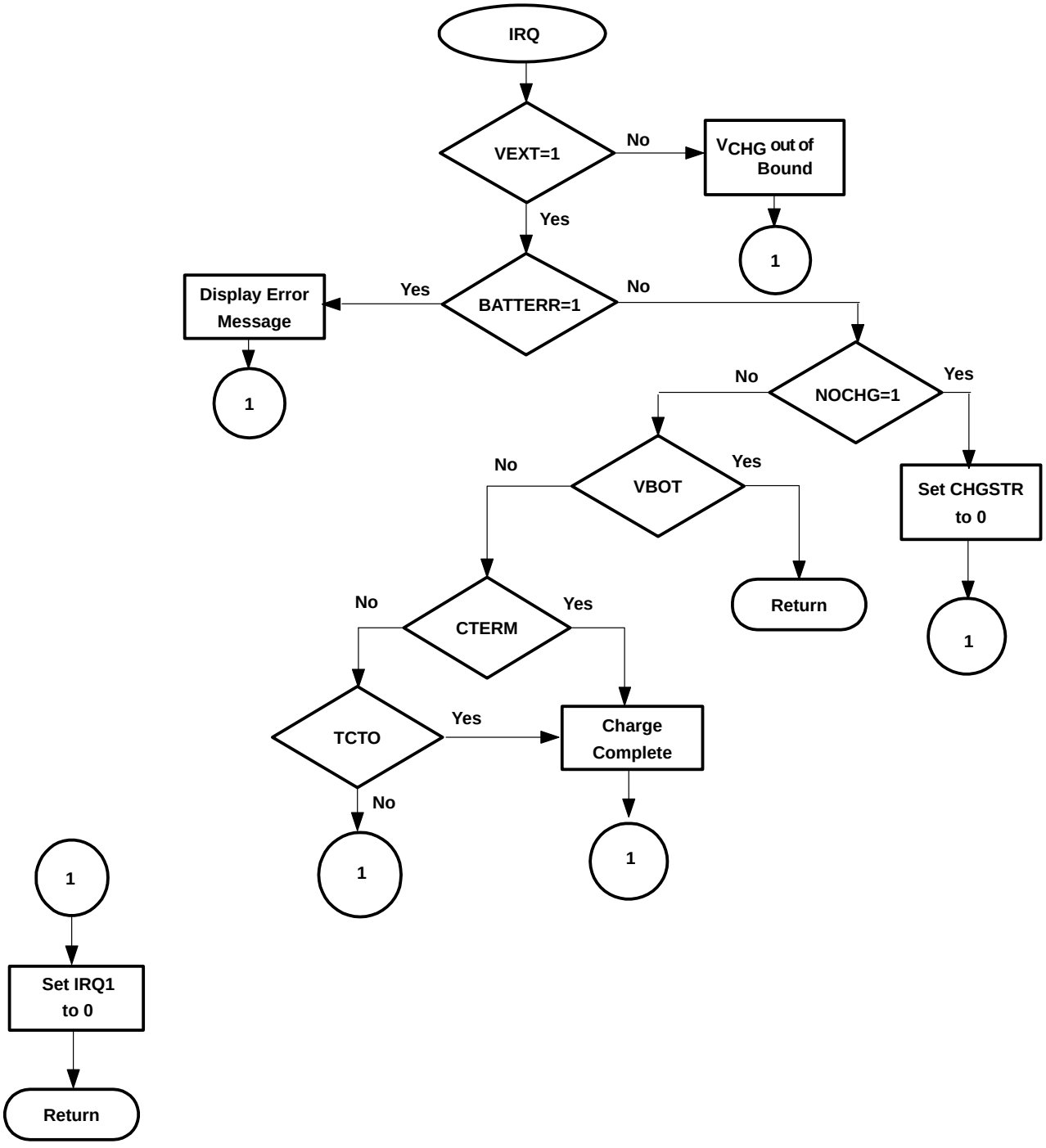


Figure 17. Charger State Diagram

APPLICATION INFORMATION

battery pack wake-up

Li-Ion cells can be easily damaged by overcharging or overdischarging. To prevent damage, a pack-protector device is used within the battery pack. During the charging cycle, if the pack-protector senses an over-voltage condition, it disconnects the pack from the charger to prevent further charging but allows discharging. During the discharging cycle, if the protector senses an under-voltage condition, it disconnects the cell from the load to prevent further discharging.

This phase of the charging cycle provides a wake-up capability for the battery pack with a pack-protector device. At the start of the charge cycle, the TWL2214CA device provides a wake-up signal of 1 mA and 4.3 V to the battery pack. At the end of the 8-second time limit, if the battery pack voltage remains at 4.3 V, a no-battery flag is set in the status register to signal the condition that the charging path is open. If the battery voltage is below 2.5 V, a BATTERR flag is set in the status register to signal a bad battery cell. In either case, the charging activity is halted.

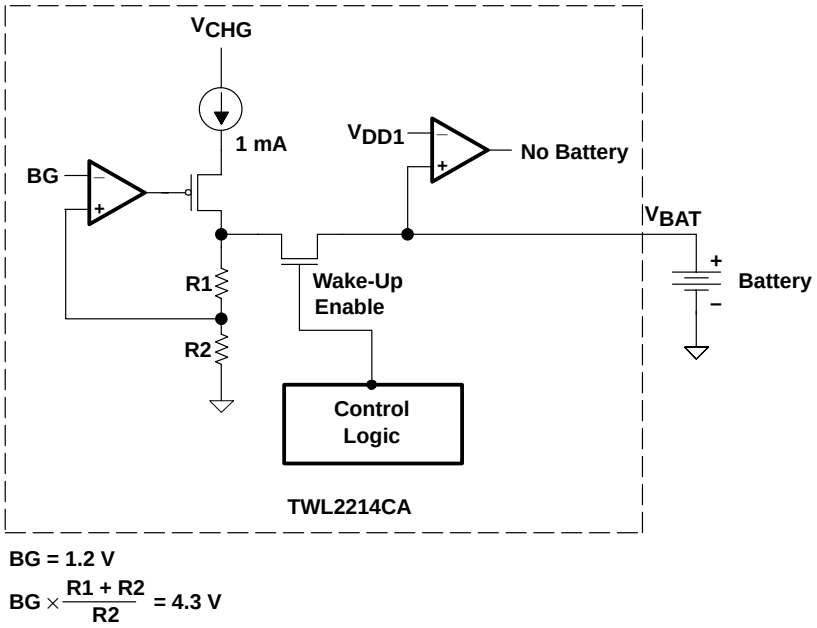


Figure 18. Battery Pack Wake Up

precharge

The TWL2214CA device starts the precharge phase when the battery voltage is less than 3.2 V. The precharge time is limited by the PTR timer. The precharge current level is set by an external resistor. The maximum precharge current the charger can supply is 100 mA. Use the following equation to choose the external resistor value.

$$R_{PR} = \frac{V_{PRE}}{I_{PRE}} \times 45, V_{PRE} = 1.2V \pm 10\%$$

Where:

R_{PR} = External resistor
I_{PRE} = Desired precharge current
V_{PRE} = Voltage at RPRE terminal

APPLICATION INFORMATION

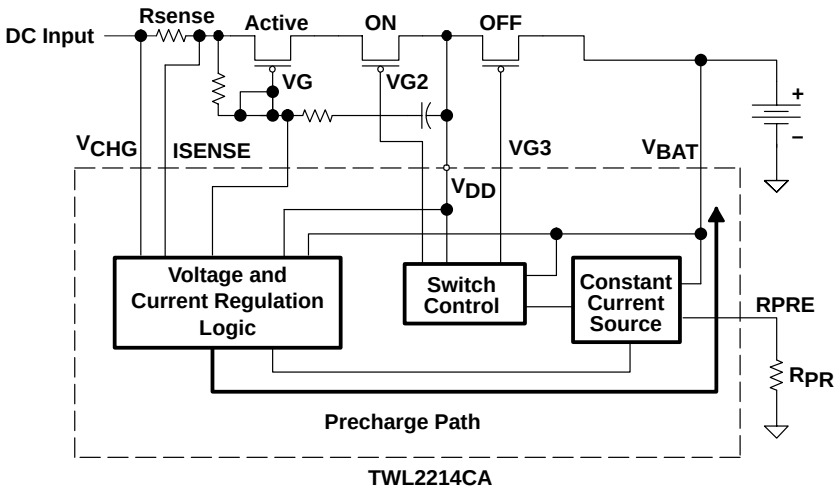


Figure 19. Precharge Functional Diagram

fast charge constant current (CC mode)

When the battery voltage is 3.2 V or higher, the TWL2214CA device starts the fast charge CC mode cycle. In CC mode, the charger regulates the charging current to its maximum level. The maximum charging current (I_{MAX}) is determined by the external sense resistor, R_{SENSE}, and the voltage, V_{SENSE}. V_{SENSE}, is programmable through the I^2C interface (refer to CSV register for programming information). The range of V_{SENSE} is from 100 mV to 200 mV, in 20-mV steps. The CC mode charge time is limited by the CCTR timer.

$$I_{MAX} = \frac{V_{SENSE}}{R_{SENSE}}$$

fast charge constant current (CV mode)

When the cell reaches the constant voltage phase, the charger switches to the fast charge CV mode. The charging current begins tapering down while the charging voltage is regulated at the programmed voltage level (4.1 V or 4.2 V). The CV mode charging is limited by the TCTR timer.

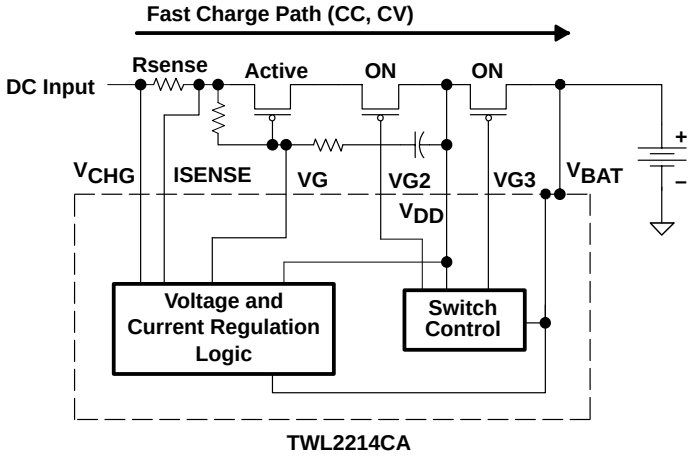


Figure 20. Fast Charge Functional Diagram

APPLICATION INFORMATION

current termination

During the CV mode, the charge cycle is terminated when the charging current is under the programmed terminated level or when the total charge timer (TCTR) times out. The terminated current level can be programmed to 10%, 20%, 30%, 40%, or 50% of the charging current at CC mode.

temperature monitoring

The TWL2214CA device monitors the battery temperature throughout the charge cycle. The input for ADC reference voltage is generated by a negative temperature coefficient (NTC) thermistor. The TWL2214CA device compares the ADC input reference voltage to the programmed threshold voltages to determine if charging is allowed. Three required thresholds are:

- VBOTRH+ Voltage for over-temperature cutoff; charging is suspended.
- VBOTRH– Voltage to resume charging function for over-temperature cutoff.
- VBOTRL Voltage for low-temperature cutoff; charging is suspended.

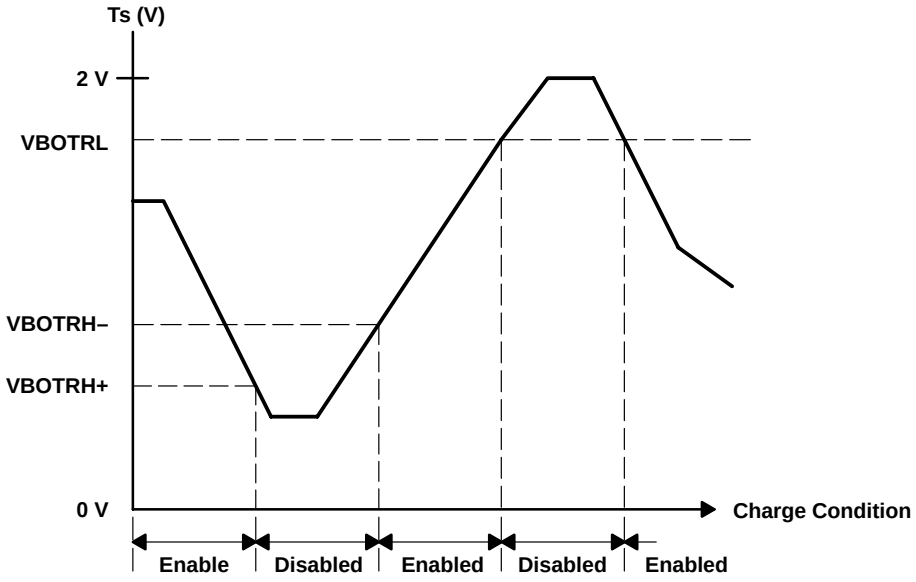


Figure 21. Temperature Monitoring

NOTE: The power-up default values are zero for these three thresholds. If the user opts not to use the temperature monitoring function during the charge cycle, the TS terminal of the device must be tied to GND to avoid an error signal.

APPLICATION INFORMATION

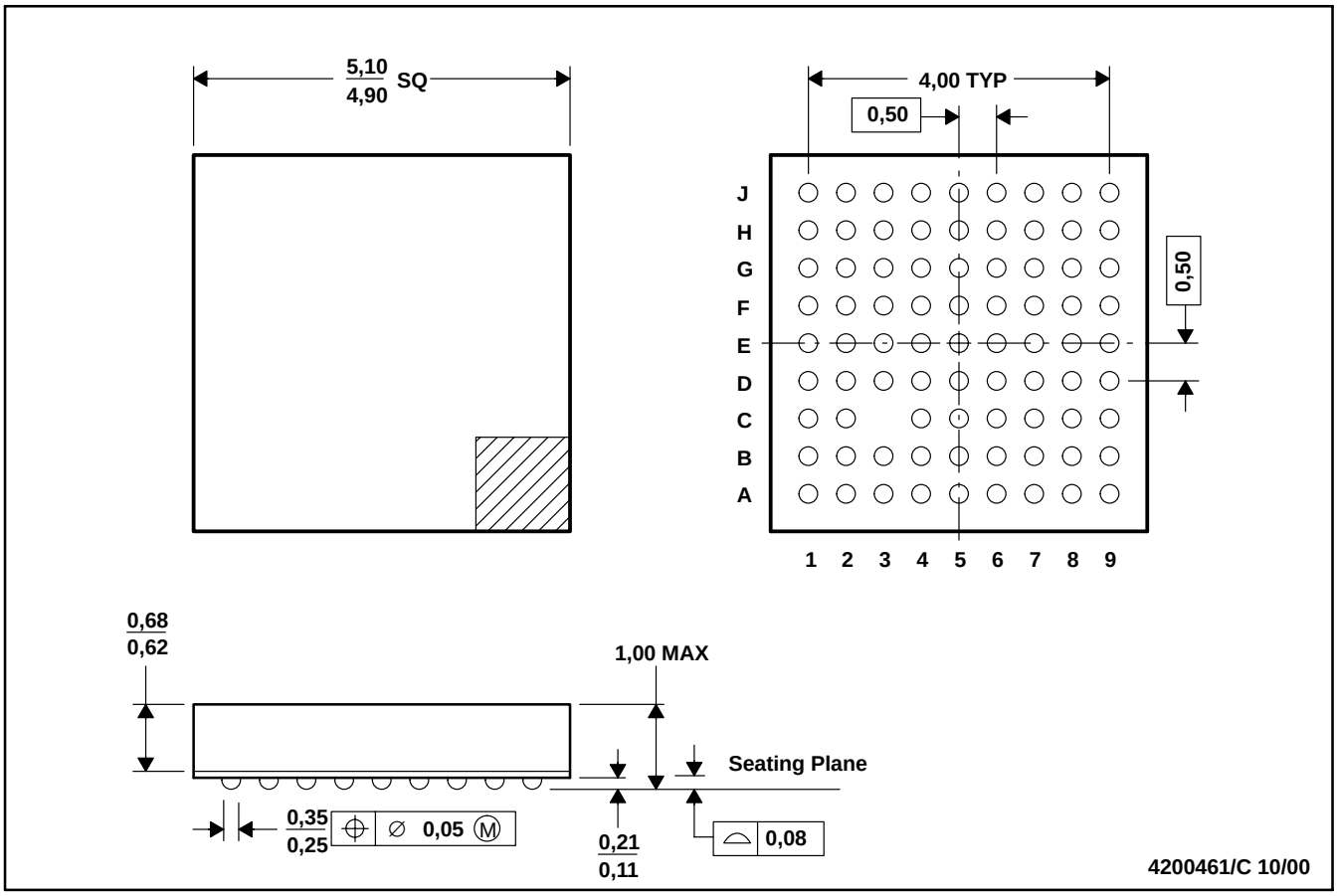
maximum time out

The TWL2214CA device provides three timers for maximal time allowed for charging. The time is programmable through I^2C interface.

TIMER DESCRIPTION	RANGE	STEP	COMMENT
PTR–Precharge timer	0–136 min	4 min	During the precharge cycle, if the timer expires before the precharging activity is complete, a BATT_ERR flag is set in the status register, and the charge is terminated.
CCTR–CC charge timer	0–274 min	8 min	During the CC mode cycle, if the timer expires before the CC activity is complete, a BATT_ERR flag is set in the status register, and the charge is terminated.
TCTR–total charge timer	0–15 hr	1 hr	Total charge time is defined as the total charge time of CC mode and CV mode. TCTR time-out occurs only in the CV mode. If the timer expires before, the charge is complete.

MECHANICAL DATA

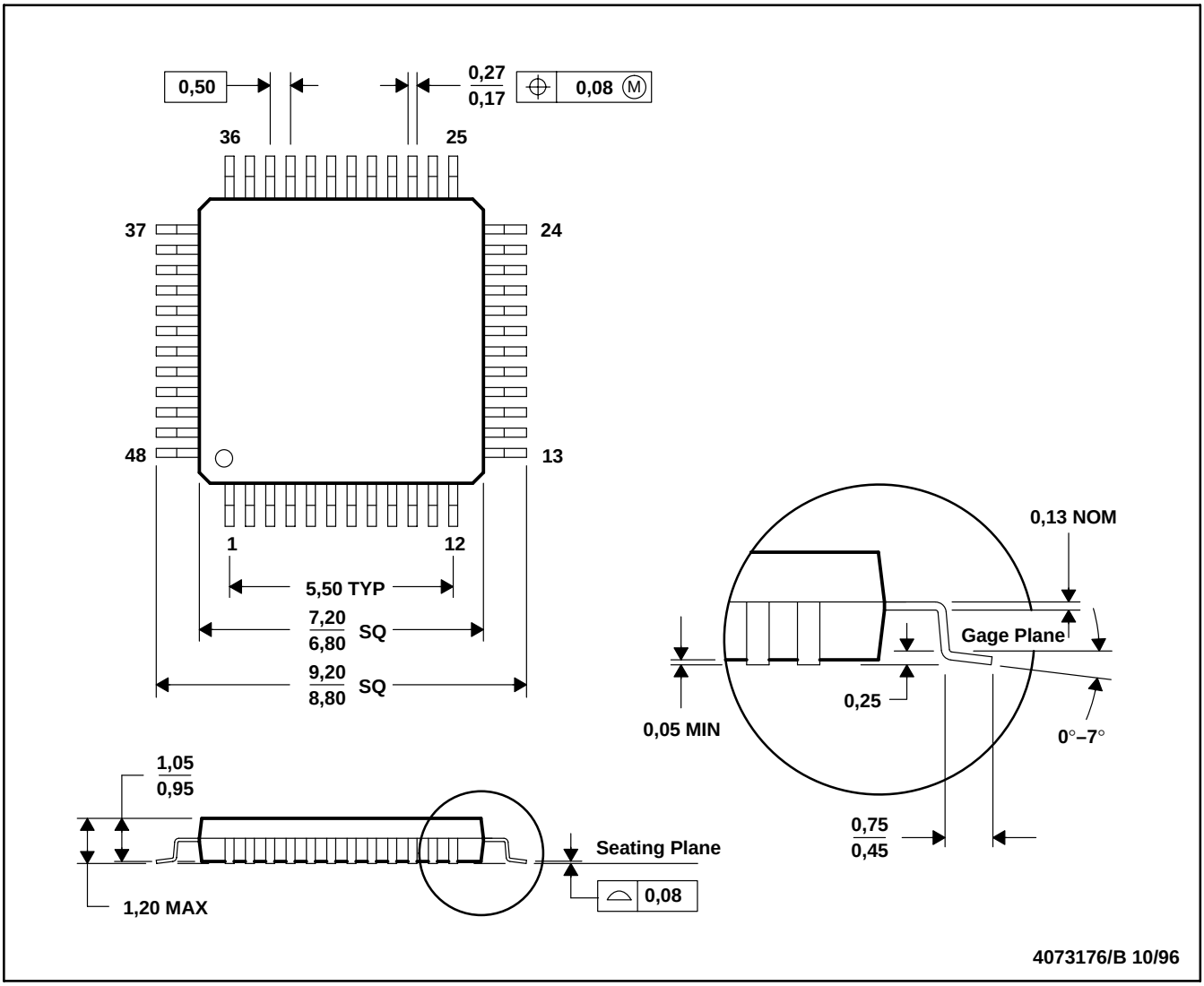
GQE (S-PBGA-N80) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

TWL2214CA, Power Supply Management IC and Li-Ion Battery Charge Control

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	TWL2214CA
Primary Battery Charger	Yes
Backup Battery Charger	No
Integrated LDO Regulators (#)	6
System Reset Controller	No
Real-Time Clock	Yes
Pin Count	48

FEATURES

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- Integrated, Single-Chip Solution for Battery Charge Control and Power Supply Management
- Linear Charger for Single-Cell Li-Ion or Li-Polymer Packs
- Integrated Control over Precharge, Constant-Current, and Constant-Voltage Charging Phases
- Programmable Charge Termination by Minimum Current and Time
- Battery Temperature Sensing
- Pack Wake-Up and Damaged Cell Detect Functions
- Safety Charge Timers During Precharge and Constant-Current Charging
- Programmable Charging Current
- Six Programmable Low-Dropout Linear Voltage Regulators
- Over 65-dB Power Supply Rejection Ratio (PSRR) From 10 Hz to 10 kHz
- System Over- and Under-Voltage Shutdown
- Power On/Off and Reset Control Logic
- Three Individually Selectable LED Backlight Drivers
- Vibrator and Ringer Drivers
- Internal 8-Bit Analog-to-Digital Converter With Auxiliary Inputs
- I^2C Control Interface and Three-Wire SPI Interface
- 48-Terminal Plastic TQFP (PFB) or MicroStar Junior BGA™ (GQR) Package

DESCRIPTION

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The TWL2214CA device is a single-chip battery and power management solution for wireless handsets, pagers, personal digital assistants (PDAs), and other battery-powered devices. For battery charging, the device incorporates a linear charger for single-cell Li-Ion and lithium polymer battery packs. Prior to charging, the TWL2214CA device initiates battery pack wake-up and damaged cell detect functions. For deeply discharged batteries, the device performs precharge conditioning by trickle charge to a user-defined current setting. Once an acceptable pack voltage is detected, the TWL2214CA device applies a constant-current fast charge at a current level that is determined by the combination of an external sense resistor and user-programmable sense voltage. When the battery reaches the selected charge regulation voltage, the TWL2214CA device maintains regulation until charging is terminated by a minimum current or a timer. During the entire charge cycle, the TWL2214CA device monitors temperature by external thermistor and suspends charging if temperature exceeds a programmed range. Three programmable safety timers limit the precharge, constant current, and total charge times.

For power management, the TWL2214CA device includes six low-dropout linear voltage regulators. One regulator is driven from the device power-on/-off logic and incorporates a microcontroller reset function. Five low-noise regulators include individually programmable output voltage and enable-disable. The TWL2214CA device can be powered from a battery or from an ac adapter. When

an adapter is present, it supplies power to the device, allowing the system to function without a battery.

The TWL2214CA device also includes individually selectable drivers for three separate backlight LEDs, a ringer, and a vibrator motor. An internal 8-bit analog-to-digital converter (ADC) is accessible from external terminals. All TWL2214CA programming and status are accessed by the system microcontroller via the I^2C/SPI serial interface.

The TWL2214CA device is packaged in the Texas Instruments 48-terminal plastic thin quad flatpack (TQFP) (PFB) or the MicroStar Junior BGA™ (GQE) package.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: twl2214ca.pdf (511 KB,Rev.A) (Updated: 01/14/2002)

RELATED DOCUMENTS

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- Enhanced Plastic Portfolio Brochure (SGZB004, 385 KB - Updated: 08/19/2002)
- Military Analog Selection Guide (SGLB002, 318 KB - Updated: 11/09/2000)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

BLOCK DIAGRAMS

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- Digital Cellphone
- GSM Handset System (Generic)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
TWL2214CAPFB	TQFP (PFB)	48	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION

ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
TWL2214CAPFB	ACTIVE	TQFP (PFB) | 48	-40 TO 85	View Contents	1KU | 4.15	2500
TWL2214CAPFBR	ACTIVE	TQFP (PFB) | 48	-40 TO 85	View Contents	1KU | 4.18	1000

TI INVENTORY STATUS AS OF 4:00 PM GMT, 26 Sep 2002

IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME
N/A*	234 | 23 Sep	12 WKS
	>10k | 16 Dec	
	>10k | 23 Dec	
	>10k | 30 Dec	
	>10k | 06 Jan	
1000	>10k | 16 Dec	1 WKS
	>10k | 23 Dec	

REPORTED DISTRIBUTOR INVENTORY AS OF 4:00 PM GMT, 26 Sep 2002

DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE

								>10k | 30 Dec						
								>10k | 06 Jan						
								>10k | 13 Jan						

Table Data Updated on: 9/26/2002