EMB1432Q 60-V, 14-Channel Battery Stack Module Analog Front End

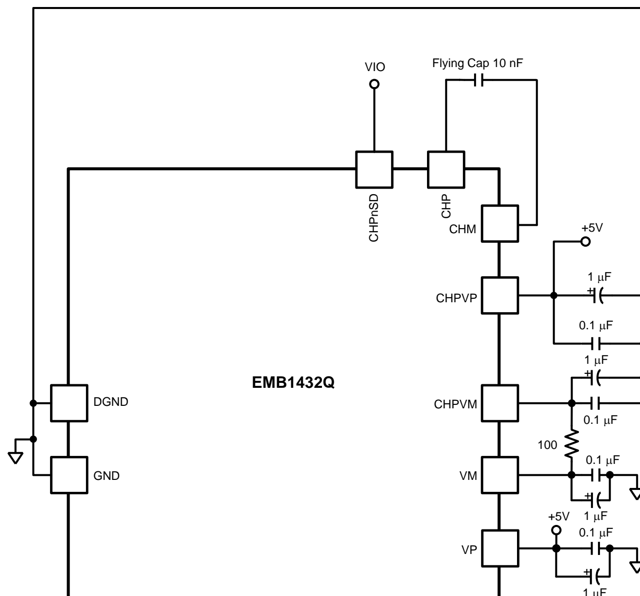
1 Features

- Positive Supply Voltage 4.75 V to 5.5 V
- Negative Supply Voltage −5.5 V to −4 V
- Positive Supply Current 750 μA (max)
- $V_{BATT} = (V_{SENSE(N)} - V_{SENSE(N-1)})$ 0.5 V to 4.6 V
- $V_{SENSE(14)}$ 60 V (max)
- Input Sense Current 6 μA (max)
- Input Referred Offset Voltage ±1 mV (Max)
- Digital Interface Supply 2.7 V to 5.5 V
- Gain 1
- Gain Error 0.05% (max)
- Ambient Operating Temperature −40°C to 125°C
- AEC Q100 Grade 1

2 Applications

- Li-Ion Battery Management Systems
- Hybrid and Electric Vehicles
- Grid Storage
- 48 V Systems
- UPS

Typical Application



3 Description

The EMB1432Q Battery Stack Module Analog Front End is a high voltage analog interface designed to monitor a lithium battery stack. It is able to select and level shift the voltage across any of 14 stacked batteries and 2 low voltage auxiliary inputs, multiplexing the signals to an output pin. The multiplexer output is set by writing to an internal register using the SPI™ protocol or by directly addressing 4 digital pins. The voltage across each battery can range from –2 V to 5.5 V without damaging the AFE, with the top cell positive pin reaching 60 V. The SENSE(N) input impedance (when the Nth battery is selected) is 1 MΩ typ, and the current drawn from SENSE(N-1) is 2 μA typ. When not selected or in shutdown mode, the current at any sense input drops to less than 1 μA.

The EMB1432Q can precisely level shift a battery voltage ranging from 0.5 V to 4.6 V with a gain of 1, an input referred offset voltage of ±1 mV and a gain error of 0.05% (max). The EMB1432Q operates with 5 V and –5 V supplies. Single supply operation is also supported: the –5 V supply can be internally generated using an internal charge pump. The I/O communication interface can be supplied through dedicated supply pins (VIO, DGND). The EMB1432Q is designed to provide accurate analog output over the AEC-Q100 type 2 temperature range of –40°C to 105°C and to be able to operate up to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
EMB1432Q	WQFN (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D — **Page**

- Added AEC Q100 Grade 1 1
- Added new Applications on page 1; *Device Information*, *Handling Ratings* and *Thermal Information* tables, *Power Supply Recommendations*, *Layout*, and *Device and Documentation Support* and *Mechanical, Packaging, and Orderable Information* sections; reformatted *Detailed Description* and *Application and Implementation* sections; added "Q" to part number. 1
- Changed paddle to pad 4

Changes from Revision B (April 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format 13

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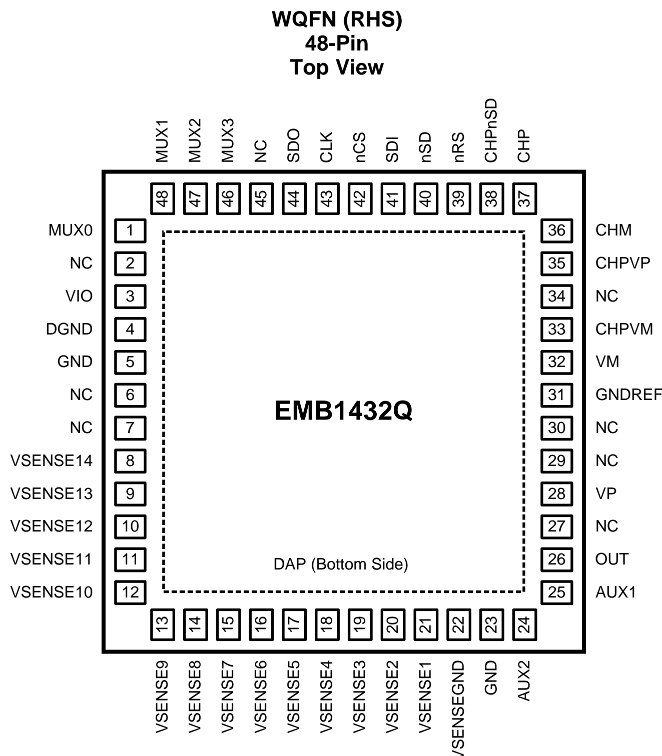
5 Pin Configuration and Functions

WQFN (RHS)
48-Pin
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
MUX0	1	Multiplexer direct addressing bit 0.
NC	2	No Connection.
VIO	3	Digital Positive Supply.
DGND	4	Digital Ground.
GND	5	Analog ground. Internally shorted to pin 23.
NC	6	No Connection.
NC	7	No Connection.
VSENSE14	8	Channel 14. To be connected to the positive rail of the 14th battery.
VSENSE13	9	Channel 13. To be connected to the negative rail of the 14th battery and to the positive rail of the 13th battery.
VSENSE12	10	Channel 12. To be connected to the negative rail of the 13th battery and to the positive rail of the 12th battery.
VSENSE11	11	Channel 11. To be connected to the negative rail of the 12th battery and to the positive rail of the 11th battery.
VSENSE10	12	Channel 10. To be connected to the negative rail of the 11th battery and to the positive rail of the 10th battery.
VSENSE9	13	Channel 9. To be connected to the negative rail of the 10th battery and to the positive rail of the 9th battery.
VSENSE8	14	Channel 8. To be connected to the negative rail of the 9th battery and to the positive rail of the 8th battery.
VSENSE7	15	Channel 7. To be connected to the negative rail of the 8th battery and to the positive rail of the 7th battery.
VSENSE6	16	Channel 6. To be connected to the negative rail of the 7th battery and to the positive rail of the 6th battery.

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
VSENSE5	17	Channel 5. To be connected to the negative rail of the 6th battery and to the positive rail of the 5th battery.
VSENSE4	18	Channel 4. To be connected to the negative rail of the 5th battery and to the positive rail of the 4th battery.
VSENSE3	19	Channel 3. To be connected to the negative rail of the 4th battery and to the positive rail of the 3rd battery.
VSENSE2	20	Channel 2. To be connected to the negative rail of the 3rd battery and to the positive rail of the 2nd battery.
VSENSE1	21	Channel 1. To be connected to the negative rail of the 2nd battery and to the positive rail of the 1st battery.
VSENSEGND	22	Channel 0. To be connected to the negative rail of the 1st battery.
GND	23	Analog Ground. Internally shorted to pin 5.
AUX2	24	Auxiliary analog input 2, unbuffered input.
AUX1	25	Auxiliary analog input 1, unbuffered input.
OUT	26	Analog Output.
NC	27	No Connection.
VP	28	+5 V positive supply. Attach a 0.1 µF bypass capacitor between VP and GND, as close as possible to the pins.
NC	29	No Connection.
NC	30	No Connection.
GNDREF	31	Reference ground for the AFE analog output.
VM	32	–5 V negative voltage supply. Attach a 0.1 µF bypass capacitor between VM and GND, as close as possible to the pins. If internal charge pump is set on, connect VM to CHPVM.
CHPVM	33	–5 V charge pump generated voltage supply. If using internal charge pump attach a 0.1 µF to 1µF reservoir capacitor between CHPVM and DGND and connect to CHPVM to VM.
NC	34	No Connection.
CHPVP	35	Charge pump positive supply. Attach a 0.1µF bypass capacitor between CHPVP and GND, as close as possible to the pins. Connect to VP on the board if using the internal charge pump.
CHM	36	Connect to negative pin of the charge pump flying capacitor (10nF).
CHP	37	Connect to positive pin of the charge pump fly capacitor (10nF).
CHPnSD	38	Charge pump shutdown, active low. Connect to VIO to turn on charge pump, connect to GND to shutdown charge pump.
nRS	39	AFE SPI register reset, active low. Connect to VIO for normal use, connect to GND to reset register.
nSD	40	AFE shut down, active low. Connect to VIO for normal use, connect to GND to shutdown AFE.
SDI	41	AFE SPI Serial Data In.
nCS	42	AFE SPI Chip Select, active low.
CLK	43	AFE SPI Clock.
SDO	44	AFE SPI Serial Data Out. In Tri-state when nCS is high.
NC	45	No Connection.
MUX3	46	Multiplexer direct addressing bit 3.
MUX2	47	Multiplexer direct addressing bit 2.
MUX1	48	Multiplexer direct addressing bit 1.
DAP	Thermal Pad	Die Attach Pad, connect to GND.

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6 Specifications

6.1 Absolute Maximum Ratings[1][2][3]

		MIN	TYP	MAX	UNIT
VP, VIO, CHPVP	Positive supply voltage			6	V
VM	Negative supply voltage			–6	V
CHM	Charge Pump negative pin			–6	V
CHP	Charge Pump positive pin			6	V
(VSENSE(N)-VSENSE(N-1))	Differential input voltage across battery cell	−2		5.5	V
AUX1, AUX2	Auxiliary inputs			6	V
CHPnSD, nRS, nSD, MUX0, MUX1, MUX2, MUX3, SDI, nCS, CLK, SDO	Digital inputs	−0.3		VIO+0.3	V
VSENSE 14				70	V
Junction temperature[4]				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability for specifications.
(3) For soldering specifications: see SNOA549.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 Handling Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		2000	V
		Machine Model		200	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VP, CHPVP	Analog positive supply voltage	4.75		5.5	V
VIO	Digital positive supply voltage	2.7		5.5	V
VM	Analog negative supply voltage	–5.5		–4.0	V
	Operating temperature range	--40		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.4 Thermal Information

THERMAL METRIC[1]		EMB1432Q WQFN (RHS) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	24.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

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6.5 Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for T_A = 25°C, VP, = VIO = CHPVP = nRS = nSD = 5 V, GND = CHPnSD = 0 V, VM = −5 V, 0.5 V < V_{BATT} < 4.6 V, V_{BATT} = $V_{SENSE(N)}$ − $V_{SENSE(N−1)}$.

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[3]	MAX[2]	UNIT
V_{OS}	Input offset voltage[4]	T_A = 25°C, 1 V < V_{BATT} < 4 V[5]		−1		1	mV
		T_A = 0°C to 65°C, 1 V < V_{BATT} < 4 V[5]		−1.5		1.5	
		T_A = −40°C to 105°C, 1V < V_{BATT} < 4 V[5]		−2		2	
		T_A = −40°C to 125°C, 1 V < V_{BATT} < 4 V		−2.5[6]		2.5[6]	
$V_{OSDRIFT}$	Long-term offset drift	500 hours OPL[5]			±0.25		mV
R_{SENSE}	Sense input resistance	SENSE(N), Nth channel selected, V_{BATT} = 4 V, FB = 0		0.92 [6]	1.06	1.20 [6]	MΩ
I_{SENSE}	Sense input current	Nth channel selected, V_{BATT} = 4 V	SENSE(N−1)[7]		2	6[6]	µA
			All other sense pins except SENSE(N) when nSD = 5 V,		0.004	0.5[6]	
			all sense pins when nSD = 0 V.[7]		0.004	4[6]	
I_{VP}	Positive supply current	Measurement mode, nSD = VIO, V_{BATT} = 4 V			0.46	0.75 [6]	mA
		Shutdown mode, nSD = 0 V			0.004	0.45[6]	µA
I_{VM}	Negative supply current	Measurement mode, nSD = VIO, V_{BATT} = 4 V			37	70 [6]	µA
		Shutdown mode, nSD = 0 V			0.002	0.25[6]	µA
I_{VIO}	VIO supply current	Measurement mode, nSD = VIO, V_{BATT} = 4 V			100	250[6]	µA
		Shutdown mode, nSD = 0 V			0.01	8[6]	µA
I_{CHPVP}	CHPVP supply current	Charge pump on, connected to VM (CHPnSD = VIO)			108	180[6]	µA
		Charge pump off (CHPnSD = 0 V)			3.3	8[6]	µA
IVR	Input voltage range	SENSE(N) − SENSE(N−1)[5]		0.5		VP − 0.4	V
	Input voltage range, auxiliary inputs	See [5]		0		VP	V
A_V	Gain	1 V < V_{BATT} < 4 V [5]			1		V/V
	Gain error	T_A = 25°C, 1 V < V_{BATT} < 4 V[5]				±0.05%	
		T_A = −40°C to 125°C, 1 V < V_{BATT} < 4 V				±0.1%[6]	
	Gain error drift	T_A = 0°C to 65°C, 1V < V_{BATT} < 4 V[5]				5	ppm/°C
BW	Bandwidth	C_L = 30 pF[5][8]			500		kHz
SR	Slew rate	C_L = 30 pF[5][8][9]			7		V/µs
C_{OUT}	Output capacitive load	See [5][8]			30		pF
+PSR	Positive power supply rejection	4.5 < VP < 5.5 V, f = 1 kHz[5][8]			70		dB
−PSR	Negative power supply rejection	−5.5 V < VM < −4.5 V, f = 1 kHz[5][8]			65		dB

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are verified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are verified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) Limits apply at the nominal temperature.
(6) Limits apply at the temperature extremes.
(7) Positive Bias Current corresponds to current flowing into the device.
(8) This parameter is verified by design and/or characterization and is not tested in production.
(9) The number specified is the slower of rising and falling slew rate and measured at 90% to 10%.

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Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, VP, = VIO = CHPVP = nRS = nSD = 5 V, GND = CHPnSD = 0 V, VM = −5 V, 0.5 V < V_{BATT} < 4.6 V, V_{BATT} = $V_{SENSE(N)}$ − $V_{SENSE(N−1)}$.

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
V_{OUT}	Output voltage range	V_{BATT} = 0.5 V	0.49[6]		0.51[6]	V
		V_{BATT} = 4.6 V	4.59[6]		4.61[6]	
R_{OUTAUX}	Output resistance when AUX1 or AUX2 are selected	See [5]		400		Ω
e_N	Input voltage noise	0.1 Hz to 10 Hz[5][8]		4		μV_{PP}
e_N	Input voltage noise density	f = 1 kHz [5]		825		nV/rtHz
t_{SETTLE}	1% settling time	Time from nCS rising edge to OUT voltage stable, V_{OUT} = 3.6 V		1.5	4[6]	µs
f_{CP}	Charge pump switching frequency	See [5][8]		380		kHz
V_{IL}	Input logic low threshold	See [5]			0.3 × VIO	V
V_{IH}	Input logic high threshold	See[5]	0.7 × VIO			V
V_{OL}	Output logic low threshold	I_{SDO} = 100 µA[5]			0.2	V
		I_{SDO} = 2 mA[5]			0.5	
V_{OH}	Output logic high threshold	I_{SDO} = 100 µA[5]	V_{IO} − 0.2			V
		I_{SDO} = 2 mA[5]	V_{IO} − 0.6			

6.6 Timing Requirements[1]

Unless otherwise specified, all limits ensured for T_A = 25°C, 2.7 V < VIO < 5.5 V.

See[2]		MIN[3]	NOM	MAX[3]	UNIT
t_1	High period, CLK,	100			ns
t_2	Low period, CLK	100			ns
t_3	Setup time, nCS to CLK	50			ns
t_4	Setup time, SDI to CLK	30			ns
t_5	Hold time, CLK to SDI	10			ns
t_6	Setup time, SDO to CLK	30			ns
t_7	Hold time, CLK to SDO	10			ns
t_8	Hold time, CLK transition to nCS rising edge	50			ns
t_9	nCS inactive	50			ns
t_{10}	Propagation delay, nCS to SDO active			50	ns
t_{11}	Hold time, CLK transition to nCS falling edge	10			ns
t_r/t_f	Signal rise and fall time, see[4]	1.5		5	ns

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Load for these tests is shown in Figure 1.
(3) Limits are verified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are verified through correlations using statistical quality control (SQC) method.
(4) This parameter is verified by design and/or characterization and is not tested in production.

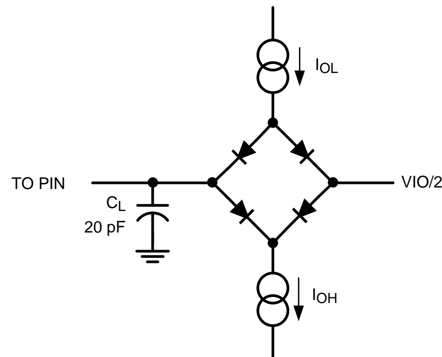
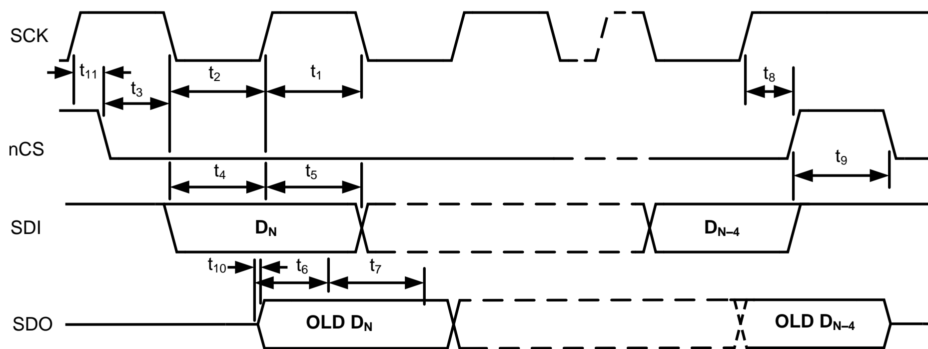


Figure 1. Test Circuit Diagram



Where:
D_N = B3, D_{N-1} = B2, D_{N-2} = B1, D_{N-3} = B0, D_{N-4} = FB

Figure 2. Timing Diagram

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6.7 Typical Characteristics

Unless otherwise specified, T_A = 25°C, VP = VIO = CHPVP = nRS = nSD = 5 V, GND = CHPnSD = 0 V, VM = −5 V, 0.5 V < V_{BATT} < 4.6 V, $V_{BATT} = V_{SENSE(N)} - V_{SENSE(N-1)}$, R_L = 1 MΩ, C_L = 30 pF.

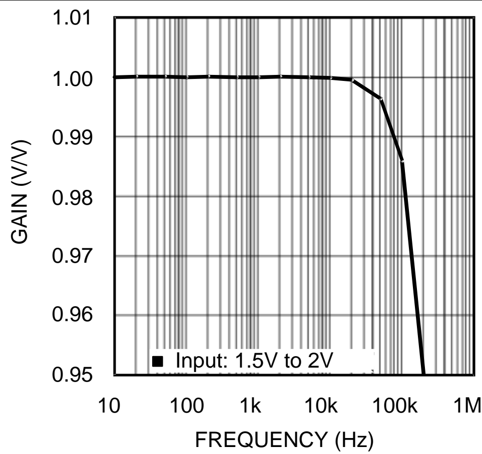

Figure 3. Small Signal Gain

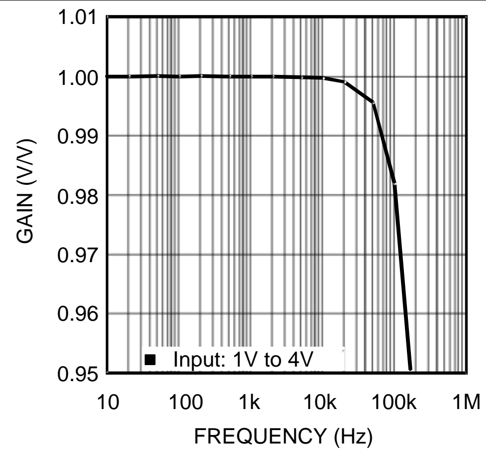

Figure 4. Large Signal Gain

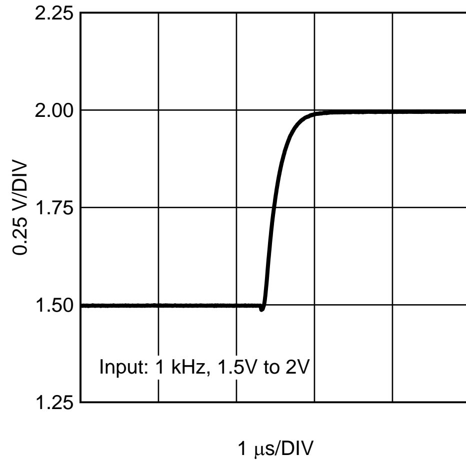

Figure 5. Small Signal Step Response

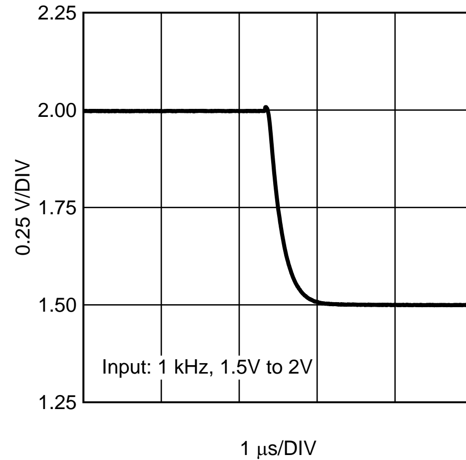

Figure 6. Small Signal Step Response

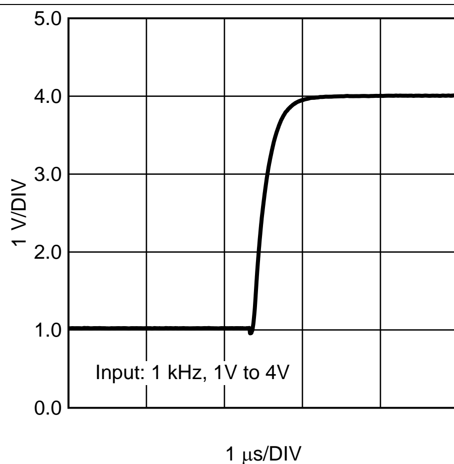

Figure 7. Large Signal Step Response

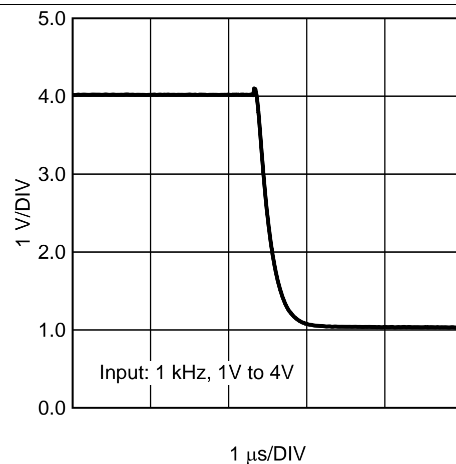

Figure 8. Large Signal Step Response

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, VP = VIO = CHPVP = nRS = nSD = 5 V, GND = CHPnSD = 0 V, VM = −5 V, 0.5 V < V_{BATT} < 4.6 V, V_{BATT} = $V_{SENSE(N)}$ − $V_{SENSE(N-1)}$, R_L = 1 MΩ, C_L = 30 pF.

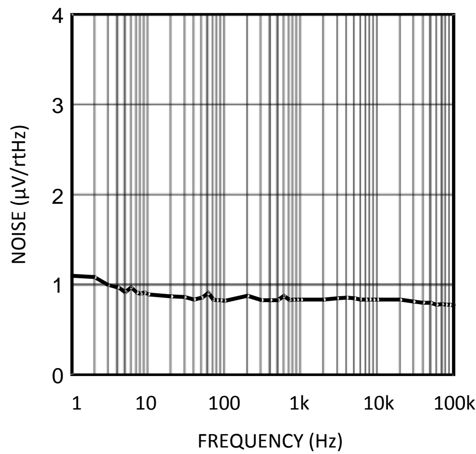

Figure 9. Voltage Noise vs. Frequency

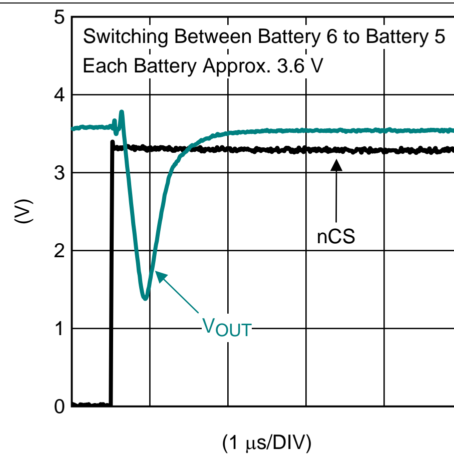

Figure 10. Switching Waveform

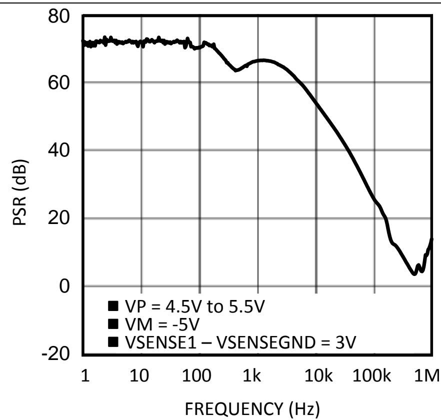

Figure 11. +PSR vs. Frequency

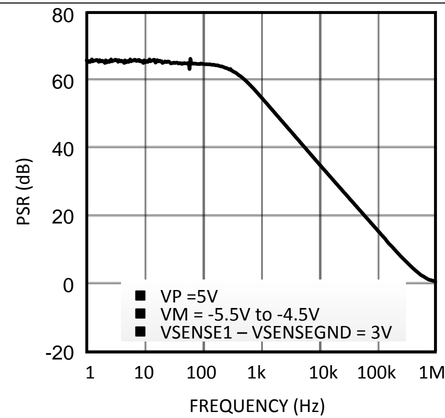

Figure 12. −PSR vs. Frequency

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7 Detailed Description

7.1 Functional Block Diagram

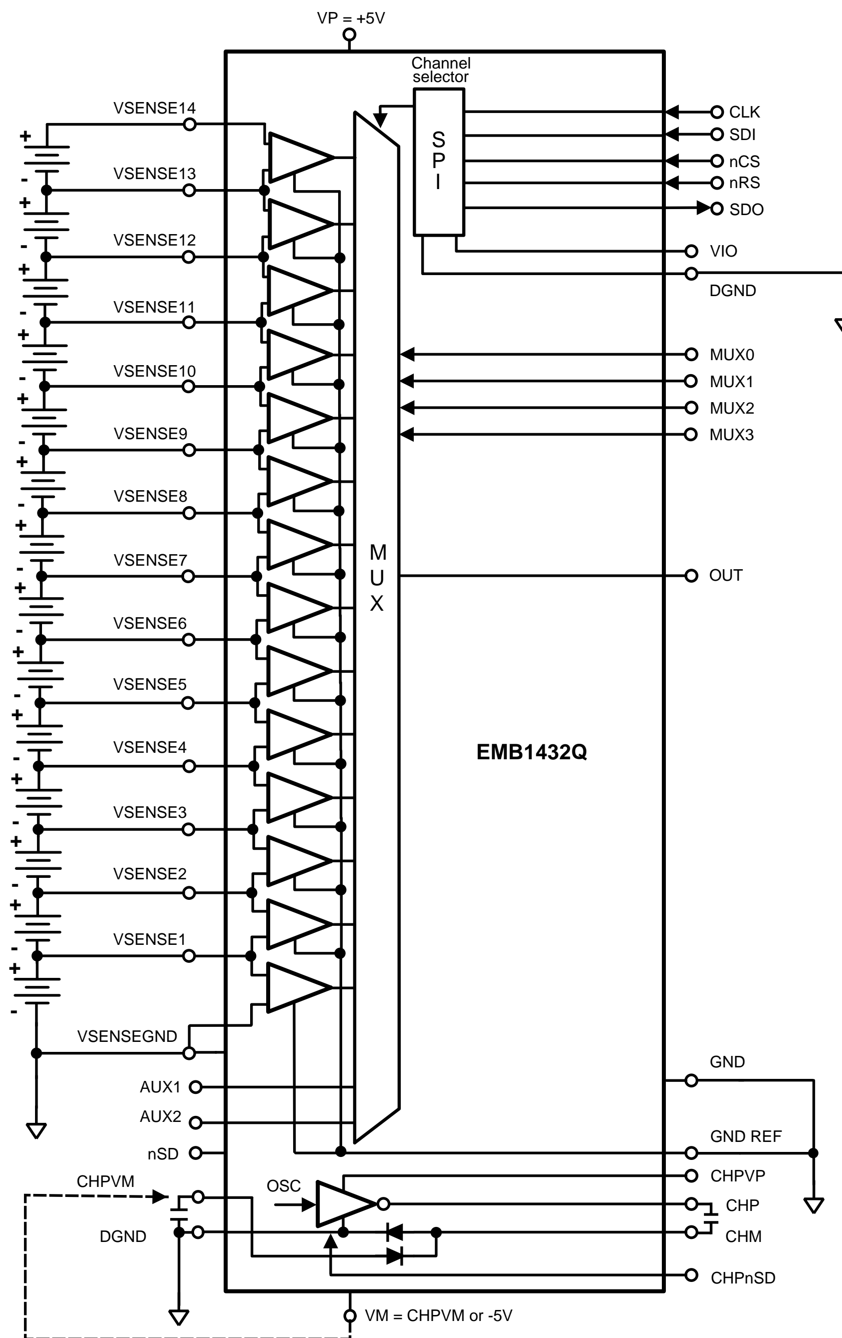

Figure 13. Battery Stack Monitor

7.2 Device Functional Modes

7.2.1 SPI Multiplexer Addressing Mode

To control the EMB1432Q using SPI connect the MUX0, MUX1, MUX2, and MUX3 pins to VIO.

The input source of the EMB1432Q is controlled by data stored in a programming register. Data to be written into the control register is first loaded into the AFE via the serial interface. The serial interface control employs the 5 bits of an internal shift register. Data is loaded through the serial data input, SDI. Data passing through the shift register are available through the serial data output, SDO. When the nCS is high the SDO is in tri-state. The serial clock, CLK controls the serial loading process. The first bit entering the register is the source address code MSB (B3). The last bit clocked in is the Force Current bit (FB).

At the 5th CLK falling edge, the first bit that was clocked in reappears at SDO. The falling edge of nCS which occurs while CLK is high will enable the shift register to receive data. Each data bit is clocked into the shift register on the rising edge of CLK. The rising edge of nCS loads the shift register content into the store register and the addressing process begins. The settling time between the rising edge of nCS and a stable output is approximately 2 µs. Operation is shown in Table 1.

Table 1. Register Organization

B3	B2	B1	B0	RESERVED
Address				Set to 0

Addresses from 0000b to 1101b will point to the battery stack, from the bottom battery at 0000b to the 14th battery at 1101b. Addresses 1110b to 1111b point to Auxiliary Input 1 and Auxiliary Input 2, which are the 2 additional analog inputs.

7.2.2 Direct Multiplexer Addressing Mode

For maximizing the multiplexing speed of the 14 battery inputs, the SPI digital interface can be bypassed using four dedicated bit lines (MUX[3:0]) for multiplexer addressing. If this mode is chosen, the selection of the source is made by setting these 4 bits with MUX3 as MSB and MUX0 as LSB. Refer to Table 2 for each source address. If this mode is not used, MUX0 to MUX3 pins must be tied to VIO to use SPI communication.

Note that Auxiliary Input 1 and Auxiliary Input 2 are not available in the Direct Multiplexer Addressing Mode. Also, the SPI pins are ignored in this mode.

Table 2. Source Selection

DIRECT MULTIPLEXER ADDRESSING MODE					SPI MULTIPLEXER ADDRESSING MODE				
Source	MUX3	MUX2	MUX1	MUX0	B3	B2	B1	B0	Source
Battery 1	0	0	0	0	0	0	0	0	Battery 1
Battery 2	0	0	0	1	0	0	0	1	Battery 2
Battery 3	0	0	1	0	0	0	1	0	Battery 3
Battery 4	0	0	1	1	0	0	1	1	Battery 4
Battery 5	0	1	0	0	0	1	0	0	Battery 5
Battery 6	0	1	0	1	0	1	0	1	Battery 6
Battery 7	0	1	1	0	0	1	1	0	Battery 7
Battery 8	0	1	1	1	0	1	1	1	Battery 8
Battery 9	1	0	0	0	1	0	0	0	Battery 9
Battery 10	1	0	0	1	1	0	0	1	Battery 10
Battery 11	1	0	1	0	1	0	1	0	Battery 11
Battery 12	1	0	1	1	1	0	1	1	Battery 12
Battery 13	1	1	0	0	1	1	0	0	Battery 13
Battery 14	1	1	0	1	1	1	0	1	Battery 14
AUX1	Not Selectable				1	1	1	0	AUX1
AUX2	Not Selectable				1	1	1	1	AUX2

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After the source address is programmed, the differential voltage appearing between Nth battery pins will be level shifted and presented at the output. If one of the two auxiliary inputs is selected, the voltage difference between this pin and GND is directly passed to the output pin. After a typical settling time of 2 µs the voltage at the output is valid. To ensure high precision in the measurement, the clock signal should be turned off after source selection.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Control Methods

The Multiplexer is a 16:1 single ended output. The selection of the source is made through either the MUX[3:0] digital input pins or, if MUX[3:0]=1111b, through the SPI digital interface as described in *SPI Multiplexer Addressing Mode* and *Direct Multiplexer Addressing Mode*.

8.2 Typical Applications

8.2.1 Double Supply Operation

Figure 14 shows the EMB1432Q set up for double supply operation. The VM and VP pins should each have a 0.1 µF capacitor connected as close as possible to the pin. Each pin should also have a capacitor of at least 1 µF connected to it. CHPnSD should be connected to ground.

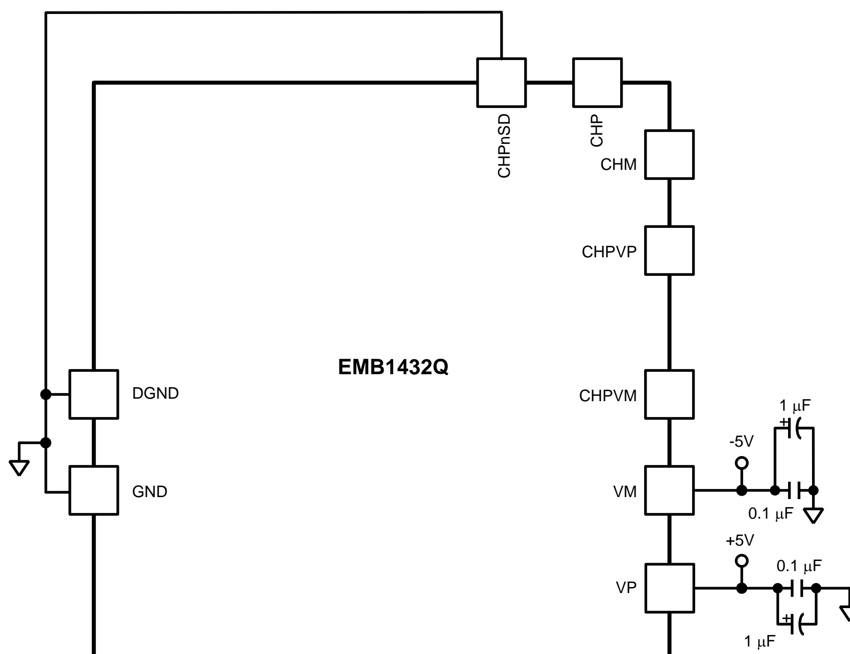

Figure 14. Schematic for Double Supply Operation

8.2.2 Detailed Design Procedure

The EMB1432Q is provided with an internal charge pump which supplies the correct negative voltage to VM. This enables the EMB1432Q to operate using only a single positive supply. This is done by doing the following:

1. Connect a 10nF flying capacitor between CHP and CHM.
2. Connect a ceramic capacitor of at least 1 µF between CHPVM and GND. It should be close to the CHPVM pin. A 0.1 µF capacitor can also be connected between CHPVM and GND for additional filtering of the charge pump switching noise.
3. Connect the negative supply pin VM to CHPVM. The 100 Ω resistor between CHPVM and VM is optional (it can be replaced by a short) but recommended to filter the charge pump switching noise.

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Typical Applications (continued)

4. To enable the internal charge pump, tie CHPnSD to VIO. If CHPnSD is connected to GND the internal charge pump is disabled.

8.2.3 Typical Application: Single Supply Operation

Figure 15 shows how to connect the external components to the EMB1432Q to use the charge pump. It is advisable to connect the bypass capacitors on CHPVP and the storage capacitor on CHPVM to the DGND pin.

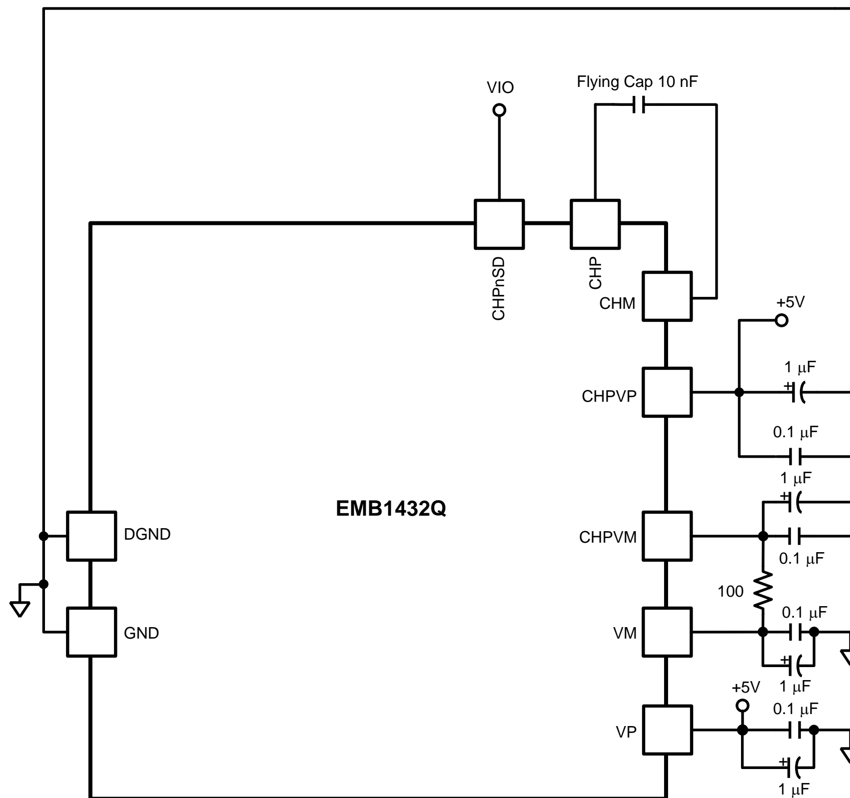

Figure 15. Schematic for Single Supply Operation

9 Device and Documentation Support

9.1 Trademarks

SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

9.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.3 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanica,l packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
EMB1432QSQ/NOPB	PREVIEW	WQFN	RHS	48		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	EMB1432Q	
EMB1432QSQE/NOPB	PREVIEW	WQFN	RHS	48		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	EMB1432Q	
EMB1432QSQX/NOPB	PREVIEW	WQFN	RHS	48		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	EMB1432Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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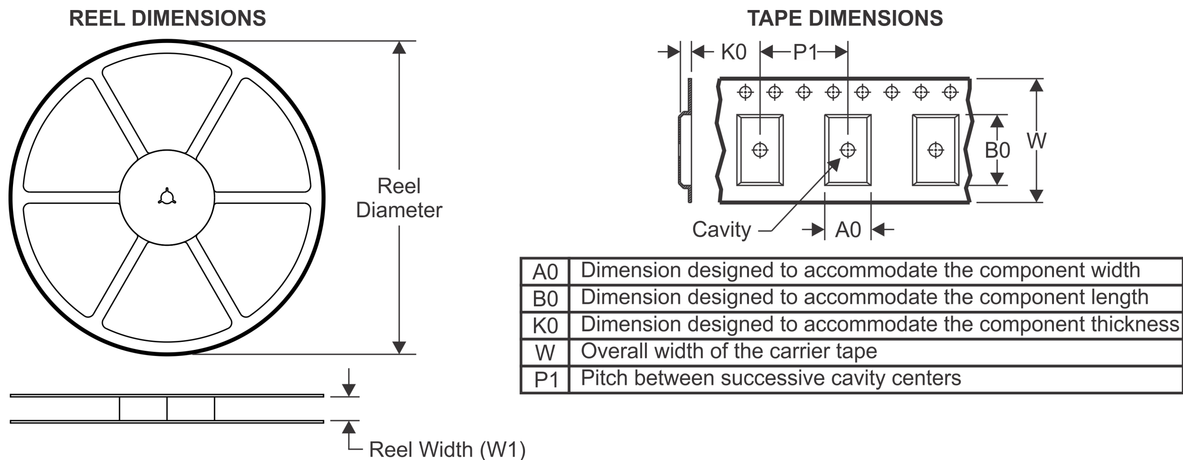
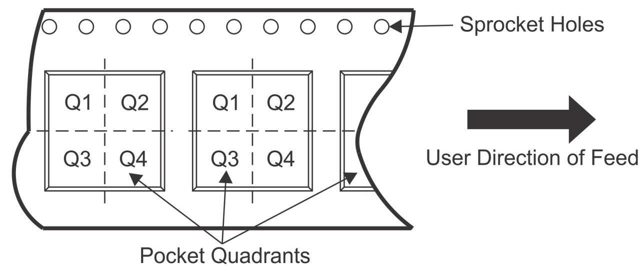
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

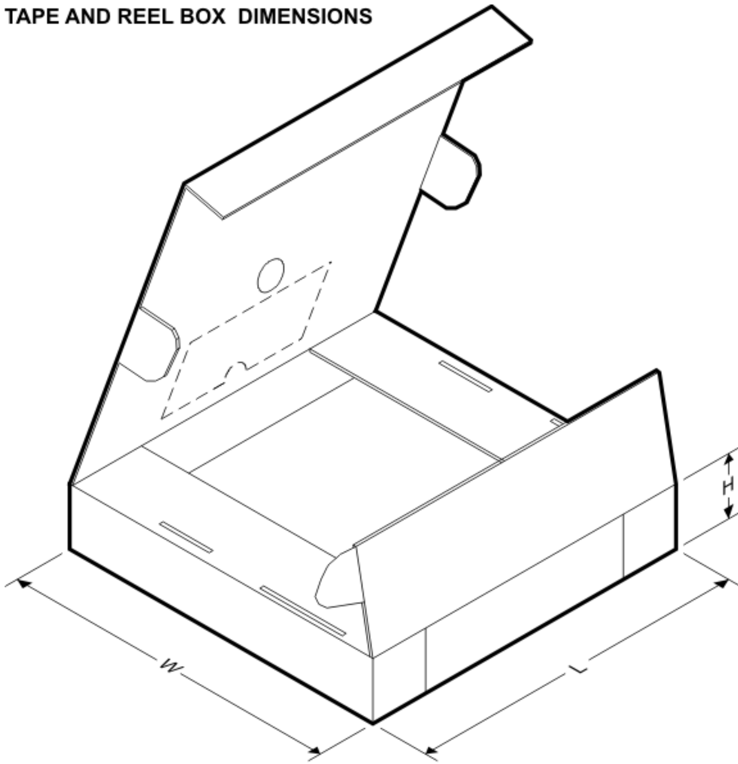
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
EMB1432QSQ/NOPB	WQFN	RHS	48	0	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
EMB1432QSQE/NOPB	WQFN	RHS	48	0	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
EMB1432QSQX/NOPB	WQFN	RHS	48	0	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

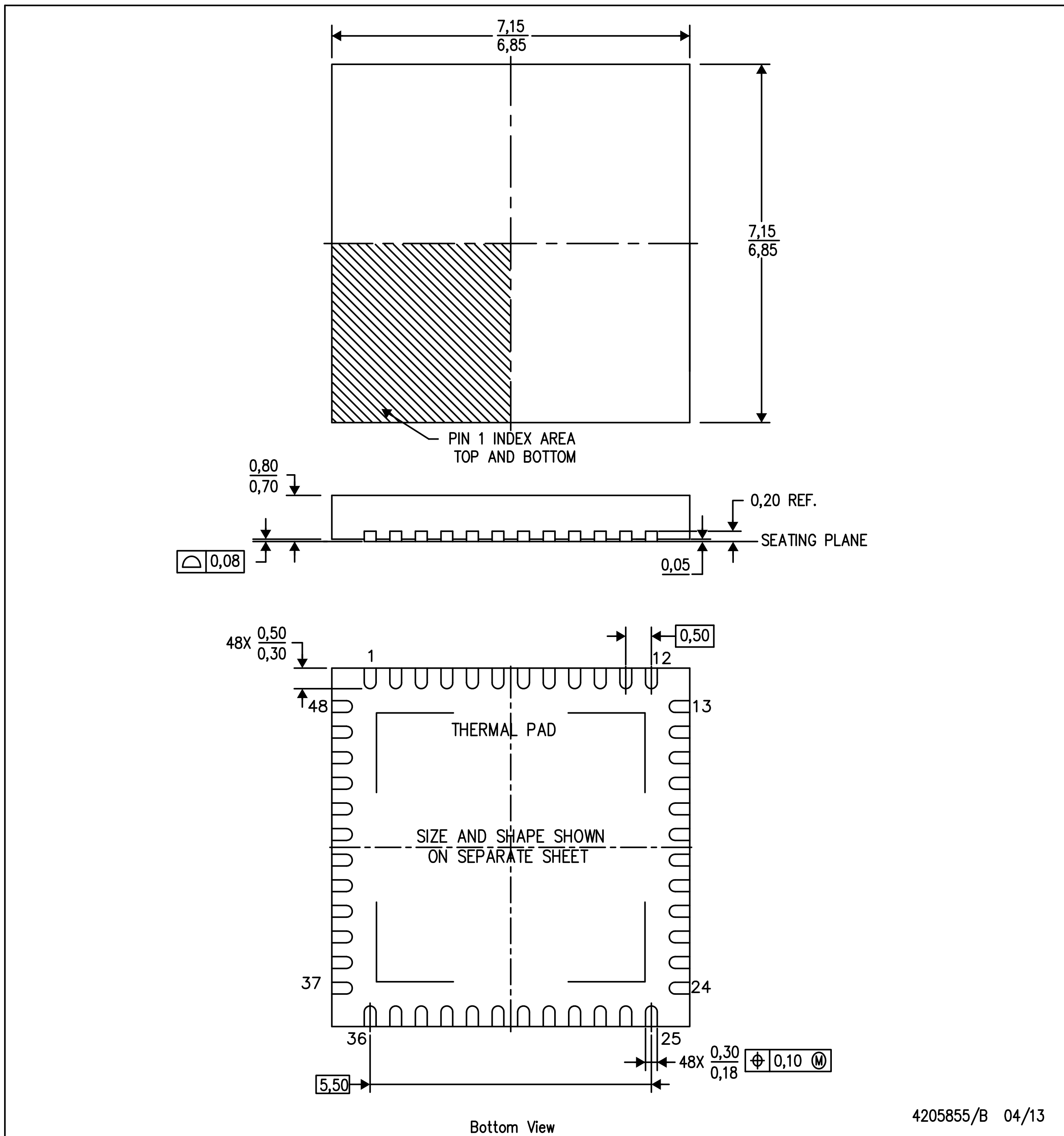
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
EMB1432QSQ/NOPB	WQFN	RHS	48	0	367.0	367.0	38.0
EMB1432QSQE/NOPB	WQFN	RHS	48	0	210.0	185.0	35.0
EMB1432QSQX/NOPB	WQFN	RHS	48	0	367.0	367.0	38.0

RHS (S-PWQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

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