National Semiconductor is now part of

Texas Instruments.

Search <u>http://www.ti.com/</u> for the latest technical

information and details on our current products and services.

100 MHz Single Channel M-LVDS Transceivers

General Description

The DS91C176 and DS91D176 are 100 MHz single channel M-LVDS (Multipoint Low Voltage Differential Signaling) transceivers designed for applications that utilize multipoint networks (e.g. clock distribution in ATCA and uTCA based systems). M-LVDS is a new bus interface standard (TIA/ EIA-899) optimized for multidrop networks. Controlled edge rates, tight input receiver thresholds and increased drive strength are sone of the key enhancments that make M-LVDS devices an ideal choice for distributing signals via multipoint networks.

The DS91C176/DS91D176 are half-duplex transceivers that accept LVTTL/LVCMOS signals at the driver inputs and convert them to differential M-LVDS signals. The receiver inputs accept low voltage differential signals (LVDS, B-LVDS, M-LVDS, LV-PECL and CML) and convert them to 3V LVCMOS

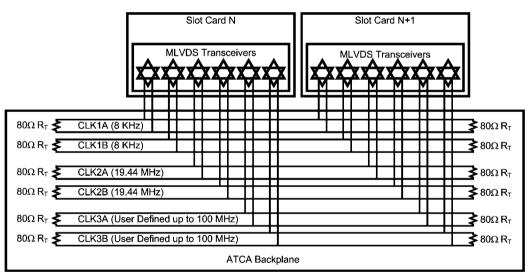
signals. The DS91D176 has a M-LVDS type 1 receiver input with no offset. The DS91C176 has an M-LVDS type 2 receiver which enable failsafe functionality.

November 9, 2009

Features

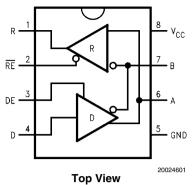
- DC to 100+ MHz / 200+ Mbps low power, low EMI operation
- Optimal for ATCA, uTCA clock distribution networks
- Meets or exceeds TIA/EIA-899 M-LVDS Standard
- Wide Input Common Mode Voltage for Increased Noise Immunity
- DS91D176 has type 1 receiver input
- DS91C176 has type 2 receiver with fail-safe
- Industrial temperature range
- Space saving SOIC-8 package

Typical Application in an ATCA Clock Distribution Network





Connection and Logic Diagram



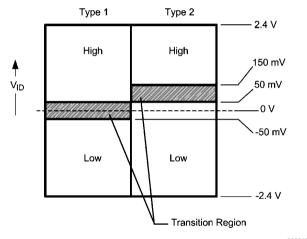
Top View Order Number DS91D176TMA, DS91C176TMA See NS Package Number M08A

Ordering Information

| Order Number | Receiver Input | Function | Package Type |
|--------------|----------------|--|--------------|
| DS91D176TMA | type 1 | Data (0V threshold receiver) | SOIC/M08A |
| DS91C176TMA | type 2 | Control (100 mV offset fail-safe receiver) | SOIC/M08A |

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater than $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.



20024640

FIGURE 1. M-LVDS Receiver Input Thresholds

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| Supply Voltage, V _{CC} –0.3V to +4 | | | |
|--|-----------------------------------|--|--|
| Control Input Voltages -0.3V to (V _{CC} + 0 | | | |
| Driver Input Voltage $-0.3V$ to $(V_{CC} + 0.3)$ | | | |
| Driver Output Voltages | -1.8V to +4.1V | | |
| Receiver Input Voltages -1.8V to +4 | | | |
| Receiver Output Voltage | -0.3V to (V _{CC} + 0.3V) | | |
| Maximum Package Power Dissipation at +25°C | | | |
| SOIC Package | 833 mW | | |
| Derate SOIC Package 6.67 mW/°C above +2 | | | |
| Thermal Resistance (4-Layer, 2 c | oz. Cu, JEDEC) | | |
| θ_{JA} | 150°C/W | | |
| θ _{JC} | 63°C/W | | |
| Maximum Junction Temperature | 150°C | | |
| Storage Temperature Range | -65°C to +150°C | | |

| Lead Temperature | |
|------------------------|----------|
| (Soldering, 4 seconds) | 260°C |
| ESD Ratings: | |
| (HBM 1.5kΩ, 100pF) | ≥ 8 kV |
| (EIAJ 0Ω, 200pF) | ≥ 250 V |
| (CDM 0Ω, 0pF) | ≥ 1000 V |

Recommended Operating Conditions

| | Min | Тур | Мах | Units |
|--|------|-----|----------|-------|
| Supply Voltage, V _{CC} | 3.0 | 3.3 | 3.6 | V |
| Voltage at Any Bus Terminal | -1.4 | | +3.8 | V |
| (Separate or Common-Mode) | | | | |
| Differential Input Voltage V _{ID} | | | 2.4 | V |
| LVTTL Input Voltage High V _{IH} | 2.0 | | V_{CC} | V |
| LVTTL Input Voltage Low V _{IL} | 0 | | 0.8 | V |
| Operating Free Air | | | | |
| Temperature T _A | -40 | +25 | +85 | °C |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2, Note 3, Note 4, Note 8)

| Symbol | Parameter | Conditions | | Min | Тур | Max | Units |
|----------------------|--|--|--------|--------------------|------|--------------------|-------|
| M-LVDS D | river | | | | | | |
| IV _{AB} I | Differential output voltage magnitude | $R_L = 50\Omega, C_L = 5pF$ | | 480 | | 650 | mV |
| ΔV_{AB} | Change in differential output voltage magnitude between logic states | Figure 2 and Figure 4 | | -50 | 0 | +50 | mV |
| V _{OS(SS)} | Steady-state common-mode output voltage | R _L = 50Ω, C _L = 5pF | | 0.3 | 1.8 | 2.1 | V |
| ΔV _{OS(SS)} | Change in steady-state common-mode output voltage between logic states | Figure 2 and Figure 3 | | 0 | | +50 | mV |
| V _{OS(PP)} | Peak-to-peak common-mode output voltage | (V _{OS(PP)} @ 500KHz clock |) | | 135 | | mV |
| V _{A(OC)} | Maximum steady-state open-circuit output voltage | Figure 5 | | 0 | | 2.4 | V |
| V _{B(OC)} | Maximum steady-state open-circuit output voltage | | | 0 | | 2.4 | V |
| V _{P(H)} | Voltage overshoot, low-to-high level output | $R_{L} = 50\Omega, C_{L} = 5pF, C_{D} = 0.5pF$ | | | | 1.2V _{SS} | V |
| V _{P(L)} | Voltage overshoot, high-to-low level output | Figure 7 and Figure 8 (Note 9) | | –0.2V _S | | | v |
| I _{IH} | High-level input current (LVTTL inputs) | V _{IH} = 2.0V | | -15 | | 15 | μA |
| I _{IL} | Low-level input current (LVTTL inputs) | V _{IL} = 0.8V | | -15 | | 15 | μΑ |
| V _{IKL} | Input Clamp Voltage (LVTTL inputs) | I _{IN} = -18mA | | -1.5 | | | V |
| I _{os} | Differential short-circuit output current | Figure 6 | | -43 | | 43 | mA |
| M-LVDS R | eceiver | | | | | | |
| V _{IT+} | Positive-going differential input voltage threshold | See Function Tables | Type 1 | | 20 | 50 | mV |
| | | | Type 2 | | 94 | 150 | mV |
| V _{IT-} | Negative-going differential input voltage threshold | See Function Tables | Type 1 | -50 | 20 | | mV |
| | | | Type 2 | 50 | 94 | | mV |
| V _{OH} | High-level output voltage (LVTTL output) | I _{OH} = -8mA | | 2.4 | 2.7 | | V |
| V _{OL} | Low-level output voltage (LVTTL output) | I _{OL} = 8mA | | | 0.28 | 0.4 | V |
| I _{oz} | TRI-STATE output current | V _O = 0V or 3.6V | | -10 | | 10 | μA |
| I _{OSR} | Short-circuit receiver output current (LVTTL output) | i) V _O = 0V | | | -48 | -90 | mA |
| M-LVDS B | us (Input and Output) Pins | | | | | | |
| I _A | Transceiver input/output current | $V_A = 3.8V, V_B = 1.2V$ | | | | 32 | μA |
| | | $V_{A} = 0V \text{ or } 2.4V, V_{B} = 1.2$ | 2V | -20 | | +20 | μA |
| | | $V_A = -1.4V, V_B = 1.2V$ | | -32 | | | μA |

| $ \begin{array}{c} \mbox{V}_{B} = 3.8 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}_{B} = 0 \mbox{V or } 2.4 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}_{B} = -1.4 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}_{B} = -1.4 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}_{D} \\ \mbox{V}_{A} = \mbox{V}_{B}, -1.4 \mbox{V} \leq \mbox{V} \leq 3.8 \mbox{V}_{D} \\ \mbox{V}_{A} = 3.8 \mbox{V}, \mbox{V}_{B} = 1.2 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{A} = 0 \mbox{V or } 2.4 \mbox{V}, \mbox{V}_{B} = 1.2 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{A} = -1.4 \mbox{V}, \mbox{V}_{B} = 1.2 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{B} = 0 \mbox{V or } 2.4 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{B} = -1.4 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{B} = -1.4 \mbox{V}, \mbox{V}_{A} = 1.2 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{A} = \mbox{V}_{B}, -1.4 \mbox{V} \leq 3.8 \mbox{V}, \\ \mbox{DE} = \mbox{V}_{CC} \\ \mbox{OV} \leq \mbox{V}_{CC} \leq 1.5 \mbox{V}_{A} \\ \mbox{V}_{CC} = \mbox{OPEN} \\ \mbox{V}_{CC} = \mbox{OPEN} \\ \mbox{V}_{CC} = \mbox{OPEN} \\ \mbox{V}_{CC} = \mbox{OPEN} \\ \mbox{OPEN} \\ \mbox{V}_{CC} = \mbox{OPEN} \\ OP$ | -20 -32 -4 -20 -20 -32 -32 -32 -32 -32 -32 | | 32 +20 +4 32 +20 32 +20 +20 +4 | Αμ Αμ |
|--|--|------------------------------------|--|--|
| $\label{eq:second} \begin{array}{ c c c c } \hline V_{B} = -1.4V, V_{A} = 1.2V \\ \hline V_{A} = V_{B}, -1.4V \leq V \leq 3.8V \\ \hline V_{A} = 3.8V, V_{B} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = 0V \mbox{ or } 2.4V, V_{B} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = -1.4V, V_{B} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = 3.8V, V_{A} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = 0V \mbox{ or } 2.4V, V_{A} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = 0V \mbox{ or } 2.4V, V_{A} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = -1.4V, V_{A} = 1.2V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = V_{B}, -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ \hline 0V \leq V_{CC} \leq 1.5V \\ \hline \end{array}$ | -32 -4 -20 -20 -32 -32 -32 | | +4 32 +20 32 +20 | μΑ μΑ μΑ μΑ μΑ μΑ μΑ |
| $ \begin{array}{llllllllllllllllllllllllllllllllllll$ | -4 -20 -32 -32 -32 | | 32 +20 32 +20 | μΑ μΑ μΑ μΑ μΑ μΑ |
| $ \begin{array}{l} V_{A} = 3.8 V, V_{B} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{A} = 0V \text{ or } 2.4 V, V_{B} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{A} = -1.4 V, V_{B} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{B} = 3.8 V, V_{A} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{B} = 0V \text{ or } 2.4 V, V_{A} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{B} = -1.4 V, V_{A} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{A} = V_{B}, -1.4 V \leq V \leq 3.8 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \end{array} $ | -20 -32 -20 -20 -32 | | 32 +20 32 +20 | μΑ μΑ μΑ μΑ μΑ |
| $ \begin{array}{l} V_{A} = 3.8 V, V_{B} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{A} = 0V \text{ or } 2.4 V, V_{B} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{A} = -1.4 V, V_{B} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{B} = 3.8 V, V_{A} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{B} = 0V \text{ or } 2.4 V, V_{A} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{B} = -1.4 V, V_{A} = 1.2 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \hline V_{A} = V_{B}, -1.4 V \leq V \leq 3.8 V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5 V \\ \end{array} $ | -32 -20 -32 | | +20 32 +20 | μΑ μΑ μΑ μΑ |
| $\begin{array}{l} 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = 0V \mbox{ or } 2.4V, \ V_{B} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = -1.4V, \ V_{B} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = 3.8V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = 0V \mbox{ or } 2.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = V_{B}, \ -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \end{array}$ | -32 -20 -32 | | +20 32 +20 | μΑ μΑ μΑ μΑ |
| $ \begin{array}{l} V_{A} = 0V \text{ or } 2.4V, \ V_{B} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{A} = -1.4V, \ V_{B} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{B} = 3.8V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{B} = 0V \text{ or } 2.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{A} = V_{B}, -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \end{array} $ | -32 -20 -32 | | 32+20 | μΑ μΑ μΑ |
| $\begin{array}{l} DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \\ V_{A} = -1.4V, V_{B} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \\ \\ V_{B} = 3.8V, V_{A} = 1.2V, \\ DE = V_{CC} \\ \\ 0V \leq V_{CC} \leq 1.5V \\ \\ \\ \\ \\ V_{B} = 0V \text{ or } 2.4V, V_{A} = 1.2V, \\ \\ \\ \\ DE = V_{CC} \\ \\ \\ 0V \leq V_{CC} \leq 1.5V \\ \\ \\ \\ \\ \\ \\ V_{B} = -1.4V, V_{A} = 1.2V, \\ \\ \\ \\ \\ \\ \\ \\ DE = V_{CC} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$ | -32 -20 -32 | | 32+20 | μΑ μΑ μΑ |
| $\begin{array}{l} 0V \leq V_{CC} \leq 1.5V \\ \hline V_A = -1.4V, V_B = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_B = 3.8V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_B = 0V \ or \ 2.4V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_B = -1.4V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_B = -1.4V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_A = V_B, -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \end{array}$ | -32 -20 -32 | | 32+20 | μΑ μΑ μΑ |
| $\begin{split} & V_{A} = -1.4V, V_{B} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{B} = 3.8V, V_{A} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{B} = 0V \text{ or } 2.4V, V_{A} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{B} = -1.4V, V_{A} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{A} = V_{B}, -1.4V \leq V \leq 3.8V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ \end{split}$ | -20 | | +20 | μΑ μΑ μΑ |
| $\begin{split} DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_B = 3.8V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_B = 0V \text{ or } 2.4V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_B = -1.4V, V_A = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_A = V_B, -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \end{split}$ | -20 | | +20 | μΑ μΑ μΑ |
| $\begin{array}{l} 0V \leq V_{CC} \leq 1.5V \\ V_{B} = 3.8V, V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_{B} = 0V \mbox{ or } 2.4V, V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_{B} = -1.4V, V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_{A} = V_{B}, -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \end{array}$ | -20 | | +20 | μΑ μΑ μΑ |
| $\begin{split} & V_{B} = 3.8V, V_{A} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{B} = 0V \text{ or } 2.4V, V_{A} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{B} = -1.4V, V_{A} = 1.2V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ & V_{A} = V_{B}, -1.4V \leq V \leq 3.8V, \\ & DE = V_{CC} \\ & 0V \leq V_{CC} \leq 1.5V \\ \end{split}$ | -32 | | +20 | μΑ |
| $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ $V_B = 0V \text{ or } 2.4V, V_A = 1.2V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ $V_B = -1.4V, V_A = 1.2V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ $V_A = V_B, -1.4V \le V \le 3.8V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ | -32 | | +20 | μΑ |
| $\begin{array}{l} 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = 0V \mbox{ or } 2.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline V_{A} = V_{B}, \ -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \end{array}$ | -32 | | +20 | μΑ μΑ |
| $ \begin{array}{l} V_{B} = 0V \text{ or } 2.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{B} = -1.4V, \ V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \hline \\ V_{A} = V_{B}, \ -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ \end{array} $ | -32 | | | μΑ |
| $\begin{split} DE &= V_{CC} \\ 0V &\leq V_{CC} \leq 1.5V \\ \\ V_{B} &= -1.4V, V_{A} = 1.2V, \\ DE &= V_{CC} \\ 0V &\leq V_{CC} \leq 1.5V \\ \\ \\ V_{A} &= V_{B}, -1.4V \leq V \leq 3.8V, \\ DE &= V_{CC} \\ 0V &\leq V_{CC} \leq 1.5V \end{split}$ | -32 | | | μΑ |
| $\begin{array}{l} 0V \leq V_{CC} \leq 1.5V \\ V_{B} = -1.4V, V_{A} = 1.2V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \\ V_{A} = V_{B}, -1.4V \leq V \leq 3.8V, \\ DE = V_{CC} \\ 0V \leq V_{CC} \leq 1.5V \end{array}$ | -32 | | | μΑ |
| $V_{B} = -1.4V, V_{A} = 1.2V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ $V_{A} = V_{B}, -1.4V \le V \le 3.8V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ | | | +4 | |
| $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ $V_A = V_B, -1.4V \le V \le 3.8V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ | | | +4 | |
| $0V \le V_{CC} \le 1.5V$ $V_A = V_B, -1.4V \le V \le 3.8V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ | | | +4 | |
| $V_{A} = V_{B}, -1.4V \le V \le 3.8V,$ $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ | -4 | | +4 | uA |
| $DE = V_{CC}$ $0V \le V_{CC} \le 1.5V$ | -4 | | +4 | L UA |
| $0V \le V_{CC} \le 1.5V$ | -4 | | +4 | I UA |
| | | | | " |
| | | 9 | | |
| | | 9 | | pF pF |
| - | | 5.7 | | + · |
| _ | | 5.7 | | pF |
| | | 1.0 | | |
| | | | | 1 |
| $B_1 = 50\Omega$, $DE = V_{CC}$, $\overline{BE} = V_{CC}$ | | 20 | 29.5 | mA |
| | | | | mA |
| | - | | | mA |
| | $ \begin{array}{l} R_{L} = 50\Omega, DE = V_{CC}, \overline{RE} = V_{CC} \\ \\ DE = GND, \overline{RE} = V_{CC} \\ \\ \\ DE = GND, \overline{RE} = GND \end{array} $ | $DE = GND, \overline{RE} = V_{CC}$ | $DE = GND, \overline{RE} = V_{CC} \qquad 6$ | $DE = GND, \overline{RE} = V_{CC} \qquad 6 \qquad 9.0$ |

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 3, Note 8) Units Symbol Parameter Conditions Min Тур Max DRIVER AC SPECIFICATION Differential Propagation Delay Low to High 1.3 3.4 5.0 $R_{I} = 50\Omega, C_{I} = 5 pF,$ ns t_{PLH} Differential Propagation Delay High to Low $C_{D} = 0.5 \, pF$ 1.3 3.1 5.0 ns t_{PHL} $t_{SKD1} (t_{sk(p)})$ Pulse Skew It_{PLHD} – t_{PHLD}I (*Note 5, Note 9*) Figure 7 and Figure 8 300 420 ps Part-to-Part Skew (Note 6, Note 9) 1.3 t_{SKD3} ns Rise Time (Note 9) 1.0 1.8 3.0 t_{TLH} (t_r) ns Fall Time (Note 9) 1.0 1.8 3.0 $t_{THL} (t_f)$ ns Enable Time (Z to Active High) 8 t_{PZH} $R_L = 50\Omega$, $C_L = 5 pF$, ns Enable Time (Z to Active Low) $C_{D} = 0.5 \, pF$ t_{PZL} 8 ns Disable Time (Active Low to Z) Figure 9 and Figure 10 8 ns t_{PLZ} 8 Disable Time (Active High to Z) ns t_{PHZ} Random Jitter, RJ (Note 9) 100 MHz Clock Pattern (Note 7) 2.5 5.5 t_{JIT} nsrms 200 Maximum Data Rate f_{MAX} Mbps **RECEIVER AC SPECIFICATION** Propagation Delay Low to High $C_{1} = 15 \, \text{pF}$ 2.0 4.7 7.5 t_{PLH} ns Propagation Delay High to Low Figures 11, 12 and Figure 13 2.0 5.3 7.5 ns t_{PHL} Pulse Skew It_{PLHD} - t_{PHLD}I (Note 5, Note 9) 0.6 1.7 $t_{SKD1} (t_{sk(p)})$ ns Part-to-Part Skew (Note 6, Note 9) 1.3 ns t_{SKD3} t_{TLH} (t_r) Rise Time (Note 9) 0.5 1.2 2.5 ns 0.5 1.2 2.5 Fall Time (Note 9) $t_{THL}(t_f)$ ns t_{PZH} Enable Time (Z to Active High) 10 $R_{I} = 500\Omega, C_{I} = 15 \text{ pF}$ ns Figure 14 and Figure 15 Enable Time (Z to Active Low) 10 t_{PZL} ns Disable Time (Active Low to Z) 10 ns t_{PLZ} $\mathbf{t}_{\mathsf{PHZ}}$ Disable Time (Active High to Z) 10 ns Maximum Data Rate 200 Mbps f_{MAX}

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 3.3V and T_A = 25 ^{\circ}C.

Switching Characteristics

Note 4: The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this datasheet.

Note 5: t_{SKD1}, lt_{PLLD} - t_{PHLD}I, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

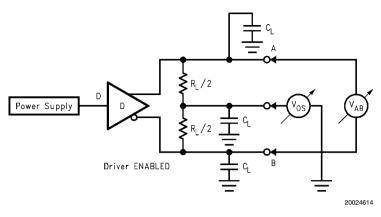
Note 6: t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 7: Stimulus and fixture Jitter has been subtracted.

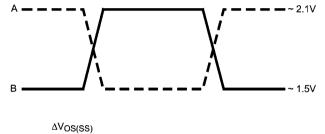
Note 8: C_L includes fixture capacitance and C_D includes probe capacitance.

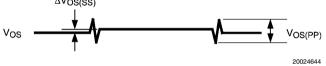
Note 9: Not production tested. Guaranteed by a statistical analysis on a sample basis at the time of characterization.

Test Circuits and Waveforms

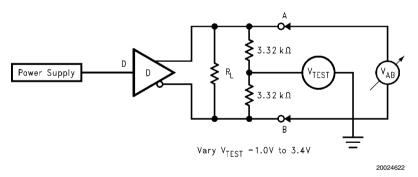














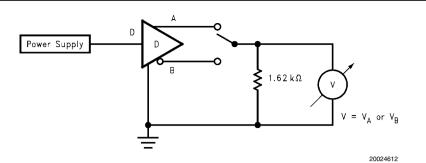


FIGURE 5. Differential Driver DC Open Test Circuit

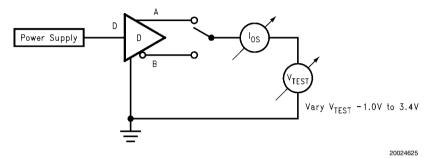


FIGURE 6. Differential Driver Short-Circuit Test Circuit

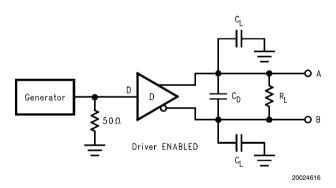


FIGURE 7. Driver Propagation Delay and Transition Time Test Circuit

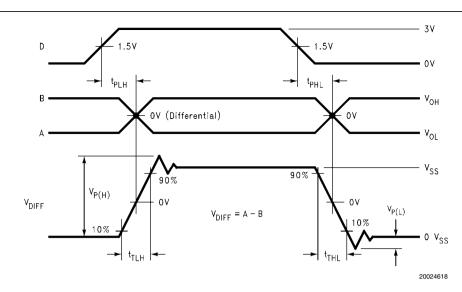
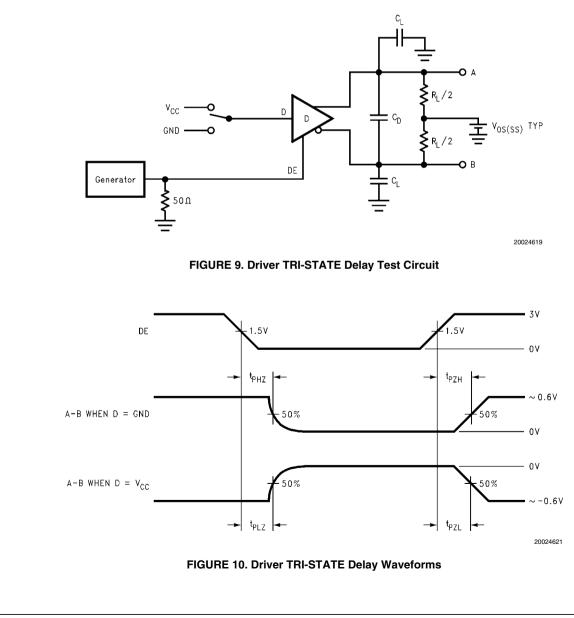


FIGURE 8. Driver Propagation Delays and Transition Time Waveforms



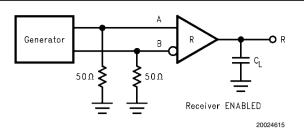


FIGURE 11. Receiver Propagation Delay and Transition Time Test Circuit

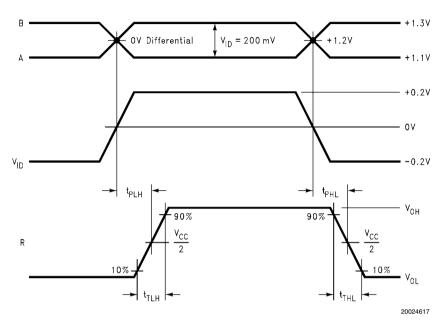
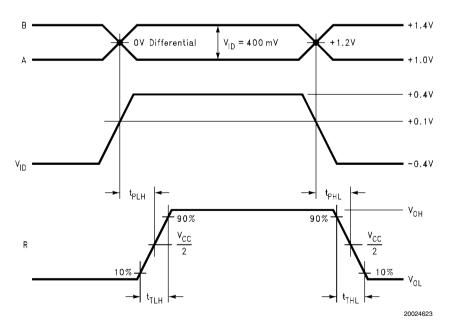
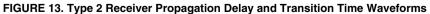


FIGURE 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms





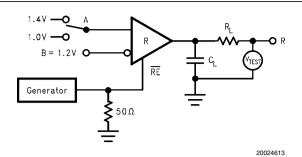


FIGURE 14. Receiver TRI-STATE Delay Test Circuit

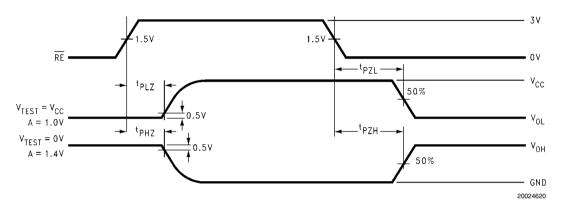


FIGURE 15. Receiver TRI-STATE Delay Waveforms

Function Tables

DS91D176/DS91C176 Transmitting

| Inputs | | | Out | puts |
|--------|------|------|-----|------|
| RE | DE | D | В | Α |
| Х | 2.0V | 2.0V | L | н |
| Х | 2.0V | 0.8V | н | L |
| Х | 0.8V | х | Z | z |

X — Don't care condition

Z — High impedance state

DS91D176 Receiving

| | Inputs | | Output |
|------|--------|----------|--------|
| RE | DE | A – B | R |
| 0.8V | 0.8V | ≥ +0.05V | Н |
| 0.8V | 0.8V | ≤ -0.05V | L |
| 0.8V | 0.8V | 0V | Х |
| 2.0V | 0.8V | Х | Z |

DS91C176 Receiving

| | Output | | |
|------|--------|----------|---|
| RE | DE | A – B | R |
| 0.8V | 0.8V | ≥ +0.15V | Н |
| 0.8V | 0.8V | ≤ +0.05V | L |
| 0.8V | 0.8V | 0V | L |
| 2.0V | 0.8V | Х | Z |

X — Don't care condition Z — High impedance state

X — Don't care condition Z — High impedance state

DS91D176 Receiver Input Threshold Test Voltages

| Applied | plied Voltages Resulting Differential Input Resulting Common-Mode Voltage Input Voltage | | Receiver Output | |
|-----------------|--|-----------------|--------------------|---|
| V _{IA} | V _{IB} | V _{ID} | V _{IC} | R |
| 2.400V | 0.000V | 2.400V | 1.200V | Н |
| 0.000V | 2.400V | -2.400V | 1.200V | L |
| 3.800V | 3.750V | 0.050V | 3.775V | Н |
| 3.750V | 3.800V | -0.050V | 3.775V | L |
| -1.400V | -1.350V | -0.050V | -1.375V | Н |
| -1.350V | -1.400V | 0.050V | -1.375V | L |

H — High Level L — Low Level

Output state assumes that the receiver is enabled ($\overline{RE} = L$)

DS91C176 Receiver Input Threshold Test Voltages

| Applied | Voltages | Resulting Differential Input Voltage | Resulting Common-Mode Input Voltage | Receiver Output |
|---------|-----------------|---|--|--------------------|
| VIA | V _{IB} | V _{ID} | V _{IC} | R |
| 2.400V | 0.000V | 2.400V | 1.200V | Н |
| 0.000V | 2.400V | -2.400V | 1.200V | L |
| 3.800V | 3.650V | 0.150V | 3.725V | н |
| 3.800V | 3.750V | 0.050V | 3.775V | L |
| -1.250V | -1.400V | 0.150V | -1.325V | н |
| -1.350V | -1.400V | 0.050V | -1.375V | L |

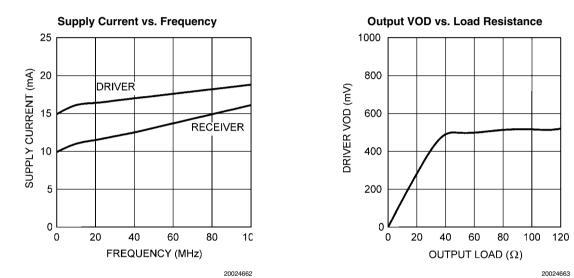
H — High Level

L — Low Level Output state assumes that the receiver is enabled ($\overline{RE} = L$)

Pin Descriptions

| Pin No. | Name | Description |
|---------|-----------------|--|
| 1 | R | Receiver output pin |
| 2 | RE | Receiver enable pin: When \overline{RE} is high, the receiver is disabled. When \overline{RE} is low or open, the receiver is enabled. |
| 3 | DE | Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled. |
| 4 | D | Driver input pin |
| 5 | GND | Ground pin |
| 6 | А | Non-inverting driver output pin/Non-inverting receiver input pin |
| 7 | В | Inverting driver output pin/Inverting receiver input pin |
| 8 | V _{cc} | Power supply pin, +3.3V ± 0.3V |

Typical Performance Characteristics

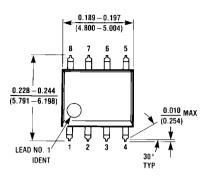


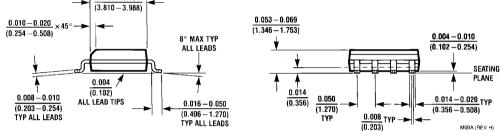
Supply Current measured using a clock pattern with driver terminated to 50ohms .V_{CC} = 3.3V, T_A = +25°C V_{CC} = 3.3V, T_A = +25°C.

FIGURE 16. DS91D176/DS91C176 Typical Performance Characteristics

Physical Dimensions inches (millimeters) unless otherwise noted

0.150-0.157





Order Number DS91D176TMA, DS91C176TMA See NS package Number M08A

Notes

| Products | | Design Support | |
|--------------------------------|------------------------------|---------------------------------|-------------------------------|
| Amplifiers | www.national.com/amplifiers | WEBENCH® Tools | www.national.com/webench |
| Audio | www.national.com/audio | App Notes | www.national.com/appnotes |
| Clock and Timing | www.national.com/timing | Reference Designs | www.national.com/refdesigns |
| Data Converters | www.national.com/adc | Samples | www.national.com/samples |
| Interface | www.national.com/interface | Eval Boards | www.national.com/evalboards |
| LVDS | www.national.com/lvds | Packaging | www.national.com/packaging |
| Power Management | www.national.com/power | Green Compliance | www.national.com/quality/gree |
| Switching Regulators | www.national.com/switchers | Distributors | www.national.com/contacts |
| LDOs | www.national.com/ldo | Quality and Reliability | www.national.com/quality |
| LED Lighting | www.national.com/led | Feedback/Support | www.national.com/feedback |
| Voltage Reference | www.national.com/vref | Design Made Easy | www.national.com/easy |
| PowerWise® Solutions | www.national.com/powerwise | Solutions | www.national.com/solutions |
| Serial Digital Interface (SDI) | www.national.com/sdi | Mil/Aero | www.national.com/milaero |
| Temperature Sensors | www.national.com/tempsensors | SolarMagic™ | www.national.com/solarmagic |
| Wireless (PLL/VCO) | www.national.com/wireless | PowerWise® Design University | www.national.com/training |

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2009 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center Email: europe.support@nsc.com National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com National Semiconductor Japan Technical Support Center Email: jpn.feedback@nsc.com