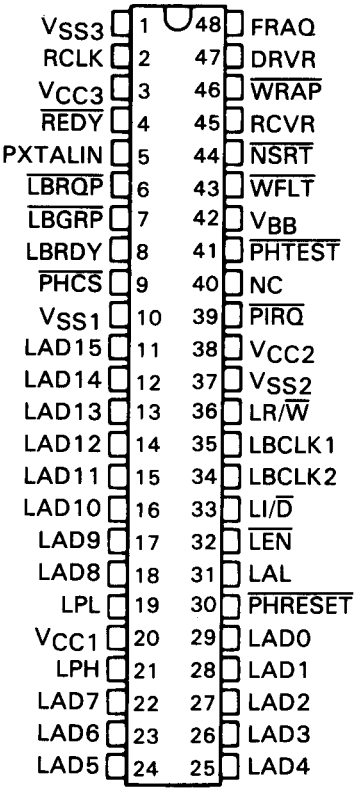
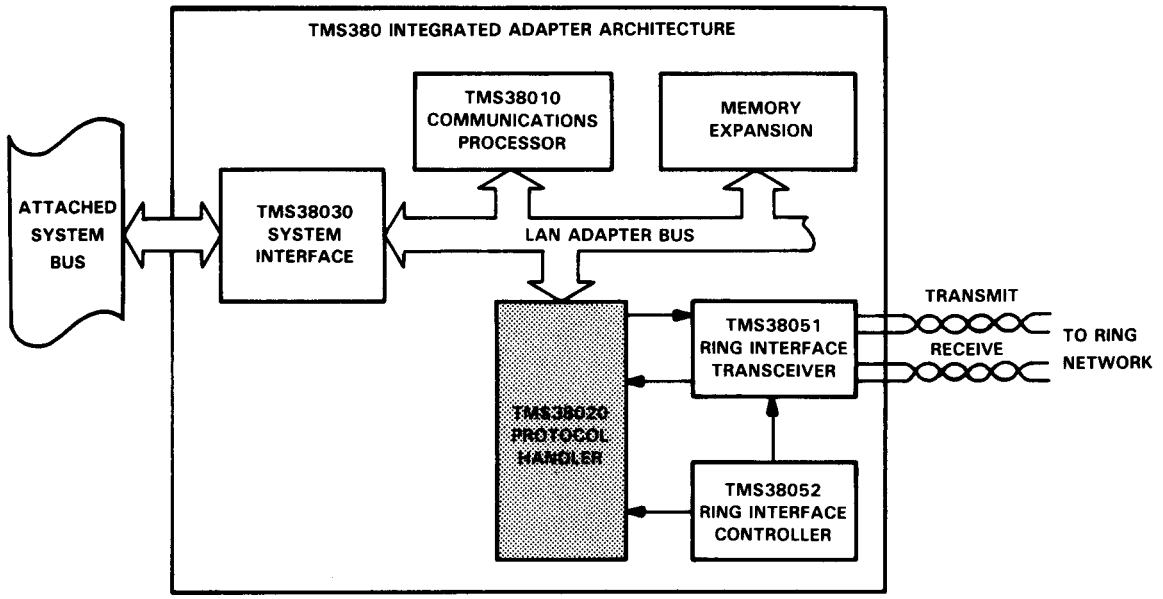
SEPTEMBER 1985 – REVISED MAY 1986

- Compatible with IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications
  - Differential Manchester Code Conversion on 4M-Bit per Second Serial Data Stream
  - Address Recognition (Functional, Group and Specific)
  - Manchester Code Violation Detection
  - Starting and Ending Delimiter Generation and Detection
  - CRC Generation and Checking
  - High-Speed Frame Repeat Path Minimizes Ring Latency (2-Bit Times)
  - Token Transmit and Priority Control
  - Monitor Functions
- Separate Pairs of DMA Channels for Receive and Transmit
- Automatic Frame Buffer Management
- On-Chip 16K-Byte ROM for Adapter Software
  - 8K x 18-Bit ROM with Byte Parity Protection
  - Single Word Prefetch
- Test Pin for Hi-Z, Module-in-Place Testing
- 48-Pin, 600-Mil, Ceramic Dual-in-Line Packaging
- Low-Power Scaled-NMOS Technology

JD PACKAGE
(TOP VIEW)



token ring LAN application diagram



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pin descriptions

NAME	I/O	DESCRIPTION
		LAN ADAPTER BUS INTERFACE PINS
LBCLK1, LBCLK2	I	Bus Clocks
$\overline{\text{LAL}}$	I/O	Address Latch Enable
$\overline{\text{LEN}}$	I/O	Data Enable
LBRDY	I/O	Bus Ready
$\overline{\text{PIRQ}}$	O	PH Interrupt Request
$\overline{\text{LBRQP}}$	O	Bus Request
$\overline{\text{LBGRP}}$	I	Bus Grant
LAD0 - LAD15	I/O	Address/Data bus. LAD0 is the most-signiticant bit, LAD15 is the least-significant bit.
LPH,LPL	I/O	Parity High/Parity Low
LI/$\overline{\text{D}}$	I/O	Instruction/Data Bus Status Code
LR/$\overline{\text{W}}$	I/O	Read/Not Write
$\overline{\text{PHRESET}}$	I	Reset
$\overline{\text{PHCS}}$	I	Chip Select
		RING INTERFACE PINS
DRVR	O	Transmitter Data
FRAQ	O	Frequency Acquisition Select
$\overline{\text{NSRT}}$	O	Insert Control
RCLK	I	Recovered Data Clock
RCVR	I	Received Data
$\overline{\text{REDY}}$	I	Ring Interface Ready
$\overline{\text{WFLT}}$	I	Wire Fault Detect
$\overline{\text{WRAP}}$	O	Wrap Select
PXTALIN	I	Ring Frequency Reference Clock
		MISCELLANEOUS PINS
$\overline{\text{PHTEST}}$	I	Module-in-Place Test Mode Select. This pin should be left unconnected.
V_{CC}		5-V supply pins.
V_{SS}		Ground pins.
V_{BB}		Substrate bias. This pin is reserved and should be left unconnected.
NC		Reserved. This pin should be left unconnected.

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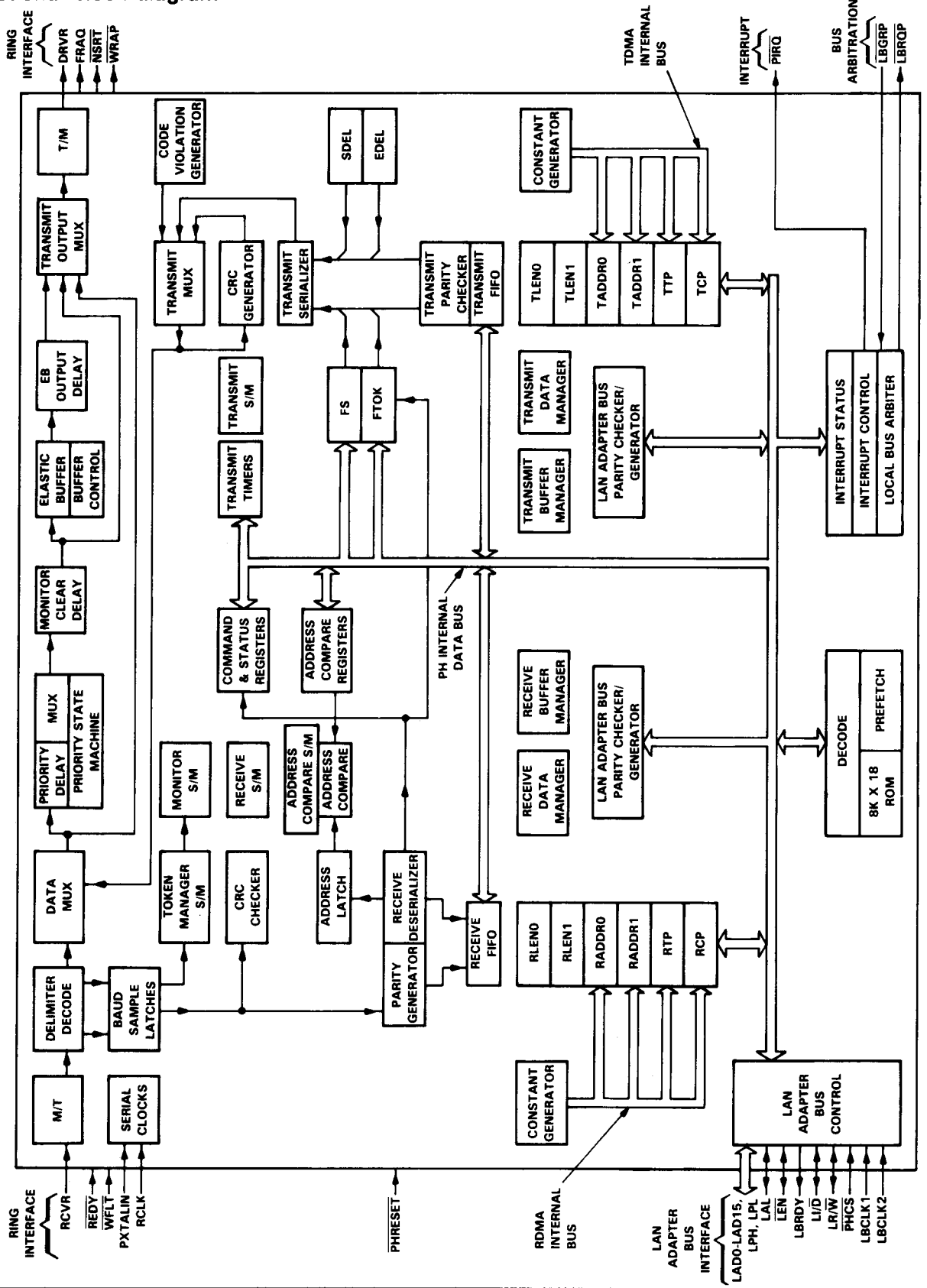
functional block diagram



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description

The TMS38020 Protocol Handler integrates onto a single chip the hardware-based protocol functions for a 4 megabit per second token ring Local Area Network (LAN). An on-chip ROM contains 16K bytes of software used by the TMS38010 Communications Processor for implementation of a complete token ring Adapter function. The TMS38020 provides Differential Manchester encoding and decoding, frame address recognition, and includes state machine functions which capture free tokens, transmit and receive frames, manage the Adapter RAM buffers and provide token transmit and priority controls. Four DMA channels, two for transmit and two for receive, insure high-speed transfer of frames between the Adapter's buffer RAM and the ring. Integrity of transmitted and received data is provided by CRC generation and checking, detection of Differential Manchester code violations, and parity on internal data paths and at the LAN Adapter bus interface.

The TMS38020, when coupled with the TMS38010 Communications Processor, the TMS38030 System Interface, and the TMS38051 and TMS38052 Ring Interface chips, forms a highly integrated token ring LAN Adapter.

architecture

The TMS38020 Protocol Handler contains a bus master interface to the LAN Adapter bus for transfer of frame data between itself and LAN Adapter bus memory, a bus slave interface to the LAN Adapter bus for control by an external CPU, an interface to the Ring Interface circuit, and a 16K-byte ROM. Internal to the TMS38020 are several finite-state machine-implemented functions which provide bit-and frame-level processing of token protocols as well as control the flow of DMA data to and from buffer RAM resident on the LAN Adapter bus. The following paragraphs describe the blocks shown in the functional block diagram.

address compare state machine

The address compare state machine controls the recognition of addresses in a received frame (including stripped frames). A description of frame addressing methodology may be found in the Communications Services Section of the User's Guide.

CRC checker

This block contains a 32-bit feedback shift register for calculation of the cyclic redundancy code of frames received. The TMS38020 calculates the CRC for each frame that the TMS38020 receives. If the calculated CRC does not agree with the CRC value of the received frame, the TMS38020 sets an error indicator bit within the frame to flag the occurrence of the error. If the TMS38020 was copying the frame at the time the CRC error was detected (due to an address match), the TMS38020 notifies the LAN Adapter CPU of the error. Mathematically, the CRC is calculated by considering the checked bytes as a polynomial and dividing it modulo 2 by the following polynomial:

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

CRC generator

The cyclic redundancy code (CRC) generator generates the CRC field to be inserted by the TMS38020 when transmitting. The procedure for generating CRC is identical to that described for the CRC checker.

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data multiplexer

The data multiplexer selects the source of the data to be transmitted. The source may be received ring data (repeat mode), a constant of zeros (idles), or data to be transmitted by the TMS38020.

delimiter decode

This block detects the Start Delimiter (SDEL) and End Delimiter (EDEL) sequences defined for the protocol.

elastic buffer

The elastic buffer absorbs the accumulated phase jitter in the ring. During normal operation, only one station (the Active Monitor) inserts its elastic buffer on the ring. As the accumulated phase delay around the ring varies, it is "absorbed" by the elastic buffer. The elastic buffer can absorb ± 3 bits of accumulated jitter. The total delay through the elastic buffer is 3 ± 3 bits. When the elastic buffer is not inserted on the ring, it permits the TMS38020 to detect when the incoming data frequency falls outside acceptable bounds by detecting overrun and underrun conditions.

The overrun and underrun conditions are defined to occur within a specific number of bit times. To minimize the possibility of overrun and underrun over longer periods of time, the PH re-initalizes the elastic buffer every 512 bit times when in standby monitor mode and whenever the PH detects a token when in active monitor mode.

fire token register (FTOK)

The fire token register is used to hold the access control (AC) field that will be used in transmitting a token on the ring.

interrupt status logic

The interrupt status logic contains a register with information concerning TMS38020 interrupts. This logic provides interrupt vectoring, masking, and prioritization.

LAN Adapter bus parity checker

The LAN Adapter bus parity checker checks all data placed on the internal TMS38020 data bus from the LAN Adapter bus. This includes data written to the TMS38020 by an external bus master, data read by the TMS38020 receive or transmit buffer manager, and data read by the TMS38020 transmit DMA unit for transmission on the ring.

LAN Adapter bus parity generator

The parity generator generates the parity to be placed on the LAN Adapter bus when any TMS38020 register is read by an external bus master. However, receive data which has parity generated by the serial parity generator has no parity generated by the bus parity generator.

manchester-to-transitional decoder (M/T)

This functional block converts the Differential Manchester code received from the ring into an internal format called "transitional" code. Transitional code is so named because baud† are encoded based upon their transition from the previous baud. The receive data sampled on pin RCVR is sampled by the recovered data clock input on pin RCLK.

monitor delay

The token ring protocol calls for a ring function called an Active Monitor. Each ring will have one Active Monitor which is chosen during a contention process. One function of an Active Monitor is to introduce enough delay in a ring to provide a minimum length ring sufficient to circulate a free token. When the TMS38020 is configured as an Active Monitor [the CXMT bit of the Ring Command 1 (RINGCMD1) register is set], it inserts additional monitor delay to meet the effective ring length requirement. The monitor delay

†Two baud equals one bit of Differential Manchester encoding.

consists of a 7.5-baud (half-bit times) delay preceding the elastic buffer and a 22.5-baud delay succeeding it. The total delay through the TMS38020 when the Active Monitor mode is selected is 4-baud normal delay plus 19-baud for the priority delay plus 30-baud for the monitor delay plus 6-baud average elastic buffer delay. This delay totals 59 ± 6 baud.

monitor state machine

The monitor state machine controls the setting of the Monitor Count bit of busy or priority tokens which are repeated on the ring and the detection of token activity on the ring. This state machine is active when the TMS38020 is configured as an Active Monitor [MON bit of Ring Command 1 Register (RINGCMD1) is set].

priority delay and state machine

The TMS38020 provides control of seven levels of token priority. The priority state machine is responsible for controlling the token priority as defined by the protocol. The priority delay of 19 half-bit times is inserted when a station releases a token to allow the station to modify the token according to the priority protocol.

receive buffer manager

The receive buffer manager controls the receive buffer chaining operations on the LAN Adapter bus.

receive data manager

The receive data manager requests and acknowledges LAN Adapter bus cycles for DMA to write the received frame into memory on the LAN Adapter bus.

receive deserializer

The receive deserializer block is a 16-bit serial-in parallel-out shift register. The input is the sampled data from the ring. A serial parity generator unit calculates the parity for each eight bits shifted in and stores this parity with the parallel data. The 18 bits of data and parity are then loaded in parallel into the receive FIFO buffer.

receive DMA registers

The receive DMA registers are indicated in the functional block diagram by the names RCP, RTP, RADDR0, RADDR1, RLEN0, and RLEN1. These registers are managed by the receive buffer manager. Only the register RCP (receive chain pointer) may be accessed by external LAN Adapter bus masters. The remaining registers are not accessible by external bus masters. A brief description of these registers follows.

receive chain pointer (RCP)

This register contains the address of the buffer currently being filled with data from the ring.

receive temporary pointer (RTP)

The receive temporary pointer register contains the starting address of the buffer into which the receive DMA channel will store data when the buffer being used is full.

channel address registers (RADDR0, RADDR1)

The TMS38020 maintains two DMA channels for receive operations. The channel address register for both receive DMA channels contains the LAN Adapter bus address of the word being accessed by that channel.

channel length registers (RLEN0, RLEN1)

The channel length register for each of the two receive DMA channels contains the number of empty bytes left in the buffer currently being filled by that channel.

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receive FIFO

The receive first-in, first-out (FIFO) buffer stores up to two words (16 bits) of deserialized data before it is transferred via DMA onto the LAN Adapter bus. Data is transferred onto the LAN Adapter bus under control of the receive data manager block.

serial receive state machine

This state machine controls operation of the receiver portion of the serial data path.

serial transmit state machine

This state machine controls the operation of the serial transmit data path.

transitional-to-manchester decoder (T/M)

This functional block converts the internal transitional code representation of transmit data to Differential Manchester code.

transmit buffer manager

The transmit buffer manager performs the automatic buffer chaining of transmit buffers contained in LAN Adapter bus memory.

transmit data manager

The transmit data manager requests and acknowledges LAN Adapter bus cycles for DMA to read data to be transmitted on the ring.

transmit DMA registers

The transmit DMA registers (TCP, TTP, TADDR0, TADDR1, TLEN0, and TLEN1) are managed by the transmit buffer manager. Of these, only the transmit chain pointer (TCP) may be loaded by external LAN Adapter bus masters. The remaining registers are not accessible by external bus masters. The transmit DMA registers are described briefly below.

transmit chain pointer (TCP)

The transmit chain pointer contains the address of the buffer currently being read for transmit data.

transmit temporary pointer (TTP)

The transmit temporary pointer register contains the starting address of the buffer from which transmit data will be read by the DMA channel when the present buffer has been read.

channel address registers (TADDR0, TADDR1)

The TMS38020 maintains two DMA channels for transmit operations. The channel address register for both transmit DMA channels contains the LAN Adapter bus address of the word being read by that channel.

channel length registers (TLEN0, TLEN1)

The channel length register for each of the two transmit DMA channels contains the number of bytes yet to be transmitted from the current buffer.

transmit FIFO

The transmit FIFO buffers two 16-bit words, allowing the TMS38020 to maintain a constant flow of transmitted data into the transmit serializer. The parity from the LAN Adapter bus is maintained within the FIFO.

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transmit multiplexer

The transmit multiplexer selects either the CRC generator or transmit serializer output onto the transmit data path.

transmit parity checker

The transmit parity checker checks the parity of data transferred from the top of the transmit FIFO to the transmit serializer. It performs the final check of data before it is placed in the serializer.

transmit serializer

The transmit serializer is a 16-bit parallel-in, serial-out shift register. The shift register is loaded from the data at the top of the transmit FIFO, from the concatenation of the Start Delimiter (SDEL) and the fire token register (FTOK) or from a concatenation of the End Delimiter (EDEL) and the frame status (FS) register.

transmit timer

The TMS38020 contains a physical trailer timer (PTT). This timer provides a watchdog timer function for halting the frame strip process after transmitting a frame.

command and status registers

The command and status registers of the TMS38020 are registers which may be read/written through memory-mapped I/O by an external bus master on the LAN Adapter bus. These registers are mapped to LAN Adapter bus addresses as shown in Table 1.

ADDRESS	BITS				DESCRIPTION
	0	7	8	15	
>0100	RINGCMD0				RING COMMAND 0
>0102	RINGCMD1				RING COMMAND 1
>0104	RINGSTS				RING STATUS
>0106	INTSTAT				INTERRUPT STATUS
>0108	00†		PTTLATCH		PHYSICAL TRAILER TIMER LATCH
>010A	RCP				RECEIVE CHAIN POINTER
>010C	TCP				TRANSMIT CHAIN POINTER
>010E	FTOK		00‡		FIRE TOKEN

†Most-significant bits are reserved.
‡Least-significant bits are reserved.

FIGURE 1. TMS38020 COMMAND AND STATUS REGISTERS

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ring command 0 (RINGCMD0)

The RINGCMD0 register enables specific receive and transmit modes of the TMS38020 including idle insertion between frames and stripping of transmitted data from the ring. The bits of RINGCMD0 are defined in Table 1.

TABLE 1. RING COMMAND 0 (RINGCMD0) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	XMTIMM	Transmit Immediate Mode
1	BDM	Baud Data Mode
2	NOSTRIP	No Strip Mode
3	XMTCRC	Transmit CRC
4	RNFT	Release No Free Token
5	XMTIDLE	Transmit Idles Mode
6	ETO	Enable Transmitter Output
7	PTEST	Parity Test
8	GAP0	Interframe Gap Bit 0
9	GAP1	Interframe Gap Bit 1
10	GAP2	Interframe Gap Bit 2
11		Reserved. This bit must be zero.
12		Reserved. This bit must be zero.
13		Reserved. This bit must be zero.
14		Reserved. This bit must be zero.
15	NOCHAIN	No Receive Chaining

ring command 1 (RINGCMD1)

The RINGCMD1 register is the master control register of the TMS38020. This register controls such functions as reset, clock sourcing, ring insertion, and address recognition. The bits of RINGCMD1 are defined in Table 2. The functions of receive options, ROPT0 and ROPT1, are presented in Table 3.

TABLE 2. RING COMMAND 1 (RINGCMD1) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	NRESET	Not Reset
1	NFRAQ	Not Frequency Acquisition
2	INSERT	Insert Into Ring
3	NWRAP	Not Internal Wrap
4	CXMT	Crystal Transmit Mode Select
5	MON	Active Monitor Mode Select
6		Reserved. This bit must be set to zero.
7		Reserved. This bit must be set to one.
8		Reserved. This bit must be set to zero.
9	IGN0	Ignore Control 0
10	IGN1	Ignore Control 1
11	IGN2	Ignore Control 2
12	IGN3	Ignore Control 3
13	ROPT0	Receive Option 0
14	ROPT1	Receive Option 1
15		Reserved.

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TABLE 3. RECEIVE OPTION BIT DECODE

ROPT0	ROPT1	DESCRIPTION
0	0	Copy frame if address match
0	1	Copy if MAC frame and address match
1	1	Copy all frames; set ARI and FCI only if address match.
1	0	Reserved. Must not be used.

ring status register (RINGSTS)

The RINGSTS register provides general ring status information, including ring interface status, error logging, and token validation. The bits of RINGSTS are defined in Table 4.

TABLE 4. RING STATUS (RINGSTS) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	NGO	Not Go (Signal Loss)
1	GTDET	Good Token Detect
2	ATDET	Any Token Detect
3	WFAULT	Wire Fault
4	EBOUF	Elastic Buffer Over/Under Flow
5-9		Reserved
10	MAC0	MAC Attention Code Bit 0
11	MAC1	MAC Attention Code Bit 1
12	MAC2	MAC Attention Code Bit 2
13	MAC3	MAC Attention Code Bit 3
14	RIDER0	FS Rider Control Bit 0
15	RIDER1	FS Rider Control Bit 2

interrupt status (INTSTAT)

The INSTAT register contains information concerning TMS38020 interrupts. This register provides interrupt vectoring, masking, and prioritization. The bits of INSTAT are defined in Table 5. Table 6 lists the decode for bits 11 through 14 (INTCODE0 through INTCODE3).

TABLE 5. INTERRUPT STATUS (INTSTAT) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	MIE	Master Interrupt Enable
1		Reserved
2	EORBE	End of Receive Buffer Interrupt Enable
3	EOTBE	End of Transmit Buffer Interrupt Enable
4	SLIE	Signal Loss Interrupt Enable
5-7		Reserved
8	ID0	Interrupt Source ID Bit 0
9	ID1	Interrupt Source ID Bit 1
10	ID2	Interrupt Source ID Bit 2
11	INTCODE0	Interrupt Code Bit 0
12	INTCODE1	Interrupt Code Bit 1
13	INTCODE2	Interrupt Code Bit 2
14	INTCODE3	Interrupt Code Bit 3
15	"0"	Always zero

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TABLE 6. INTERRUPT CODE 0 (INTCODE0) THROUGH INTERRUPT CODE 3 (INTCODE3) DECODE

INTCODE0	INTCODE1	INTCODE2	INTCODE3	DEFINITION
0	0	0	0	Reserved
0	0	0	1	LAN Adapter Bus Parity Error
0	0	1	0	Token Error
0	0	1	1	Signal Loss
0	1	0	0	BURST5 Error in Frame
0	1	0	1	Log Error
0	1	1	0	No Buffer Available
0	1	1	1	Attention
1	0	0	0	Reserved
1	0	0	1	Receive Frame Error
1	0	1	0	Transmit Frame Error
1	0	1	1	Receive End of Buffer
1	1	0	0	Transmit End of Buffer
1	1	0	1	Receive End of Frame
1	1	1	0	Transmit End of Frame
1	1	1	1	No Interrupt Pending

physical trailer timer latch (PTTLATCH)

The PTTLATCH register is an 8-bit control register containing a ring-speed-specific time constant. This value is the starting value of a timer which is started following the transmission of a frame so that a lost frame condition may be detected.

receive chain pointer (RCP)

The RCP register contains the starting address of the buffer into which the receive DMA channel, if active, stores receive data.

transmit chain pointer (TCP)

The TCP register contains the starting address of the buffer into which the transmit DMA channel, if active, reads data for transmission.

fire free token register (FTOK)

The FTOK register is used to hold the Access Control Field (AC) to be included in a token that will be generated by the TMS38020 and transmitted on the ring. Writing to the FTOK register causes a token to be released.

address compare registers

The TMS38020 contains 15 registers for use in comparing frame addresses. These registers are shown with their corresponding LAN Adapter bus addresses in Figure 2.

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ADDRESS	NAME	DESCRIPTION
>0110	SAH	LOCAL SPECIFIC ADDRESS BITS 0-15
>0112	SAM	LOCAL SPECIFIC ADDRESS BITS 16-31
>0114	SAL	LOCAL SPECIFIC ADDRESS BITS 32-47
>0116		RESERVED. ALWAYS READ AS ZERO.
>0118	STRIPHI	STRIP ADDRESS BITS 16-31
>011A	STRIPLO	STRIP ADDRESS BITS 32-47
>011C	GNAHI	LOCAL GROUP ADDRESS BITS 0-15
>011E	GNALO	LOCAL GROUP ADDRESS BITS 16-31
>0120	>0000	RESERVED†
>0122	>0000	RESERVED†
>0124	>0000	RESERVED†
>0126	>0000	RESERVED†
>0128	>0000	RESERVED†
>012A	>0000	RESERVED†
>012C	FNAHI	FUNCTIONAL ADDRESS BITS 0-15
>012E	FNALO	FUNCTIONAL ADDRESS BITS 16-31

†These registers must be initialized to zero following power up.

FIGURE 2. ADDRESS COMPARE REGISTERS

buffer management

The TMS38020's buffer managers move frame data in and out of buffer RAM, located on the LAN Adapter bus, through one or more singly-linked buffers. These buffers are aligned on 8-byte boundaries and have the organization for transmit and receive as shown in Figure 3.

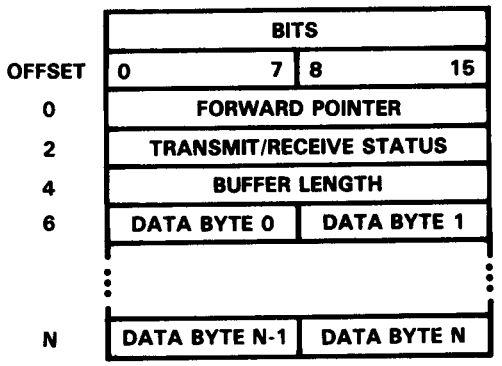

FIGURE 3. BUFFER ORGANIZATION

The forward pointer contains the address of the next buffer in a chain. The transmit/receive status field is used to report frame status. The length field contains the number of bytes in the data field of the buffer. This field is initialized by the LAN Adapter bus CPU.

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transmit buffers

When the buffer organization shown in Figure 3 is used for transmit frames, the status field has the bit functions shown in Table 7 in the last buffer in a chain used to transmit the frame.

TABLE 7. TRANSMIT STATUS FIELD BIT FUNCTIONS

BIT	NAME	FUNCTION
0	INUSE	In Use Indicator
1	LFED	Local Frame Error Detect
2	RTEDI	Returned Error Detected Indicator
3	TCC0	Transmit Completion Code Bit 0
4	TCC1	Transmit Completion Code Bit 1
5	TCC2	Transmit Completion Code Bit 2
6	TCC3	Transmit Completion Code Bit 3
7	EOF	End Of Frame Indicator
8	FS0	Stripped Frame Status Bit 0 (ARI)
9	FS1	Stripped Frame Status Bit 1 (FCI)
10	FS2	Stripped Frame Status Bit 2
11	FS3	Stripped Frame Status Bit 3
12	FS4	Stripped Frame Status Bit 4 (ARI)
13	FS5	Stripped Frame Status Bit 5 (FCI)
14		Reserved. This bit is zero.
15		Reserved. This bit is zero.

The decoded function of the transmit completion code bits (TCC) is presented in Table 8.

TABLE 8. TRANSMIT COMPLETION CODE (TCC) BIT DECODE

PARALLEL LAN ADAPTER BUS PATH

TCC0	TCC1	DESCRIPTION
0	0	Normal Completion
0	1	Parity Error
1	0	DMA Underrun
1	1	Next Buffer Unavailable

SERIAL RING DATA PATH

TCC2	TCC3	DESCRIPTION
0	0	Normal Completion
0	1	PTT Timeout
1	0	Invalid Free Token
1	1	Invalid Abort on Strip

For frames to be transmitted on the ring, the data portion of a transmit buffer has the format shown in Figure 4.

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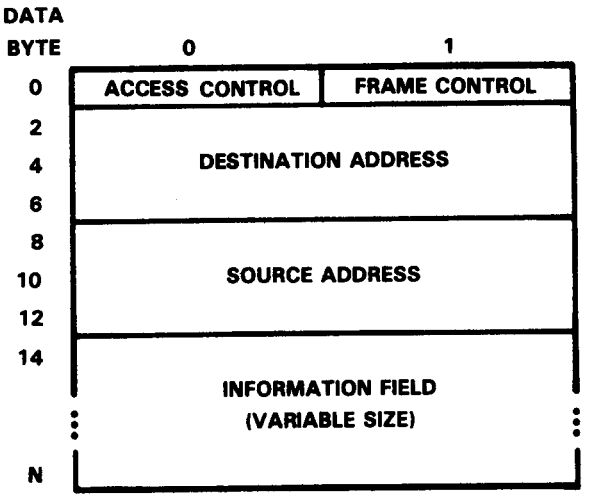

FIGURE 4. TRANSMIT DATA FORMAT

receive buffers

When the buffer organization shown in Figure 3 is used for receive frames, the status field has the bit functions shown in Table 9 in the last buffer in a chain used to receive the frame.

TABLE 9. RECEIVE STATUS FIELD BIT FUNCTIONS

BIT	NAME	FUNCTION
0	INUSE	In Use
1	LFED	Local Frame Error Detect
2	REDI	Received Error Detected Indicator
3	RCC0	Receive Completion Code Bit 0
4	RCC1	Receive Completion Code Bit 1
5	RCC2	Receive Completion Code Bit 2
6	RCC3	Receive Completion Code Bit 3
7	EOF	End of Frame Indicator
8	FS0	Receive Frame Status Bit 0
9	FS1	Receive Frame Status Bit 1
10	FS2	Receive Frame Status Bit 2
11	FS3	Receive Frame Status Bit 3
12	FS4	Receive Frame Status Bit 4
13	FS5	Receive Frame Status Bit 5
14		Reserved
15		Reserved

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The decoded function of the receive completion code bits (RCC) is presented in Table 10.

TABLE 10. RECEIVE COMPLETION CODE (RCC) BIT DECODE

PARALLEL LAN ADAPTER BUS PATH

RCC0	RCC1	DESCRIPTION
0	0	Normal Completion
0	1	Parity Error
1	0	DMA Overrun
1	1	Next Buffer Unavailable

SERIAL RING DATA PATH

RCC2	RCC3	DESCRIPTION
0	0	Normal Completion
0	1	Error: FCI not set
1	0	Implicit Abort
1	1	Explicit Abort

For frames received from the ring, the data portion of a receive buffer has the format shown in Figure 5.

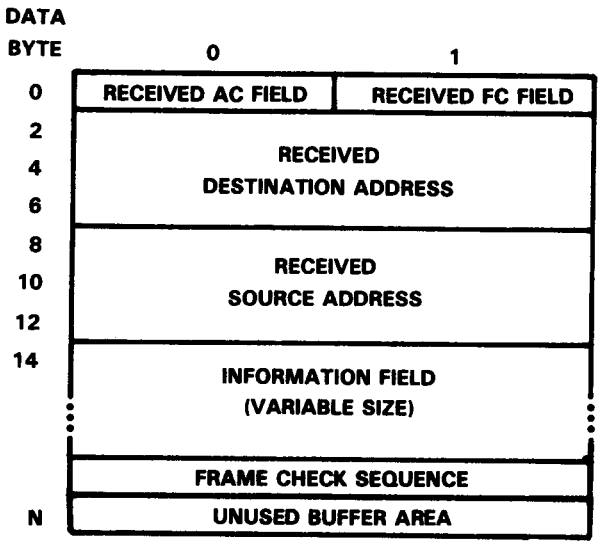

FIGURE 5. RECEIVE DATA FORMAT

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TMS38020 ROM

The TMS38020 contains a 16K-byte ROM organized as 8K x 18 bits. Each byte contains an odd parity bit. The ROM is not used by internal TMS38020 logic but is accessed by the LAN Adapter bus CPU for program storage. This ROM contains object code for the TMS38010 Communications Processor. This ROM contains software which provides media access protocols compatible with IEEE Std 802.5-1985, protocol services for network management servers, and diagnostics which verify proper functionality of the TMS380 Token Ring Adapter.

Access to this ROM from the TMS38010 Communications Processor is in one or two LAN Adapter bus read cycles. A prefetch unit reads the word sequentially following the last word read so that sequential accesses occur with no wait states forced on the TMS38010. When access is nonsequential, the TMS38020 deasserts LBRDY in the first cycle to force the CPU to accept a wait state. On the second cycle, the TMS38020 asserts LBRDY and places the ROM data on the bus.

For testing purposes, the TMS38020 ROM should not be accessed for more than eight consecutive read cycles to successive (sequential) locations unless an intervening non-read cycle (one LBCLK cycle) or a non-sequential read cycle is performed.

When the TMS38020 is a bus slave, it will also respond if external circuitry deasserts LBRDY; it will continuously drive its output data (on reads) or delay modifying its internal register (on writes) until LBRDY is asserted high.

address decoding

The TMS38020 performs decoding of LAN Adapter bus addresses as shown in Table 12. Note that not all addresses are strictly decoded. For example, the TMS38020 does not decode address line A1 for ROM accesses at >C000. Thus, a memory read at address location >8000 is identical to an address read at location >C000. For this reason, expansion RAM on the LAN Adapter bus should negate $\overline{\text{PHCS}}$ whenever expansion RAM overlays memory addresses >8000 through >BFFF.

TABLE 12. TMS38020 ADDRESS DECODING

$\overline{\text{PHCS}}$	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	SELECTED TMS38020 LOCATION
H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	L	L	L	L	L	L	L	X	X	X	X	X	X	X	TMS38020 not selected
L	L	L	L	L	L	L	L	H	X	X	L	L	Int'l Decode			Command/Status Registers
L	L	L	L	L	L	L	L	H	X	X	L	H	Int'l Decode			Address Compare Registers
L	L	L	L	L	L	L	L	H	X	X	H	L	Int'l Decode			Compare Address Registers
L	L	L	L	L	L	L	L	H	X	X	H	H	Int'l Decode			Internal Test Registers
L	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	H	X	← Internal Decode →													TMS38020 ROM

test mode

The TMS38020 features a module-in-place test mode for board-level testing with the TMS38020 in-circuit. This facilitates testing by bed-of-nails testers. This test mode is enabled by tying the $\overline{\text{PHTEST}}$ pin (pin 41) to ground and supplying clock inputs LBCLK1 and LBCLK2 per the timing requirements specification. This has the effect of driving all outputs of the TMS38020 to a high-impedance state. When not used for testing purposes, this pin should be left unconnected. An internal pullup drives this pin high when not externally connected.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range (see Note 2) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to V_{SS}.
2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 80°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage (Note 3)			0		V
V_{IH}	High-level input voltage	LBCLK1, LBCLK2	3.8			V
		RCVR, RCLK	2.6			V
		$\overline{\text{PHTEST}}$	V_{CC}			V
		All other inputs	2			V
V_{IL}	Low-level input voltage	LBCLK1, LBCLK2, RCVR, RCLK			0.6	V
		$\overline{\text{PHTEST}}$			V_{SS}	V
		All other inputs			0.8	V
I_{OH}	High-level output current	All outputs			0.15	mA
I_{OL}	Low-level output current	DRVR			−1.2	mA
		LBRDY			−2.4	mA
		All other outputs			−1.7	mA
C_L	Load capacitance	DRVR			30	pF
		All other outputs			100	pF
T_A	Operating free-air temperature (Note 2)		0		70	°C

NOTES: 2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 80°C.
3. Care should be taken by PC board designers to provide a minimum inductance path between the V_{SS} pins and system ground in order to minimize V_{SS} noise.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OH} = 0.15 mA	2.4			V
V_{OL}	Low-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OL} = Max			0.45	V
I_{OH}	High-level output current	All outputs	V_{CC} = 4.75 V, V_{OH} = 2.4 V			0.15	mA
I_{OL}	Low-level output current	DRVR	V_{CC} = 4.75 V, V_{OL} = 0.45 V			−1.2	mA
		LBRDY				−2.4	mA
		All other outputs				−1.7	mA
I_{OZL}	Off-state (high-impedance state) output current with low-level voltage applied, outputs only		V_O = 0.45 V			−50	μA
I_{OZH}	Off-state (high-impedance state) output current with high-level voltage applied, outputs only		V_O = 2.4 V			50	μA
I_{IL}	Low-level input current	$\overline{PHTEST}$ (Note 4)	V_I = V_{SS}, V_{CC} at 4.75 V – 5.25 V			−700	μA
		All other inputs				−20	μA
I_{IH}	High-level input current	All inputs except $\overline{PHTEST}$ (Note 5)	V_{CC} at 4.75 V – 5.25 V			20	μA
I_{CC}	Supply current		V_{CC} = 5 V, T_A = 25°C		110		mA
			V_{CC} = 5.25 V, T_A = 0°C			175	mA
			V_{CC} = 5.25 V, T_C = 80°C			125	mA
C_I	Input capacitance	LBCLK1, LBCLK2	f = 1 MHz, all other inputs at 0 V			20	pF
		RCVR, RCLK				10	pF
		All other inputs				15	pF

NOTES: 4. $\overline{PHTEST}$ has an internal pullup resistor implemented. It may be left unconnected; in this case it is interpreted as high.
5. I_{IH} for $\overline{PHTEST}$ is not specified because it will never be driven.

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LAN ADAPTER BUS CLOCK PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range (see Figure 6)

	PARAMETER	MIN	MAX	UNIT
$t_{c(LA)}$	LAN Adapter bus cycle time (Note 6)	333	333.7	ns
t_{d1}	Delay time, LBCLK2 low to LBCLK2 no longer low in next cycle	4Q − 2	4Q + 2	
t_{d2}	Delay time, LBCLK2 rise to LBCLK2 high in next cycle		4Q + 9	
t_{d3}	Delay time, LBCLK2 no longer low to LBCLK1 no longer low	Q − 3	Q + 3	
t_{d4}	Delay time, LBCLK2 rise to LBCLK1 high		Q + 9	
t_{d5}	Delay time, LBCLK2 no longer low to LBCLK2 no longer high	2Q − 2	2Q + 7	
t_{d6}	Delay time, LBCLK2 rise to LBCLK2 low		2Q + 12	
t_{d7}	Delay time, LBCLK2 no longer low to LBCLK1 no longer high	3Q − 15	3Q − 1	
t_{d8}	Delay time, LBCLK2 rise to LBCLK1 low		3Q	
t_{d9}	Delay time, LBCLK1 low to LBCLK2 high	Q		
t_{d10}	Delay time, LBCLK2 high to LBCLK1 high	Q − 4		
t_{d11}	Delay time, LBCLK1 high to LBCLK2 low	Q − 4		
t_{d12}	Delay time, LBCLK2 low to LBCLK1 low	Q − 16		

NOTES: 6. The LAN Adapter bus cycle time is 333.3 ns ± 0.1%. This value shall be used for calculations requiring the time between successive rising edges of LBCLK2.

7. $Q = 0.25\ t_{c(LA)}$.

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LAN ADAPTER BUS READ AND WRITE PARAMETERS

timing requirements/switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 6)

	PARAMETER	MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q – 50		
t_{d17}	Delay time, address valid to LAL no longer high	Q – 50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q + 74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q + 84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q + 47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q + 47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q – 12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q – 70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q – 4		
t_{su1}	Setup time, read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q – 41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q – 21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

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†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master (DMA). The values given are valid for both modes.

NOTE 7: Q = $0.25t_c$(LA).

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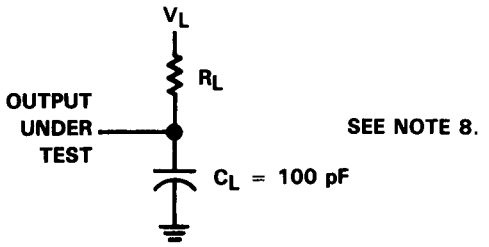
PARAMETER MEASUREMENT INFORMATION



NOTE 8: R_L and V_L are chosen as follows:

$$R_L = \frac{V_{OH} - V_{OL}}{|I_{OL} - I_{OH}|} \qquad V_L = V_{OH} - (I_{OH})(R_L)$$

FIGURE 6. LOAD CIRCUIT

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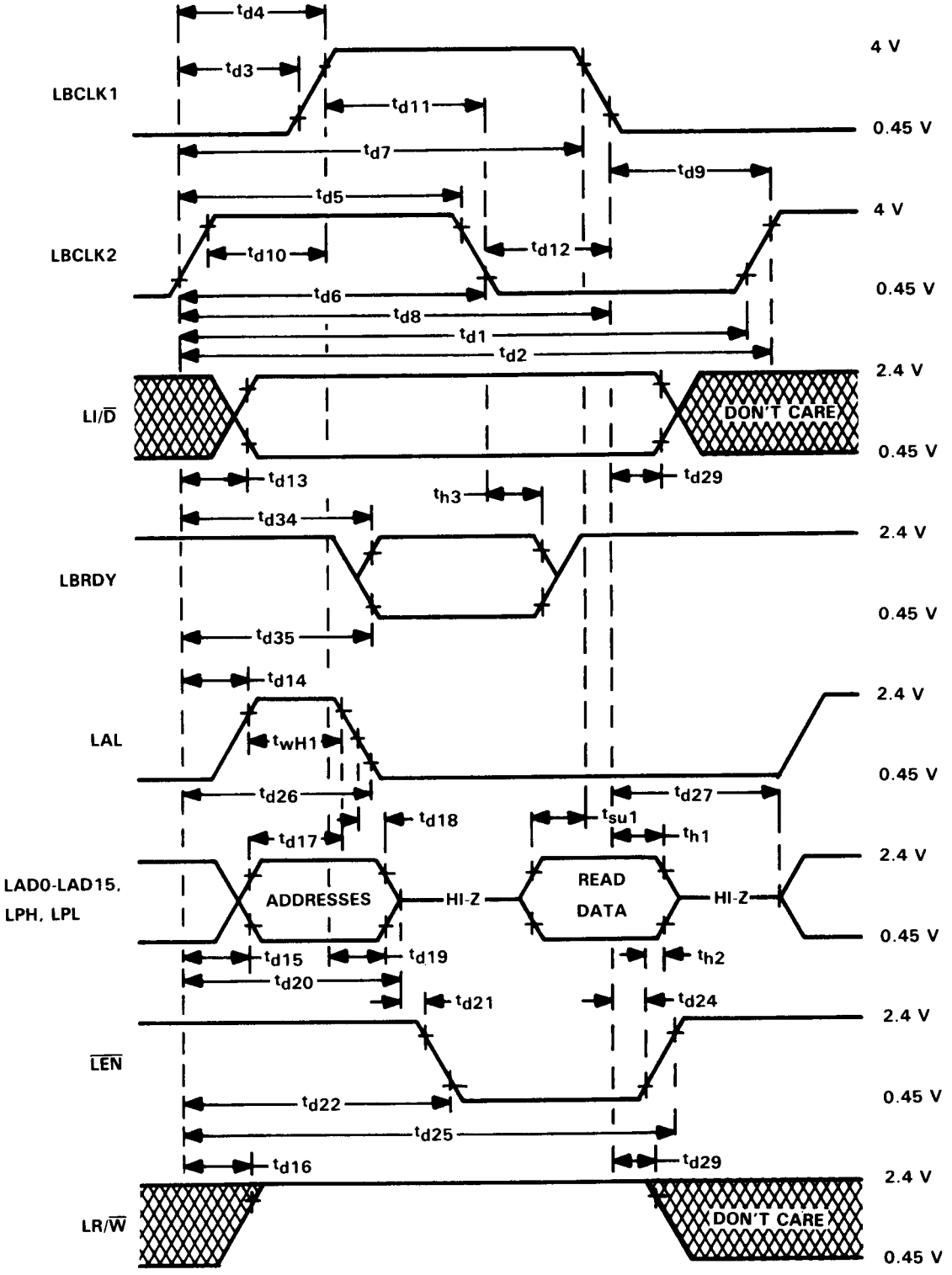
LAN Adapter bus read timing



NOTE 9: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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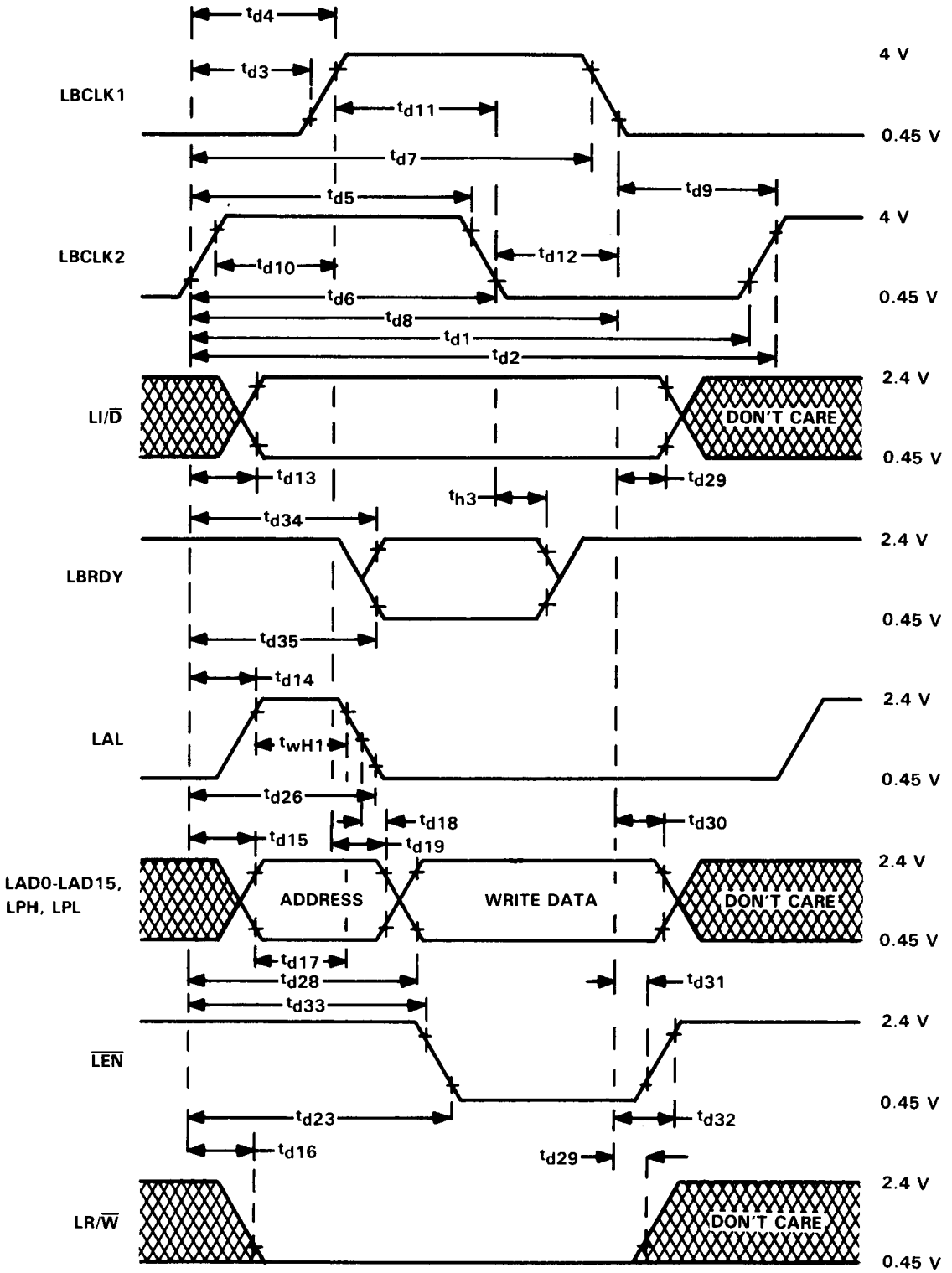
LAN Adapter bus write timing



NOTE 9: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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LAN ADAPTER BUS ARBITRATION PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 6)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay of $\overline{\text{LBRQP}}$ from LBCLK1 low		48	ns
t_{d37}	Delay of $\overline{\text{LBRQP}}$ after LBCLK1 high	0		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer high impedance by TMS38020	2Q – 9		
t_{d39}	Delay time, LBCLK2 rise to LAL driven low by TMS38020		3Q – 15	
t_{d40}	Delay time, LBCLK1 low to $\overline{\text{LEN}}$ no longer high impedance by TMS38020	80		
t_{d41}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ driven high by TMS38020		74	
t_{d42}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL no longer high impedance by TMS38020	80		

NOTE 7: Q = 0.25 t_c(LA).

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d43}	Delay time, LBCLK2 rise to $\overline{\text{LBGRP}}$ valid		2Q – 73	ns
t_{d44}	Delay time, LBCLK2 rise to $\overline{\text{LBGRP}}$ no longer valid	– 6		
t_{d45}	Delay time, LBCLK2 rise to LAL no longer driven low from old bus master	3Q – 15		
t_{d46}	Delay time, LBCLK2 rise to LAL high impedance from old bus master		4Q – 2	
t_{d47}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ high impedance from old bus master		74	
t_{d48}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$ LAD0-LAD15, LPH, and LPL high impedance from old bus master		80	

NOTE 7: Q = 0.25 $t_{c(LA)}$.

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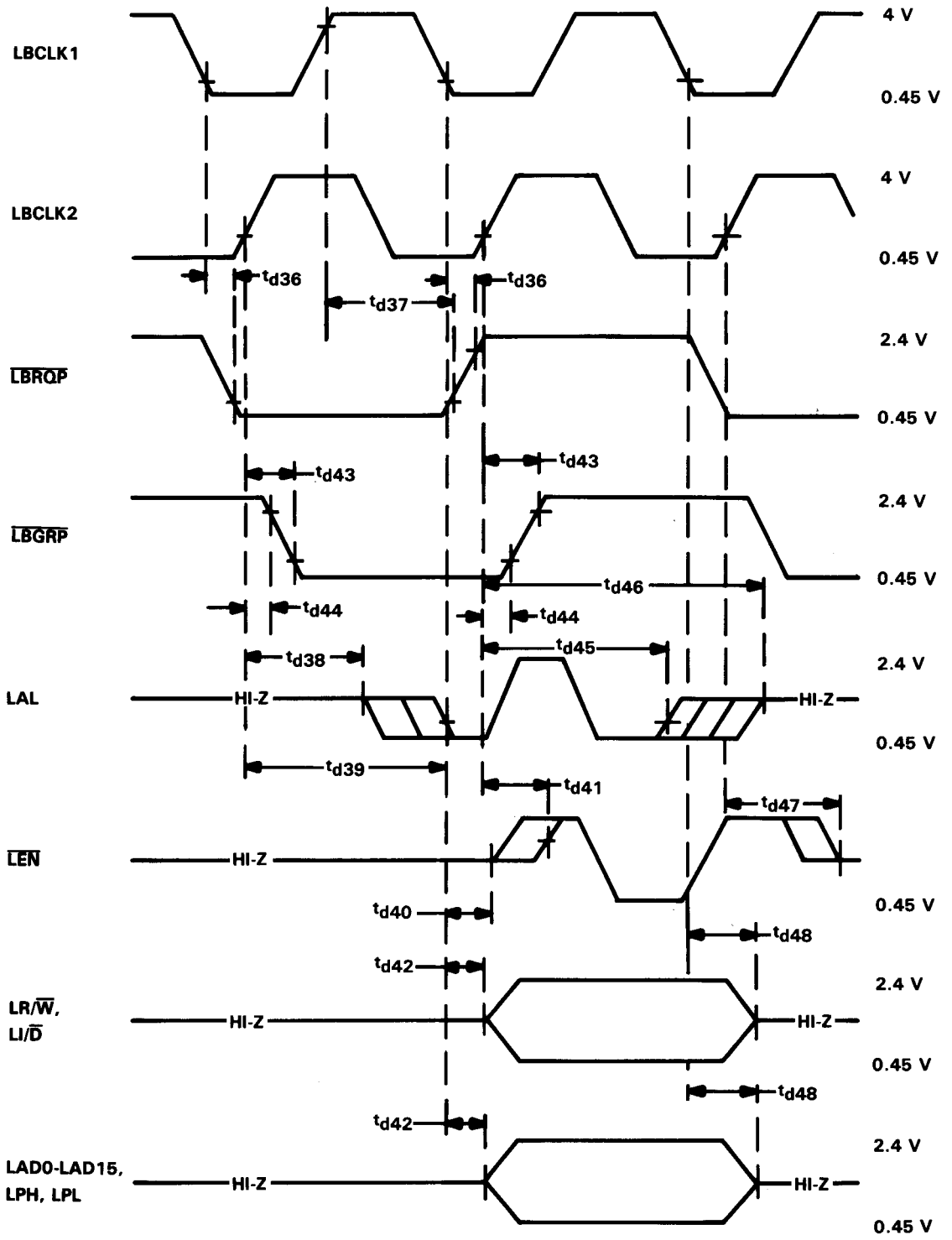
LAN Adapter bus arbitration



NOTE 10: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

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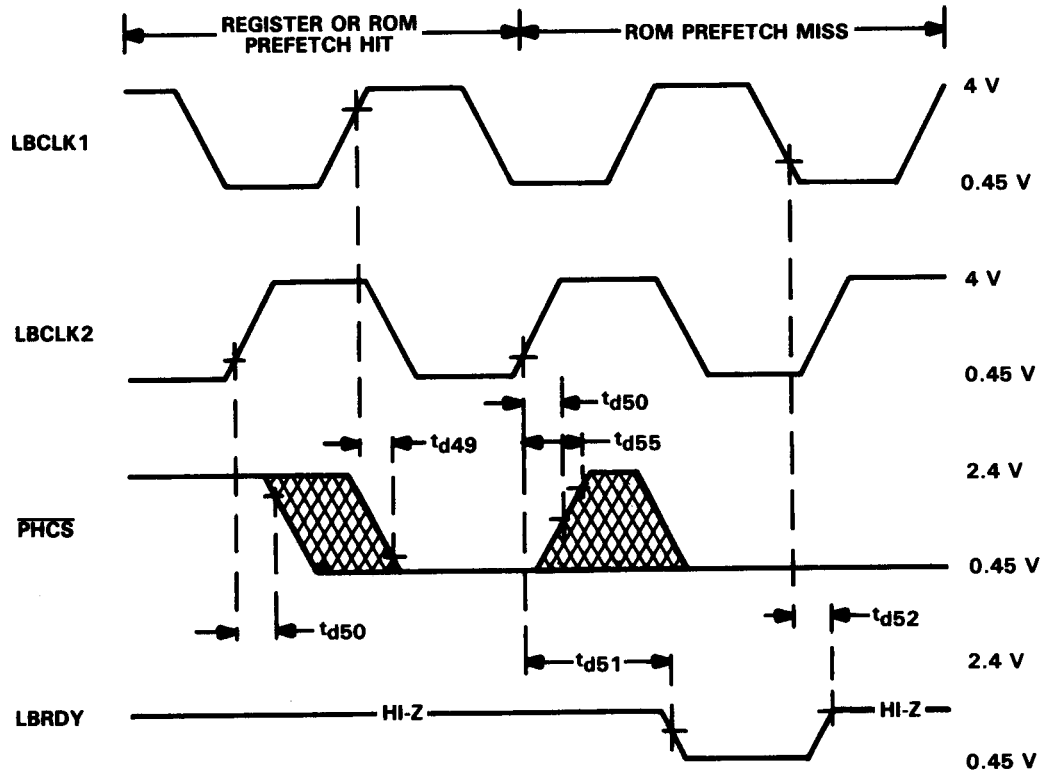
MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d49}	Delay time, LBCLK1 high to $\overline{PHCS}$ low		10	ns
t_{d50}	Delay time, LBCLK2 rise to $\overline{PHCS}$ no longer valid	0		
t_{d51}	Delay time, LBCLK2 rise to LBRDY driven low in ROM prefetch miss		145	
t_{d52}	Delay time, LBCLK1 low to LBRDY high impedance after ROM prefetch miss		45	
t_{d53}	Delay time, LBCLK2 rise to $\overline{PIRQ}$ valid		60	
t_{d54}	Delay time, LBCLK2 rise to $\overline{PIRQ}$ no longer valid	0		
t_{d55}	Delay time, LBCLK2 rise to $\overline{PHCS}$ high		Q-3	

NOTE 7: Q = 0.25 $t_{c(LA)}$.

$\overline{PHCS}$ and LBRDY timing



NOTE 10: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

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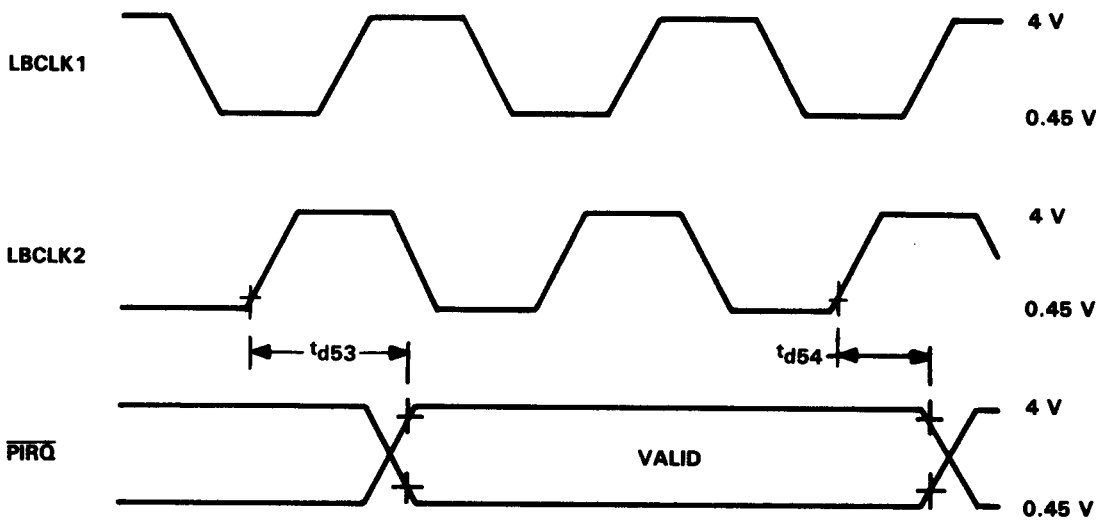
interrupt timing

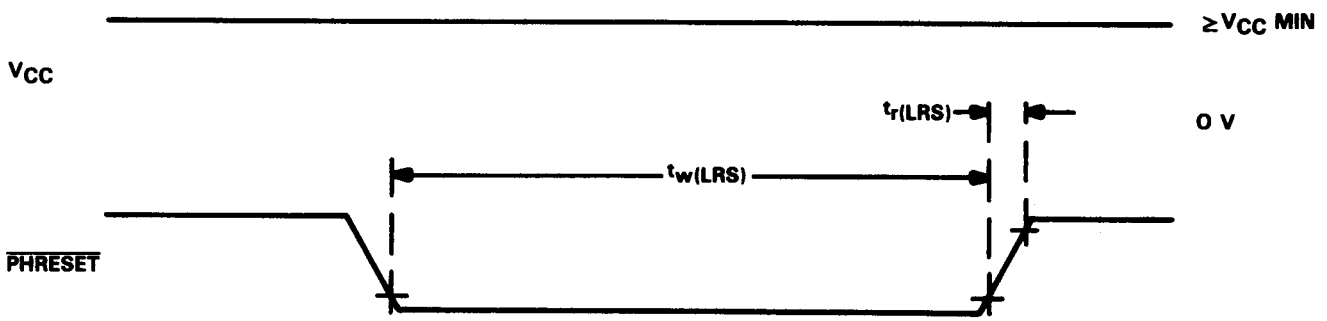


MISCELLANEOUS TIMING PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
$t_{w(LRS)}$	$\overline{\text{PHRESET}}$ pulse duration, asserted with minimum V_{CC} or greater applied	14		μs
$t_{r(LRS)}$	$\overline{\text{PHRESET}}$ rise time		100	ns
$t_{r(VCC)}$	V_{CC} rise time from 1.2 V to V_{CC} minimum	1		ms
t_{d56}	Delay from reading minimum V_{CC} during power-up to valid LBCLK1, LBCLK2 with $\overline{\text{PHRESET}}$ active		90	ms

$\overline{\text{PHRESET}}$ timing



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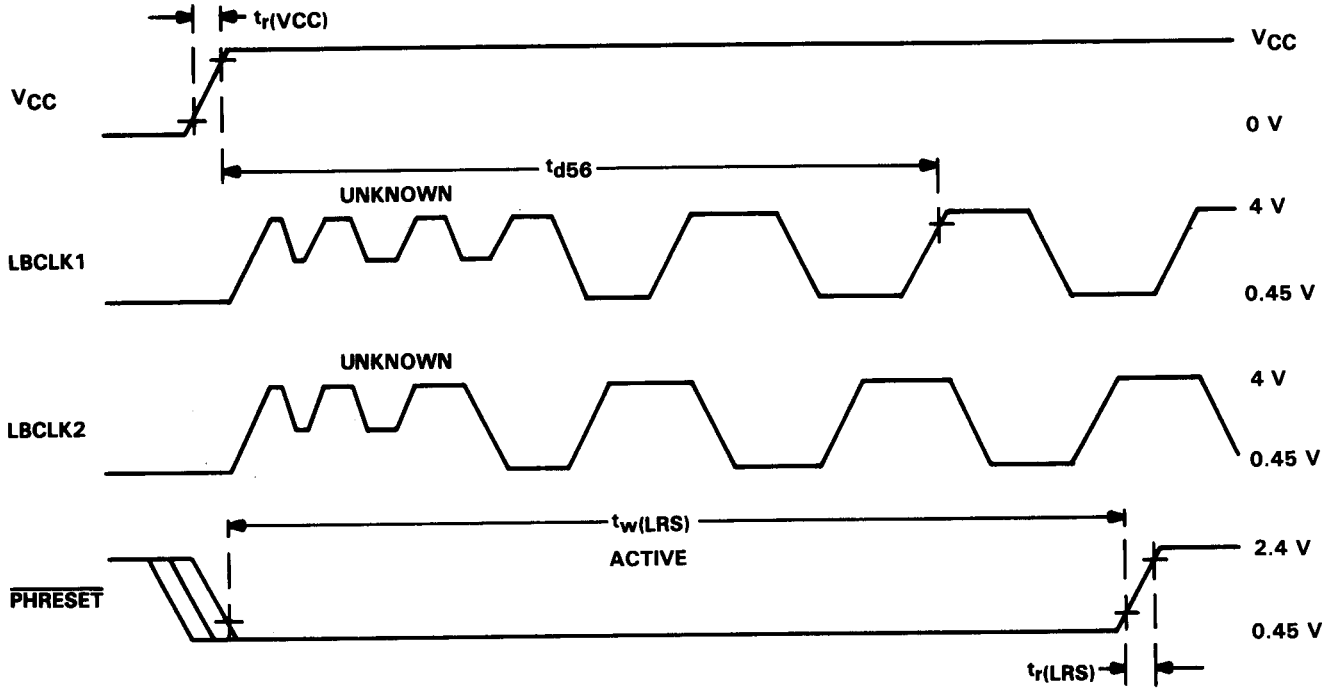
power-up, LBCLK, and $\overline{\text{PHRESET}}$ timing



NOTE 11: The timing reference points for V_{CC} are 4.5 V and 1.2 V. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for $\overline{\text{PHRESET}}$ are 2 V and 0.8 V.

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RING INTERFACE TIMING PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
$t_{c(RC)}$	RCLK cycle time (Note 14)	124.875	125.125	ns
$t_{c(PX)}$	PXTALIN cycle time	124.875	125.125	
$t_{w(RCL)}$	Pulse duration, RCLK and PXTALIN low (Notes 15, 16, 17)	46		
$t_{w(RCH)}$	Pulse duration, RCLK and PXTALIN high (Notes 15, 16, 17)	35		
$t_{su(RCVR)}$	Setup time, RCVR valid before RCLK no longer low	20		
$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK high	20		
$t_{t(RC)}$	Transition time, RCLK and PXTALIN		16	

NOTES: 14. The nominal value for $t_{c(RC)}$ is 125 ns ± 0.1%.
15. The nominal value for $t_{w(RCL)}$ and $t_{w(RCH)}$ is 62.5 ns.
16. RCVR and RCLK are driven to a high level of 2.8 V and a low level of 0.45 V during parametric tests. Timing parameters are measured from a high level of 2.6 V and a low level of 0.6 V except where shown otherwise.
17. PXTALIN is driven to a high level of 2.4 V and a low level of 0.45 V during parametric tests. Timing parameters are measured from a high level of 2 V and a low level of 0.8 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
$t_{h(DRVR)}$	Hold time, DRVR after RCLK or PXTALIN to 1.5 V level (Note 18)	12		ns
$t_{d(DRVR)}$	Delay time, RCLK or PXTALIN at 1.5 V level to DRVR at 1.5 V (Note 18)		40	
$t_{d(TRAN)}$	Delay time, data transition on DRVR ($t_{d(DRVR)} - t_{h(DRVR)}$)		5	

NOTE 18: Timing parameters of DRVR are measured from a 1.5 V level on RCLK or PXTALIN to a 1.5 V level on DRVR.

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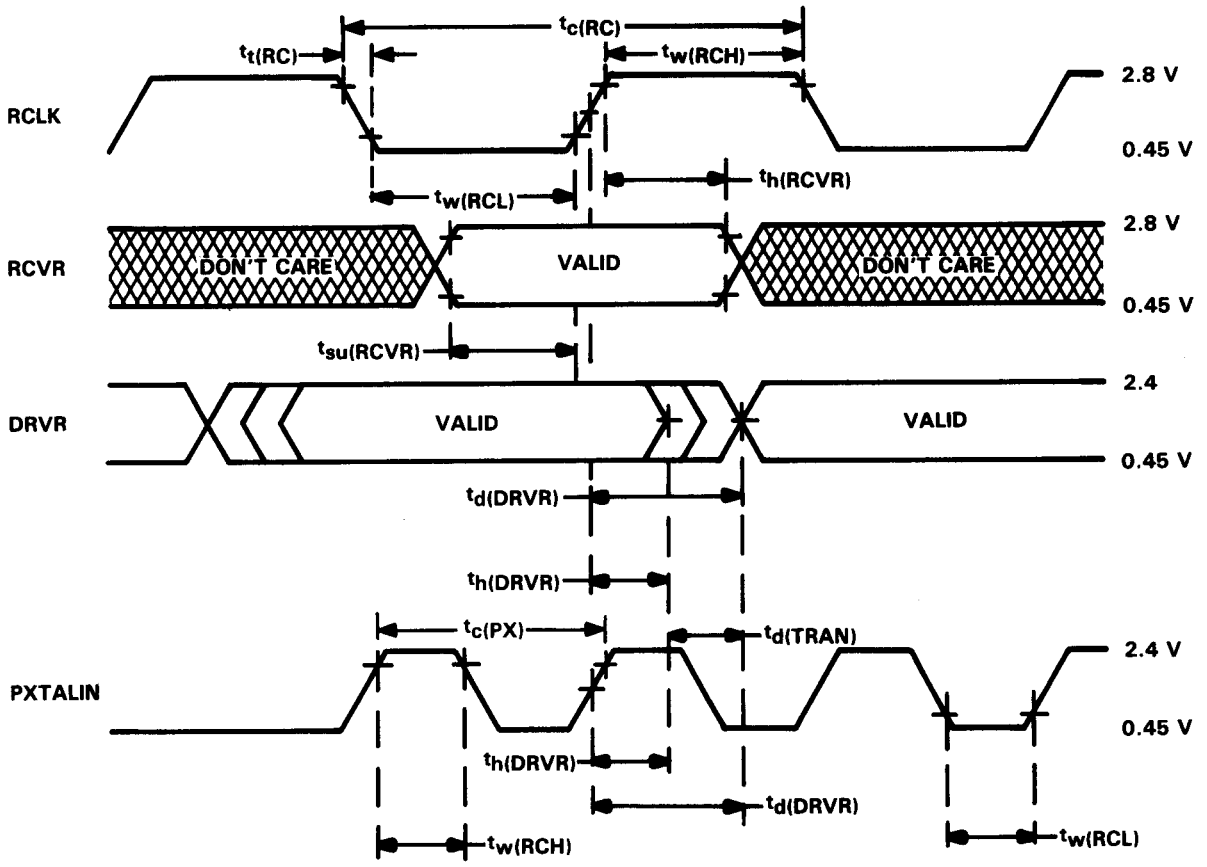
ring interface timing



NOTE 19: The timing reference points for RCVR and RCLK are 2.6 V and 0.6 V. The timing reference points for PXTALIN are 2 V and 0.8 V. The intermediate reference point for RCLK and DRVR is 1.5 V.

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