April 26, 2012

TEXAS INSTRUMENTS

DS90C185

Low Power 1.8V FPD-Link (LVDS) Serializer

General Description

The DS90C185 is a Low Power Serializer for portable battery powered applications that reduces the size of the RGB interface between the host GPU and the Display.

24 bit RGB plus three video control signals are serialized and translated to LVDS compatible levels and sent as a 4 data + clock (4D+C) reduced width LVDS compatible interface. The LVDS Interface is compatible with FPD-Link (1) deserializers and many LVDS based displays. These interfaces are commonly supported in LCD modules with “LVDS” or FPD-Link / FlatLink single-pixel input interfaces.

Displays up to 1400 x 1050 @ 60 fps are supported with 24bpp in color depth. 18bpp may also be supported by a dedicated mode with a 3D+C output. Power Dissipation is minimized by the full LVCMOS design and 1.8V powered core and V_{DDIO} rails.

The DS90C185 is offered in the small 48 pin QFN package and features single 1.8V supply operation for minimum power dissipation (50mW typ).

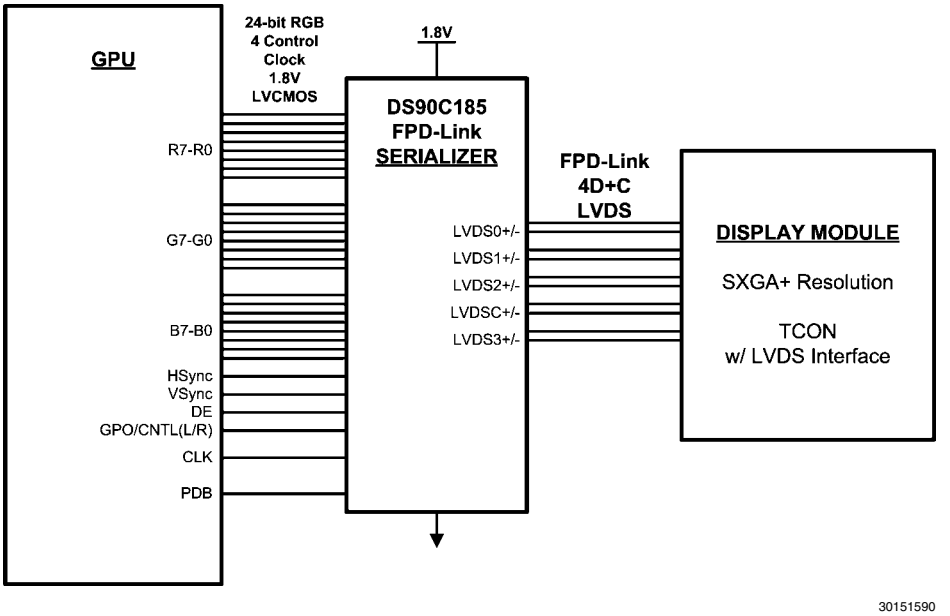
Features

- Typical power 50mW @ 75 MHz pclk
- Drives up to 1400 x 1050 @ 60 Hz (SXGA+) Displays
- 2.94 Gbps of throughput
- Two operating modes: 24 bit and 18 bit RGB
- 25 to 105 MHz Pixel Clock support
- Single 1.8V Supply
- Sleep Mode
- Spread Spectrum Clock compatibility
- Small 6mm x 6mm x 0.8mm QFN package

Applications

- eBooks
- Media Tablet Devices
- Netbooks
- Portable Display Monitors

System Diagram

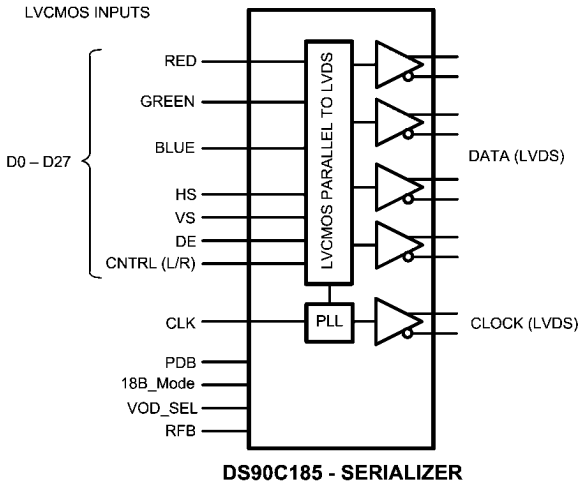


30151590

Ordering Information

Order Number	Package Description	Package ID	Supplied As
DS90C185SQE/NOPB	48–pin LLP, 6.0 x 6.0 x 0.8 mm, 0.4 mm pitch	SQF48A	250 units on Tape and Reel
DS90C185SQ/NOPB	48–pin LLP, 6.0 x 6.0 x 0.8 mm, 0.4 mm pitch	SQF48A	1000 units on Tape and Reel
DS90C185SQX/NOPB	48–pin LLP, 6.0 x 6.0 x 0.8 mm, 0.4 mm pitch	SQF48A	2500 units on Tape and Reel

Functional Block Diagram



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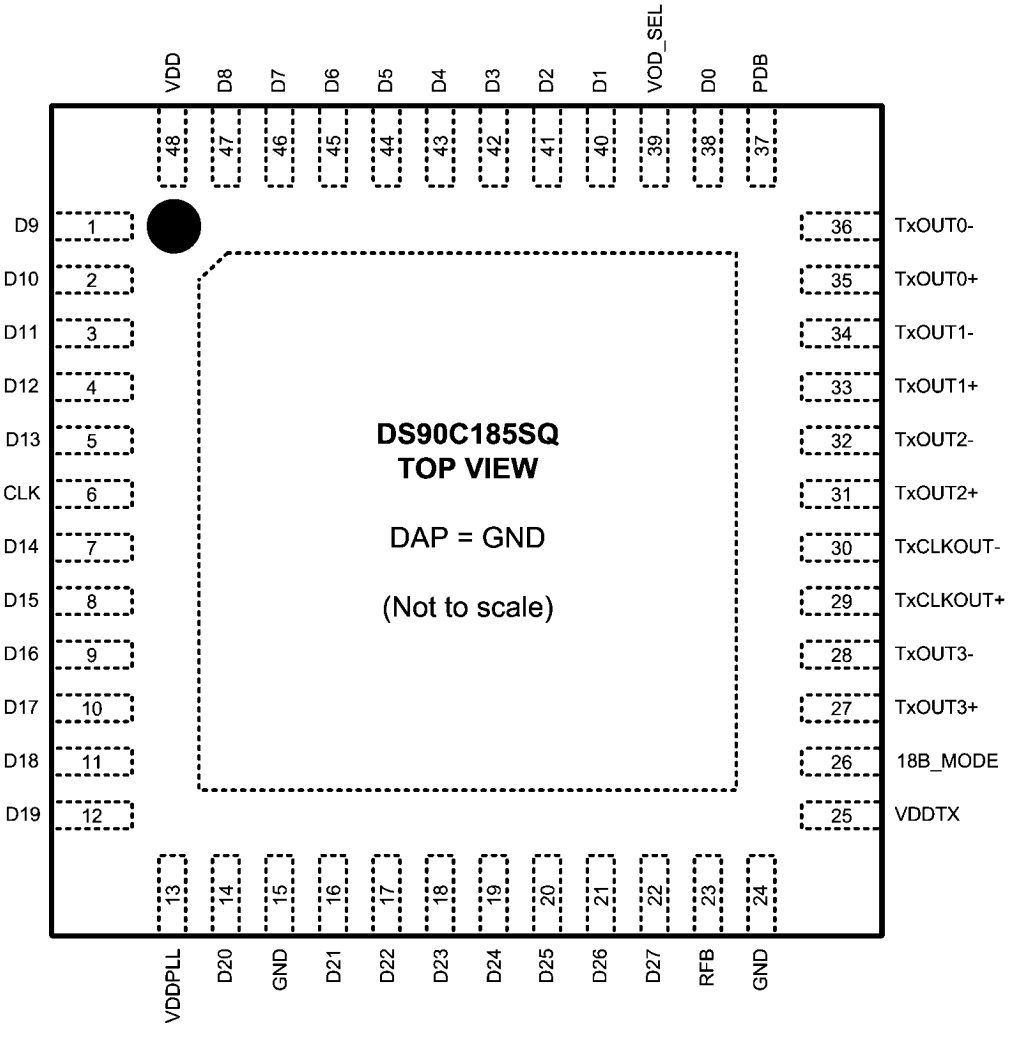
Connection Diagram



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DS90C185 Pin Descriptions

Pin Name	I/O	No.	Description
1.8 V LVCMOS VIDEO INPUTS			
D27 – D21, D20, D19 – D14, D13 – D9, D8 – D1, D0	I	22 – 16, 14, 12 – 7, 5 – 1, 47 – 40, 38	Data input pins. This includes: 8 Red, 8 Green, 8 Blue, and 3 video control lines and a general purpose or L/R control bit. Includes pull down.
CLK	I	6	Clock input. Includes pull down.
LVDS VIDEO OUTPUTS			
TxOUT0 –/+, TxOUT1 –/+, TxOUT2 –/+, TxOUT3 –/+,	O	36, 35 34, 33 32, 31 28, 27	LVDS Output Data — Expects 100 Ω DC load.
TxCLK OUT -/+	O	30, 29	LVDS Output Clock — Expects 100 Ω DC load.
1.8 V LVCMOS CONTROL INPUTS			
R_FB	I	23	LVCMOS level programmable strobe select 1 = Rising Edge Clock 0 = Falling Edge Clock — default Includes pull down.
18B_Mode	I	26	Mode Configuration Input 1 = 3D+C (18 bit RGB mode) 0 = 4D+C (24 bit RGB mode) — default Includes pull down.
VOD_SEL	I	39	VOD Select Input 1 = Reduced V_{OD} (lower power) 0 = Normal V_{OD} — default Includes pull down.
PDB	I	37	Power Down Bar(Sleep) Input 1 = ACTIVE 0 = Sleep State (low power idle) — default Includes pull down.
POWER and GROUND			
VDD	P	48	Digital power input
VDDTX	P	25	LVDS driver power input
VDDPLL	P	13	PLL power input
GND	G	15, 24	Ground pins
DAP	G		Connect DAP to ground plane

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +2.5V
LVCMOS Input Voltage	−0.5V to (V_{DD} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{DD} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C
Package Derating: θ_{JA}	26.6 °C/W above +22°C

ESD Ratings

HBM	>4kV
CDM	>1.25kV
MM	>250V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD})	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)	−10	+22	+70	°C
Supply Noise Voltage (V_{DD})			<90	mV_{PP}
Differential Load Impedance	80	100	120	Ω
Input Clock Frequency	25		105	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			0.65 * V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		0.35*V_{DD}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DD} = 1.71 V to 1.89 V		−10	±1	+10	µA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω *Figure 3*	VODSEL = H	160 (320)	300 (600)	450 (900)	mV (mV_{P-P})
			VODSEL = L	115 (230)	180 (360)	300 (600)	mV (mV_{P-P})
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L = 100Ω				50	mV
V_{OS}	Offset Voltage			0.8	0.9	1.0	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					50	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−45	−35	−25	mA
I_{OZ}	Output LVDS Driver Power Down Current	PDB = 0V			±1	±10	mA
SERIALIZER SUPPLY CURRENT							
I_{DDT1}	Serializer Supply Current Worst Case	Checkerboard pattern, R_L = 100Ω, 18B_MODE = L, VOD_SEL = H, VDD = 1.89 *Figure 1*	f = 105 MHz		60	85	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{DDTG}	Serializer Supply Current 16 Grayscale	R_L = 100Ω, 18B_MODE = L, VOD_SEL = L, VDD = 1.8 16 Grayscale Pattern	f = 75 MHz		31		mA
		R_L = 100Ω, 18B_MODE = L, VOD_SEL = H, VDD = 1.8 16 Grayscale Pattern			41		mA
		R_L = 100Ω, 18B_MODE = H, VOD_SEL = L, VDD = 1.8 16 Grayscale Pattern			28		mA
		R_L = 100Ω, 18B_MODE = H, VOD_SEL = H, VDD = 1.8 16 Grayscale Pattern			36		mA
I_{DDTP}	Serializer Supply Current PRBS-7	R_L = 100Ω, 18B_MODE = L, VOD_SEL = L, VDD = 1.8 PRBS-7 Pattern	f = 75 MHz *Figure 11*		33		mA
		R_L = 100Ω, 18B_MODE = L, VOD_SEL = H, VDD = 1.8 PRBS-7 Pattern			45		mA
		R_L = 100Ω, 18B_MODE = H, VOD_SEL = L, VDD = 1.8 PRBS-7 Pattern			29		mA
		R_L = 100Ω, 18B_MODE = H, VOD_SEL = H, VDD = 1.8 PRBS-7 Pattern			38		mA
I_{DDZ}	Serializer Power Down Current				18	200	µA

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time *(Figure 5)*	1.0		6.0	ns
TCIP	TxCLK IN Period *(Figure 6)*	9.52	T	40	ns
TCIH	TxCLK IN High Time *(Figure 6)*	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 6)*	0.35T	0.5T	0.65T	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 4*(Note 5)*)*			0.18	0.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 4*(Note 5)*)*			0.18	0.5	ns
TPPOS0	Transmitter Output Pulse Positions Normalized for Bit 0	f = 105 MHz ***Figure 10***		1		UI
TPPOS1	Transmitter Output Pulse Positions Normalized for Bit 1			2		UI
TPPOS2	Transmitter Output Pulse Positions Normalized for Bit 2			3		UI
TPPOS3	Transmitter Output Pulse Positions Normalized for Bit 3			4		UI
TPPOS4	Transmitter Output Pulse Positions Normalized for Bit 4			5		UI
TPPOS5	Transmitter Output Pulse Positions Normalized for Bit 5			6		UI
TPPOS6	Transmitter Output Pulse Positions Normalized for Bit 6			7		UI
ΔTPPOS	Variation in Transmitter Pulse Position (Bit 6 — Bit 0)			±0.06		UI
TSTC	Required TxIN Setup to TxCLK IN	***Figure 6***	0			ns
THTC	Required TxIN Hold to TxCLK IN		2.5			ns
TCCJ	Cycle to Cycle Jitter	f = 105 Mhz (Note 5)		0.028	0.035	UI
TSD	Serializer Propagation Delay	f = 105 MHz ***Figure 7***		2*TCIP + 10.54	2*TCIP + 13.96	ns
TCCS	TxOUT Channel to Channel Skew			110		ps
TPLLS	Transmitter Phase Lock Loop Set	***Figure 8***			1	ms
TPPD	Transmitter Power Down Delay	***Figure 9*** (Note 6)			100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 1.8 V and T_A = +22C unless specified otherwise.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Note 5: Parameter is guaranteed by characterization and is not tested at final test.

Note 6: Parameter is guaranteed by design and is not tested at final test.

AC Timing Diagrams

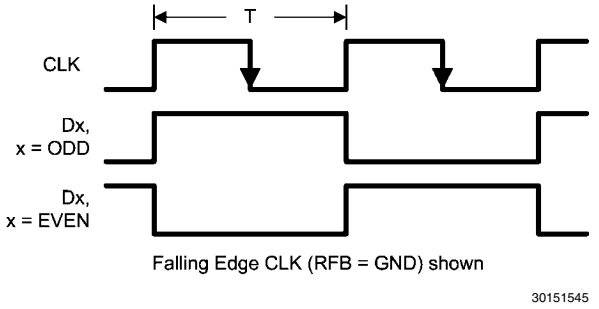


FIGURE 1. "Worst Case" Test Pattern (*Note 7*)

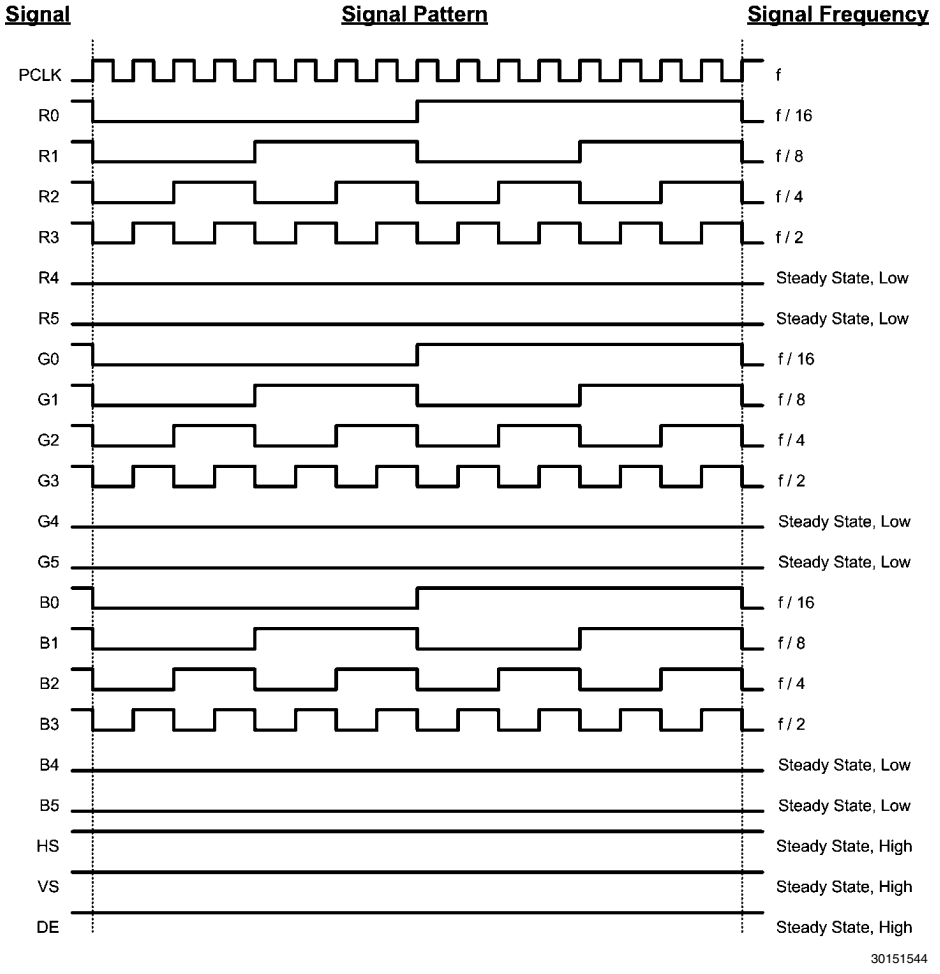


FIGURE 2. "16 Grayscale" Test Pattern - DS90C185 (*Note 8*, *Note 9*)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS I/O.

Note 8: Recommended pin to signal mapping for 18 bits per pixel, customer may choose to define differently. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: Figures 1, 2 show a falling edge data strobe (CLK).

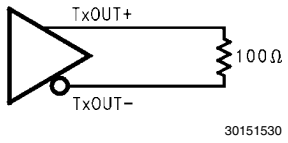


FIGURE 3. DS90C185 (Transmitter) LVDS Output Load

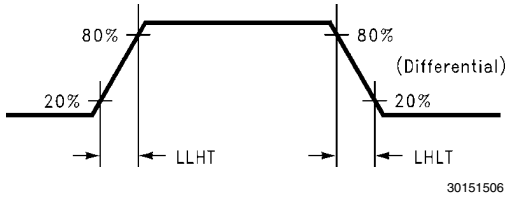


FIGURE 4. DS90C185 (Transmitter) LVDS Transition Times

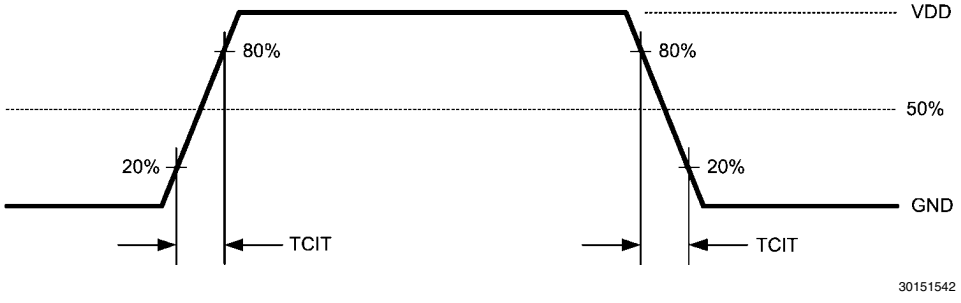


FIGURE 5. DS90C185 (Transmitter) Input Clock Transition Time

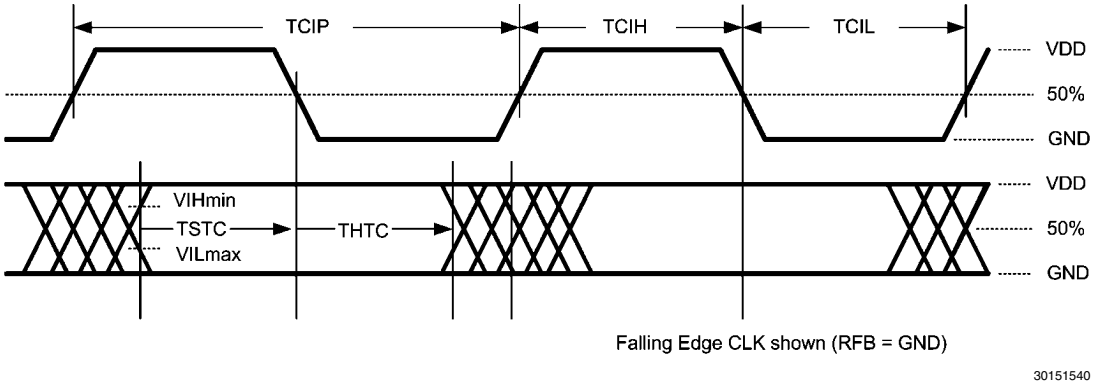


FIGURE 6. DS90C185 (Transmitter) Setup/Hold and High/Low Times with R_FB pin = GND (Falling Edge Strobe)

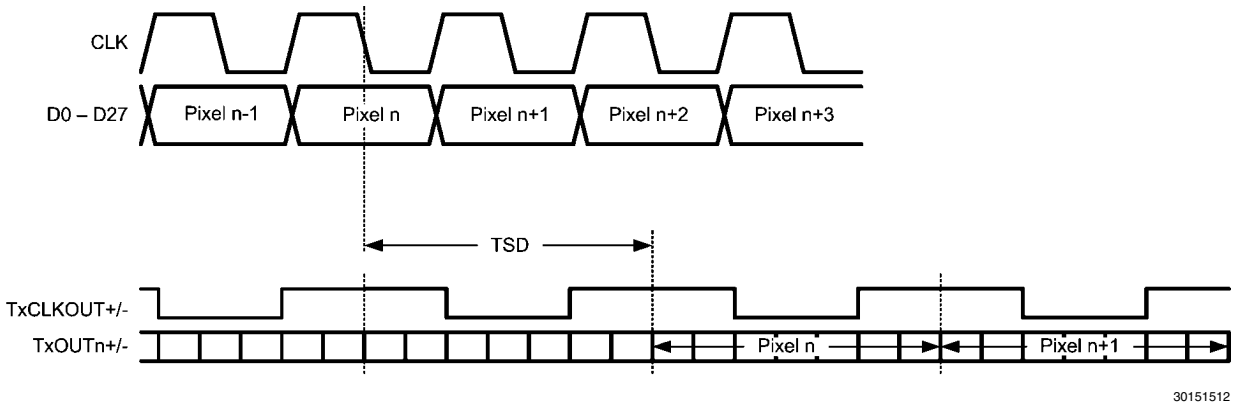


FIGURE 7. DS90C185 Propagation Delay

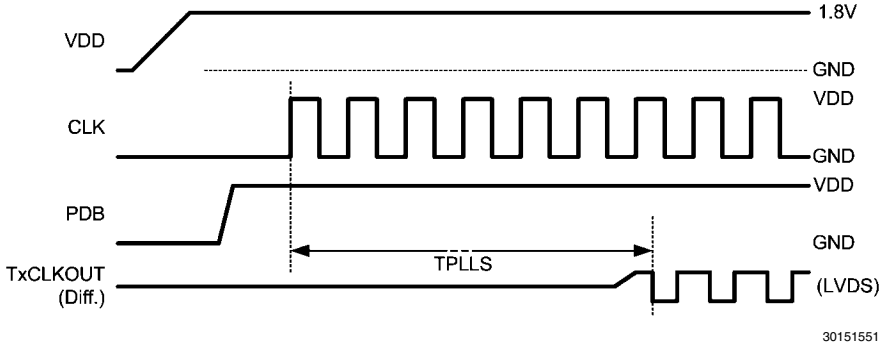


FIGURE 8. DS90C185 (Transmitter) Phase Lock Loop Set Time

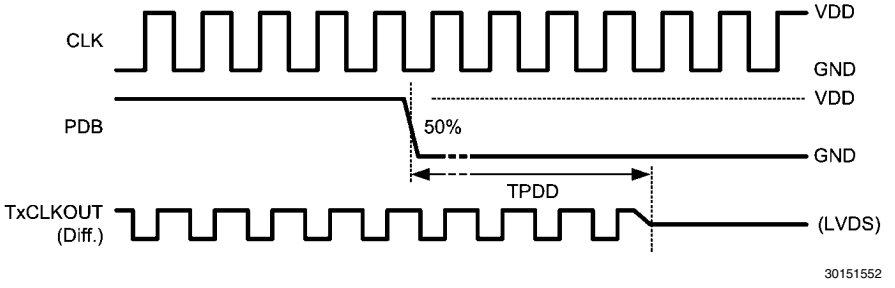


FIGURE 9. Transmitter Power Down Delay

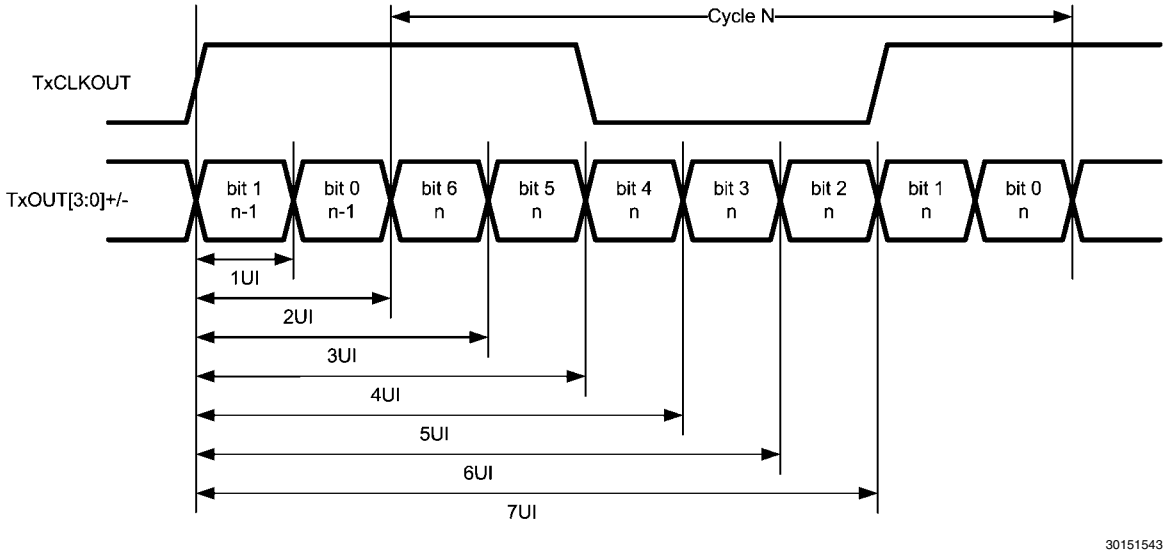


FIGURE 10. Transmitter LVDS Output Pulse Position Measurement - DS90C185

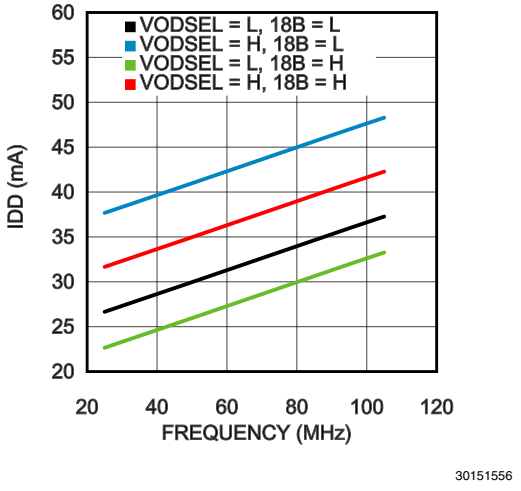


FIGURE 11. Typ Current Draw — PRBS-7 Data Pattern

LVDS Interface / TFT Color Data recommended Mapping

Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application. The DS90C185 supports single pixel interfaces with either 24bpp or 18bpp color depths.

The DS90C185 provides four LVDS data lines along with an LVDS clock line (4D+C) for the 28 LVCMOS data inputs. The 28 bit interface typically assigns 24 bits to RGB color data, 3 bits to video control (HS, VS and DE) and one spare bit can be ignored, used for L/R signaling or function as a general purpose bit. The single pixel 24bpp 4D+C LVDS interface mapping is shown *Figure 13*. A single pixel 18bpp mode is also supported by utilizing the 18B_MODE pin. In this configuration the TxOUT3 output channel is place in TRI-STATE® to save power. Its respective inputs are ignored. This mapping is shown in *Figure 12*.

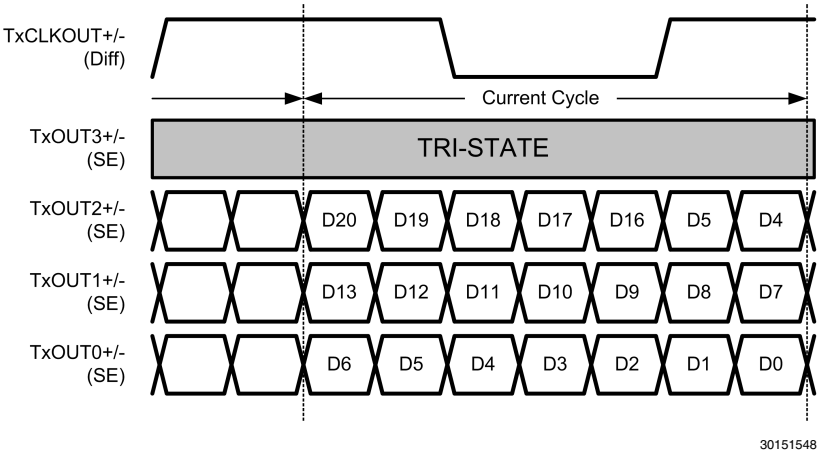


FIGURE 12. DS90C185 LVDS Map — 18B_MODE = H

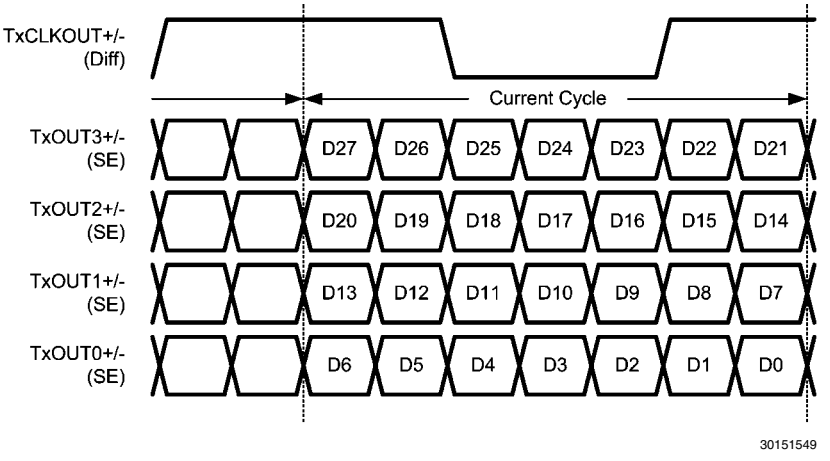


FIGURE 13. DS90C185 LVDS Map — 18B_MODE = L

COLOR MAPPING INFORMATION

A defacto color mapping is shown next. Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application.

24bpp / MSB on CH3

DS90C187 Input	Color Mapping	Note
D22	R7	MSB
D21	R6	
D5	R5	
D4	R4	
D3	R3	
D2	R2	
D1	R1	
D0	R0	LSB
D24	G7	MSB
D23	G6	
D11	G5	
D10	G4	
D9	G3	
D8	G2	
D7	G1	
D6	G0	LSB
D26	B7	MSB
D25	B6	
D17	B5	
D16	B4	
D15	B3	
D14	B2	
D13	B1	
D12	B0	
D20	DE	$\overline{\text{Data Enable}}$
D19	VS	Vertical Sync
D18	HS	Horizontal Sync
D27	GP	General Purpose

24bpp / LSB on CH3

DS90C187 Input	Color Mapping	Note
D5	R7	MSB
D4	R6	
D3	R5	
D2	R4	
D1	R3	
D0	R2	
D22	R1	
D21	R0	LSB
D11	G7	MSB
D10	G6	
D9	G5	
D8	G4	
D7	G3	
D6	G2	
D24	G1	
D23	G0	LSB
D17	B7	MSB
D16	B6	
D15	B5	
D14	B4	
D13	B3	
D12	B2	
D26	B1	
D25	B0	
D20	DE	$\overline{\text{Data Enable}}$
D19	VS	Vertical Sync
D18	HS	Horizontal Sync
D27	GP	General Purpose

18bpp

DS90C187 Input	Color Mapping	Note
D5	R5	MSB
D4	R4	
D3	R3	
D2	R2	
D1	R1	
D0	R0	LSB
D11	G5	MSB
D10	G4	
D9	G3	
D8	G2	
D7	G1	
D6	G0	LSB
D17	B5	MSB
D16	B4	
D15	B3	
D14	B2	
D13	B1	
D12	B0	
D20	DE	$\overline{\text{Data Enable}}$
D19	VS	Vertical Sync
D18	HS	Horizontal Sync

Functional Description

DS90C185 converts a wide parallel LVCMOS input bus into FPD-Link LVDS data. The device can be configured to support RGB-888 (24 bit color) or RGB-666 (18 bit color). The DS90C185 has several power saving features including: selectable VOD, 18 bit / 24 bit mode select, and a power down pin control.

In each input pixel clock cycle, data from D[27:0] is serialized and driven out on TxOUT[3:0] +/- with TxCLKOUT +/-. If 18B_MODE is LOW, then TxOUT3 +/- is powered down and the corresponding LVCMOS input signals are ignored.

The input pixel clock can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 700 Mbps (28 bits * 25MHz) to 2.94 Gbps (28 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. TxCLKOUT +/- will operate at the same rate as CLK with a duty cycle ratio of 57:43.

Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the input LVCMOS data is latched on. If RFB is HIGH, input data is latched on the RISING EDGE of the pixel clock (CLK). If RFB is LOW, the input data is latched on the FALLING EDGE of the pixel clock. Note: This can be set independently of receiver's output clock strobe.

TABLE 1. Pixel Clock Edge

RFB	Result
0	FALLING edge
1	RISING edge

Power Management

The DS90C185 has several features to assist with managing power consumption. The 18B_MODE pin allows the DS90C185 to power down the unused LVDS driver for RGB-666 (18 bit color) applications. If no clock is applied to the CLK pin, the DS90C185 will enter a low power state. To place the DS90C185 in its lowest power state, the device can be powered down by driving the PDB pin to LOW.

Sleep Mode (PDB)

The DS90C185 provides a power down feature. When the device has been powered down, current draw through the supply pins is minimized and the PLL is shut down. The LVDS drivers are also powered down with their outputs pulled to GND through 100Ω resistors.

TABLE 2. Power Down Select

PDB	Result
0	SLEEP Mode (default)
1	ACTIVE (enabled)

LVDS Outputs

The DS90C185's LVDS drivers are compatible with ANSI/TIA/EIA-644–A LVDS receivers. The LVDS drivers an output a power saving low V_{OD} or a higher V_{OD} to enable longer trace and cable lengths by configuring the VODSEL pin.

TABLE 3. VOD Select

VODSEL	Result
0	±180 mV (360mVpp)
1	±300 mV (600mVpp)

For more information regarding the electrical characteristics of the LVDS outputs, refer to the LVDS DC Characteristics and LVDS Switching Specifications.

18 bit / 24 bit Color Mode (18B)

The 18B pin can be used to further save power by powering down the 4th LVDS driver in each used bank when the application requires only 18 bit color or 3D+C LVDS. Set the 18B pin to logic HIGH to TRI-STATE® TxOUT3 +/-. For 24 bit color applications this pin should be set to logic LOW. Note that the power down function takes priority over the TRI-STATE® function.

TABLE 4. Color DepthConfigurations

18B_Mode	Result
0	24bpp, LVDS 4D+C
1	18bpp, LVDS 3D+C

LVCMOS Inputs

The DS90C185 has 28 data inputs. These inputs are typically used for 24 or 18 bits of RGB video with 1, 2 or 3 video control signal (HS, VS and DE) inputs and one spare bit that can be used for L/R signaling or function as a general purpose bit. All LVCMOS input pins are designed for 1.8V LVCMOS logic. All LVCMOS inputs, including clock, data and configuration pins have an internal pull down resistor to set a default state. If any LVCMOS inputs are unused, they can be left as no connect (NC) or connected to ground.

Applications Information

Power Up Sequence

The V_{DD} power supply pins do not require a specific power on sequence and can be powered on in any order. However, the PDB pin should only be set to logic HIGH once the power sent to all supply pins is stable. Active clock and data inputs should not be applied to the DS90C185 until all of the input power pins have been powered on, settled to the recommended operating voltage and the PDB pin has be set to logic HIGH.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (DS90C185 PDB input initially LOW):

1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Toggle DS90C185 power down pin to PDB = V_{IH}.
4. Enable video source output; start sending black video data.
5. Send >1ms of black video data; this allows the DS90C185 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (DS90C185 PDB input initially HIGH):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set DS90C185 power down pin to PDB = GND.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

Power Supply Filtering

The DS90C185 has several power supply pins at 1.8V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of at least one 0.1µF capacitor placed on each pin, with an additional 4.7µF – 22µF capacitor placed on the PLL supply pin (VDDPLL). 0.01µF capacitors are typically recommended for each pin. Additional filtering including ferrite beads may be necessary for noisy systems. It is recommended to place a 0 resistor at the bypass capacitors that connect to each power pin to allow for additional filtering if needed. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50µF — 100µF range.

Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense pcbs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the QFN (LLP) style package is provided in Application Note: AN-1187.

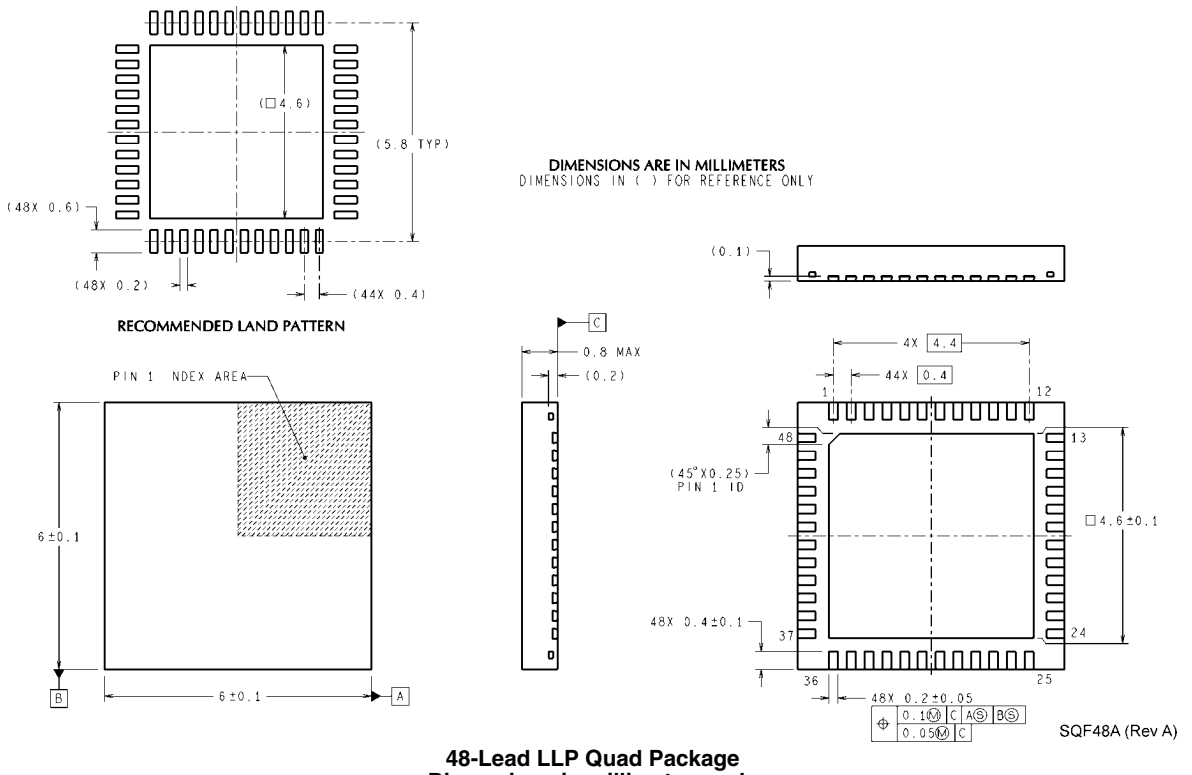
LVDS Interconnect Guidlines

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use differential connectors when above 500Mbps
- Minimize skew within the pair
- Use the S/2S/3S rule in spacings
  - — S = space between the pairs
  - — 2S = space between pairs
  - — 3S = space to LVCMOS signals
- Place ground vias next to signal vias when changing between layers
- When a signal changes reference planes, place a bypass cap and vias between the new and old reference plane

For more tips and detailed suggestions regarding high speed board layout principles, please consult the LVDS Owner's Manual at: http://www.ti.com/lvds

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead LLP Quad Package
Dimensions in millimeters only
TI Package Number SQF48A

Notes