SN54ALS640B, SN54AS640, SN74ALS640B, SN74AS640
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SDAS122A – DECEMBER 1983 – REVISED JANUARY 1995

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Inverting Logic**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54ALS640B, SN54AS640 . . . J PACKAGE
SN74ALS640B, SN74AS640 . . . DW OR N PACKAGE
(TOP VIEW)

```
        ┌───────∪───────┐
DIR  [ 1        20 ] V_CC
 A1  [ 2        19 ] OE
 A2  [ 3        18 ] B1
 A3  [ 4        17 ] B2
 A4  [ 5        16 ] B3
 A5  [ 6        15 ] B4
 A6  [ 7        14 ] B5
 A7  [ 8        13 ] B6
 A8  [ 9        12 ] B7
GND  [ 10       11 ] B8
        └───────────────┘
```

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The -1 version of the SN74ALS640B is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS640B.

The SN54ALS640B and SN54AS640 are characterized for operation over the full military temperature range of $-55°C$ to $125°C$. The SN74ALS640B and SN74AS640 are characterized for operation from $0°C$ to $70°C$.

SN54ALS640B, SN54AS640 . . . FK PACKAGE
(TOP VIEW)

```
        A2  A1  DIR V_CC OE
         3   2   1   20  19
       ┌────────────────────┐
A3 [ 4                  18 ] B1
A4 [ 5                  17 ] B2
A5 [ 6                  16 ] B3
A6 [ 7                  15 ] B4
A7 [ 8                  14 ] B5
       └────────────────────┘
         9  10  11  12  13
        A8  GND B8  B7  B6
```
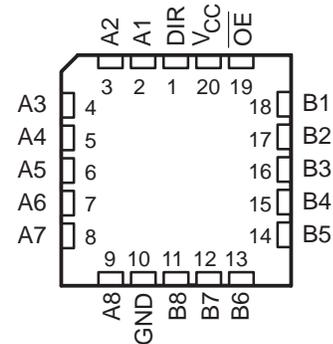
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

TEXAS INSTRUMENTS

SN54ALS640B, SN54AS640, SN74ALS640B, SN74AS640
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
SDAS122A – DECEMBER 1983 – REVISED JANUARY 1995

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
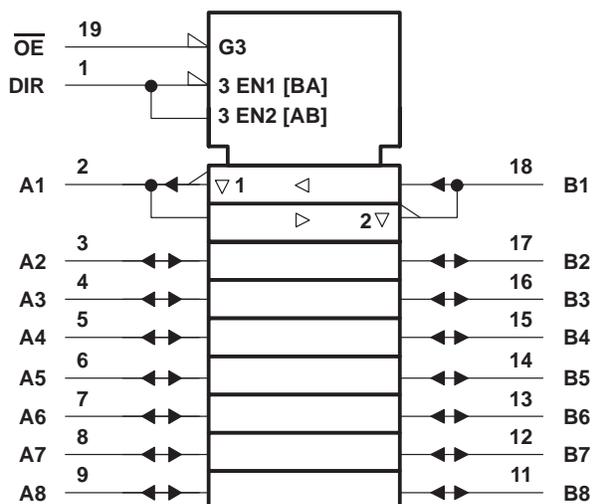
logic diagram (positive logic)

To Seven Other Transceivers

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I: All inputs .... 7 V
               I/O ports .... 5.5 V
Operating free-air temperature range, T_A: SN54ALS640B .... −55°C to 125°C
                                      SN74ALS640B .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS640B			SN74ALS640B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48§	
T_A	Operating free-air temperature	−55		125	0		70	°C

§ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SN54ALS640B, SN54AS640, SN74ALS640B, SN74AS640
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS640B			SN74ALS640B			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.5			−1.5	V
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC}-2$			$V_{CC}-2$			V
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
			$I_{OH} = -12$ mA	2						
			$I_{OH} = -15$ mA				2			
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	
			$I_{OL} = 48$ mA‡					0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5$ V	$V_I = 7$ V			0.1			0.1	mA
	A or B ports		$V_I = 5.5$ V			0.1			0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	µA
	A or B ports§					20			20	
I_{IL}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−20		−112	−30		−112	mA
I_{CC}		$V_{CC} = 5.5$ V	Outputs high		19	50		19	45	mA
			Outputs low		27	60		27	55	
			Outputs disabled		28	55		28	50	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX#				UNIT
			SN54ALS640B		SN74ALS640B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	14	2	11	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{OE}$	A or B	4	25	4	21	ns
t_{PZL}			5	27	5	24	
t_{PHZ}	$\overline{OE}$	A or B	2	12	2	10	ns
t_{PLZ}			3	20	3	15	

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

![Texas Instruments logo]

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} . . . . 7 V
Input voltage, V_I: All inputs . . . . 7 V
               I/O ports . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS640 . . . . −55°C to 125°C
                                       SN74AS640 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS640			SN74AS640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS640			SN74AS640			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2			−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -2$ mA	$V_{CC} - 2$						V
		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA				$V_{CC} - 2$			
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
			$I_{OH} = -12$ mA	2.4						
			$I_{OH} = -15$ mA				2.4			
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA		0.3	0.55				V
			$I_{OL} = 64$ mA					0.35	0.55	
I_I	Control inputs	$V_{CC} = 5.5$ V	$V_I = 7$ V			0.1			0.1	mA
	A or B ports		$V_I = 5.5$ V			0.1			0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	µA
	A or B ports[§]					70			70	
I_{IL}	Control inputs	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.5			−0.5	mA
	A or B ports[§]					−0.75			−0.75	
I_O[¶]		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−50		−150	−50		−150	mA
I_{CC}		$V_{CC} = 5.5$ V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
[¶] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]				UNIT
			SN54AS640		SN74AS640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	8	2	7	ns
t_{PHL}			1	7	2	6	
t_{PZH}	$\overline{OE}$	A or B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{OE}$	A or B	2	9	2	8	ns
t_{PLZ}			2	16	2	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

**LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

$R_L = R1 = R2$

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**
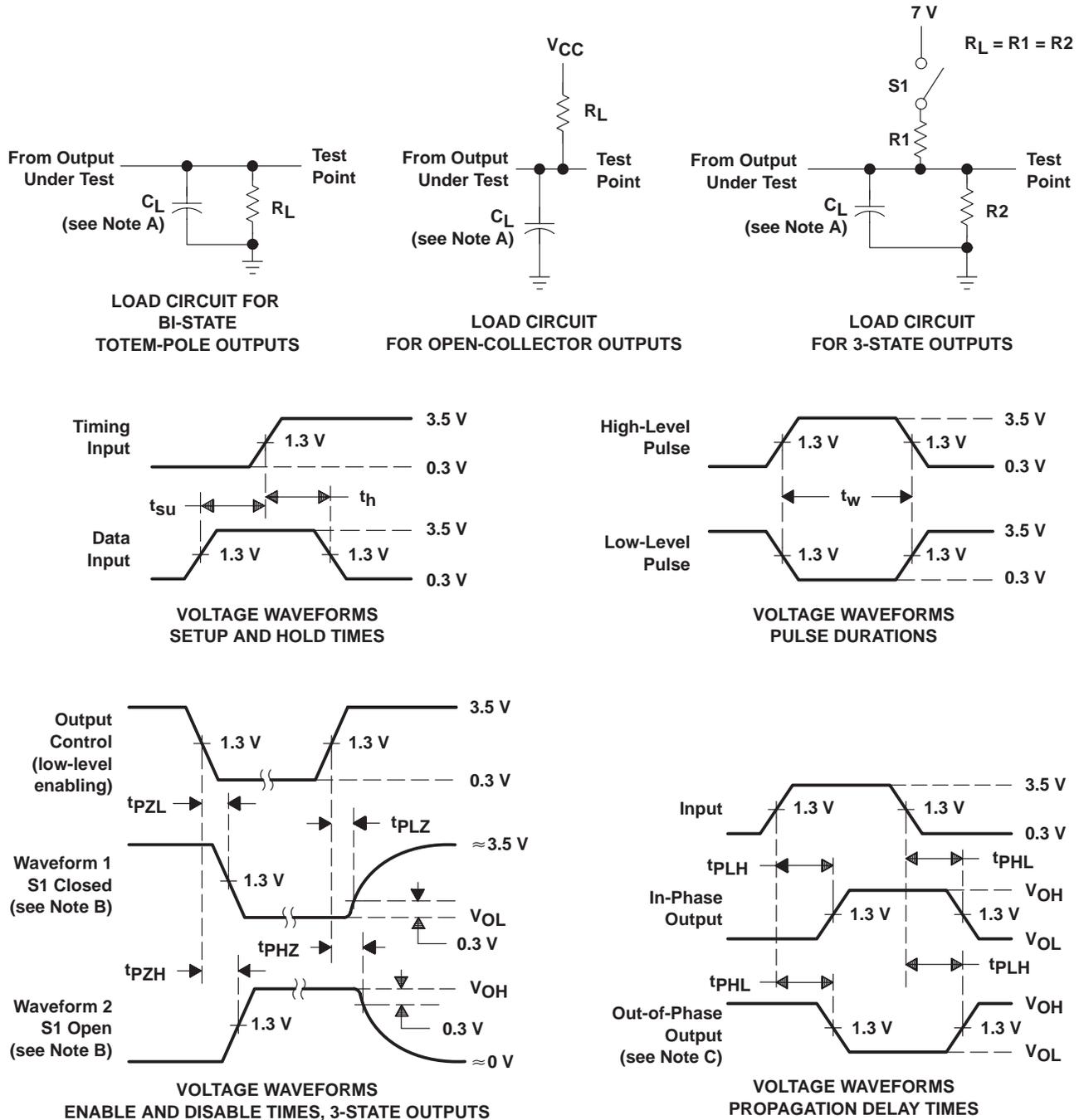
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88727012A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8872701RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701RA SNJ54ALS640BJ	Samples
5962-8872701SA	NRND	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701SA SNJ54ALS640BW	
5962-89553012A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89553012A SNJ54AS 640FK	
5962-8955301RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8955301RA SNJ54AS640J	Samples
5962-8955301SA	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
SN54ALS640BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS640BJ	Samples
SN54AS640J	NRND	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS640J	
SN74ALS640B-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640B-1DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640B-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640B-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS640B-1N	Samples
SN74ALS640B-1N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS640B-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS640B-1N	Samples
SN74ALS640B-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS640BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS640BN	Samples
SN74ALS640BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BNSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74AS640N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS640N	Samples
SN74AS640NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS640	Samples
SNJ54ALS640BFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54ALS640BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701RA SNJ54ALS640BJ	Samples
SNJ54ALS640BW	NRND	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701SA SNJ54ALS640BW	
SNJ54AS640FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89553012A SNJ54AS 640FK	
SNJ54AS640J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8955301RA SNJ54AS640J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS640B, SN54AS640, SN74ALS640B, SN74AS640 :

● Catalog: SN74ALS640B, SN74AS640

● Military: SN54ALS640B, SN54AS640

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS640B-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS640B-1NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74ALS640BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS640BNSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74AS640NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS
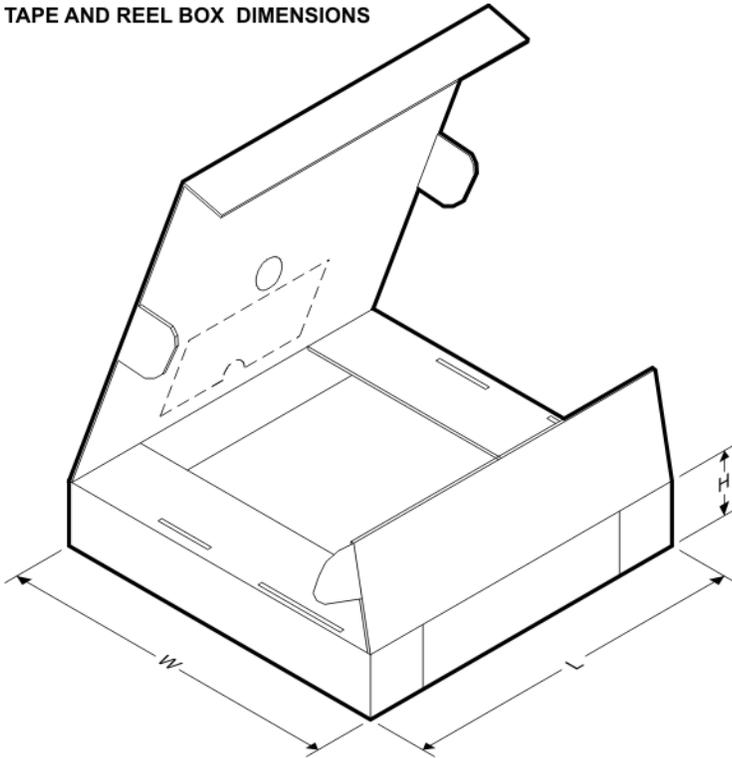
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS640B-1DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS640B-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS640BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS640BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AS640NSR	SO	NS	20	2000	367.0	367.0	45.0

DIM \ PINS **	14	16	18	20
[A]	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

[A]

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK
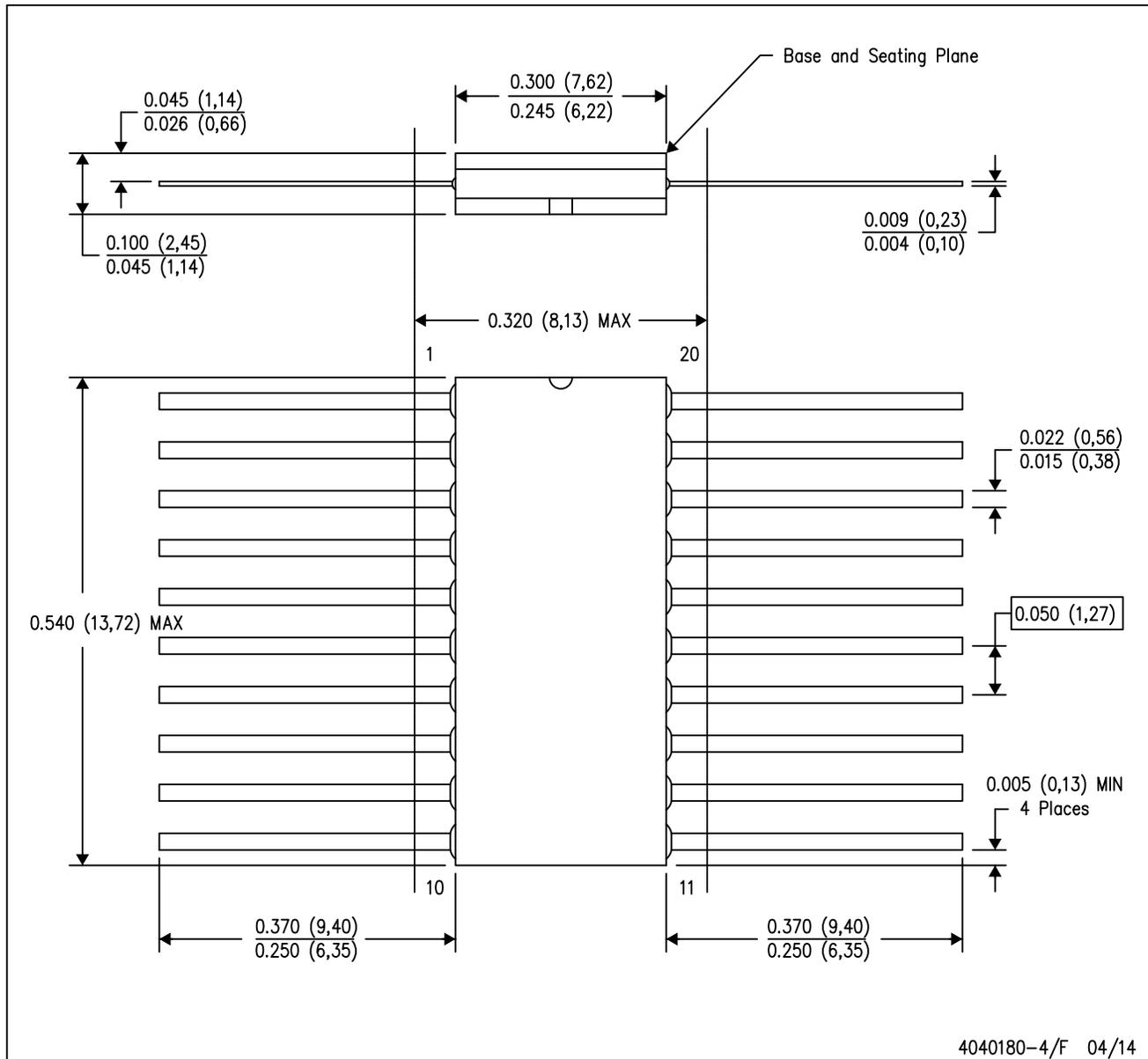
0.300 (7,62)
0.245 (6,22)

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.009 (0,23)
0.004 (0,10)

0.100 (2,45)
0.045 (1,14)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN
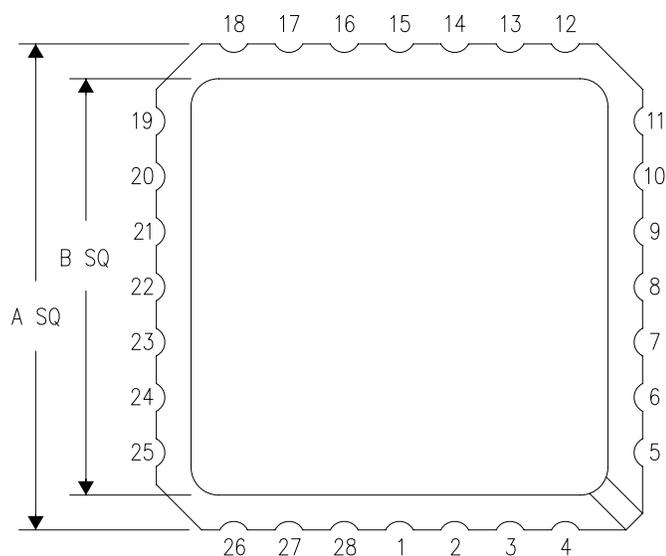
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.080\ (2,03)}{0.064\ (1,63)}$

$\dfrac{0.055\ (1,40)}{0.045\ (1,14)}$

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

$\dfrac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$
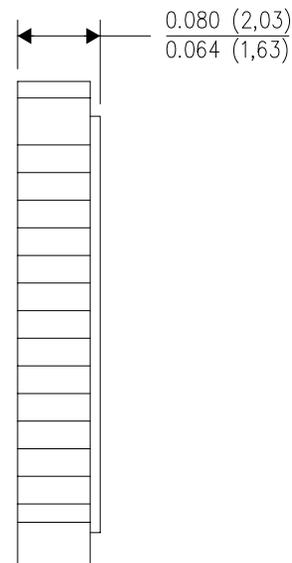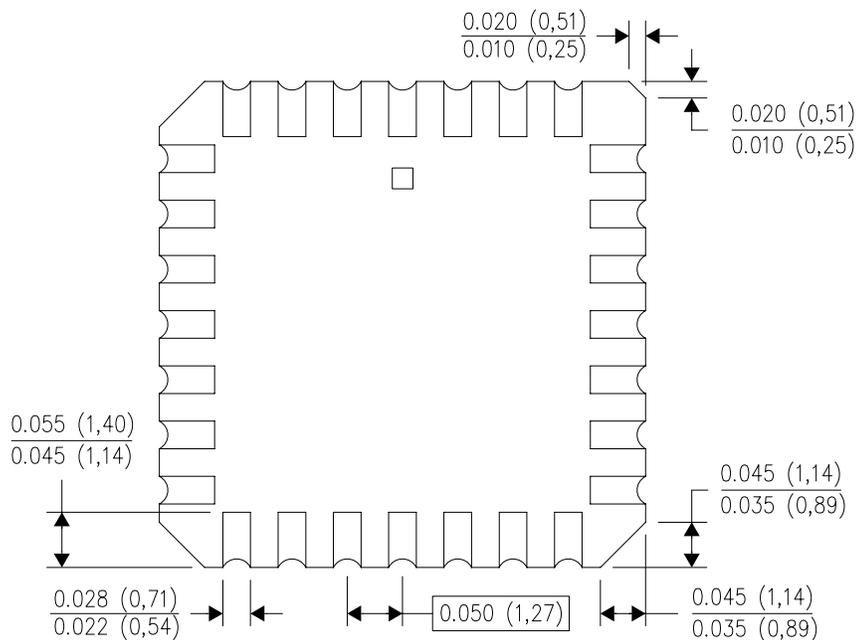
4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a metal lid.
          D.   Falls within JEDEC MS−004

TEXAS
INSTRUMENTS
www.ti.com

N (R–PDIP–T**)   **PLASTIC DUAL–IN–LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C△ MS–001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10)

1   8

0.070 (1,78) / 0.045 (1,14) △D△

0.045 (1,14) / 0.030 (0,76) △D△

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D△

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       △C△ Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
       △D△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00) / 0.496 (12,60)

20   11

0.419 (10,63) / 0.393 (9,97)

0.299 (7,60) / 0.291 (7,40)

1   10

Pin 1 Index Area

0.050 (1,27)

0.020 (0,51) / 0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30) / 0.004 (0,10)

0.013 (0,33) / 0.008 (0,20)

Gauge Plane

0.010 (0,25)

0°−8°

0.004 (0,10)

Seating Plane

0.050 (1,27) / 0.016 (0,40)

4040000−4/G 01/11
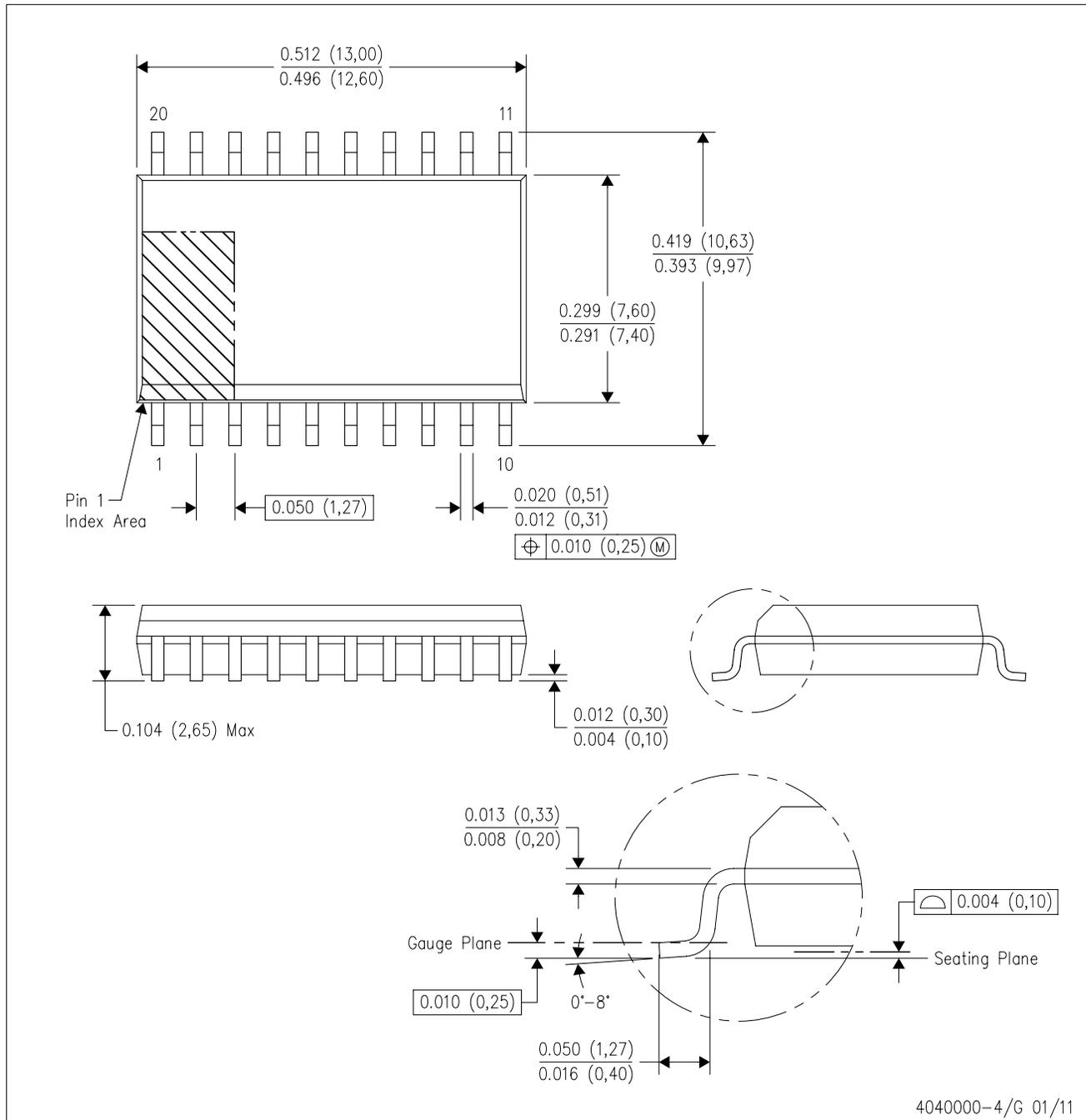
NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

TEXAS INSTRUMENTS
www.ti.com

DW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6 →   ←18x1,27

9,4

20x0,55   ←18x1,27

20x1,95

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around
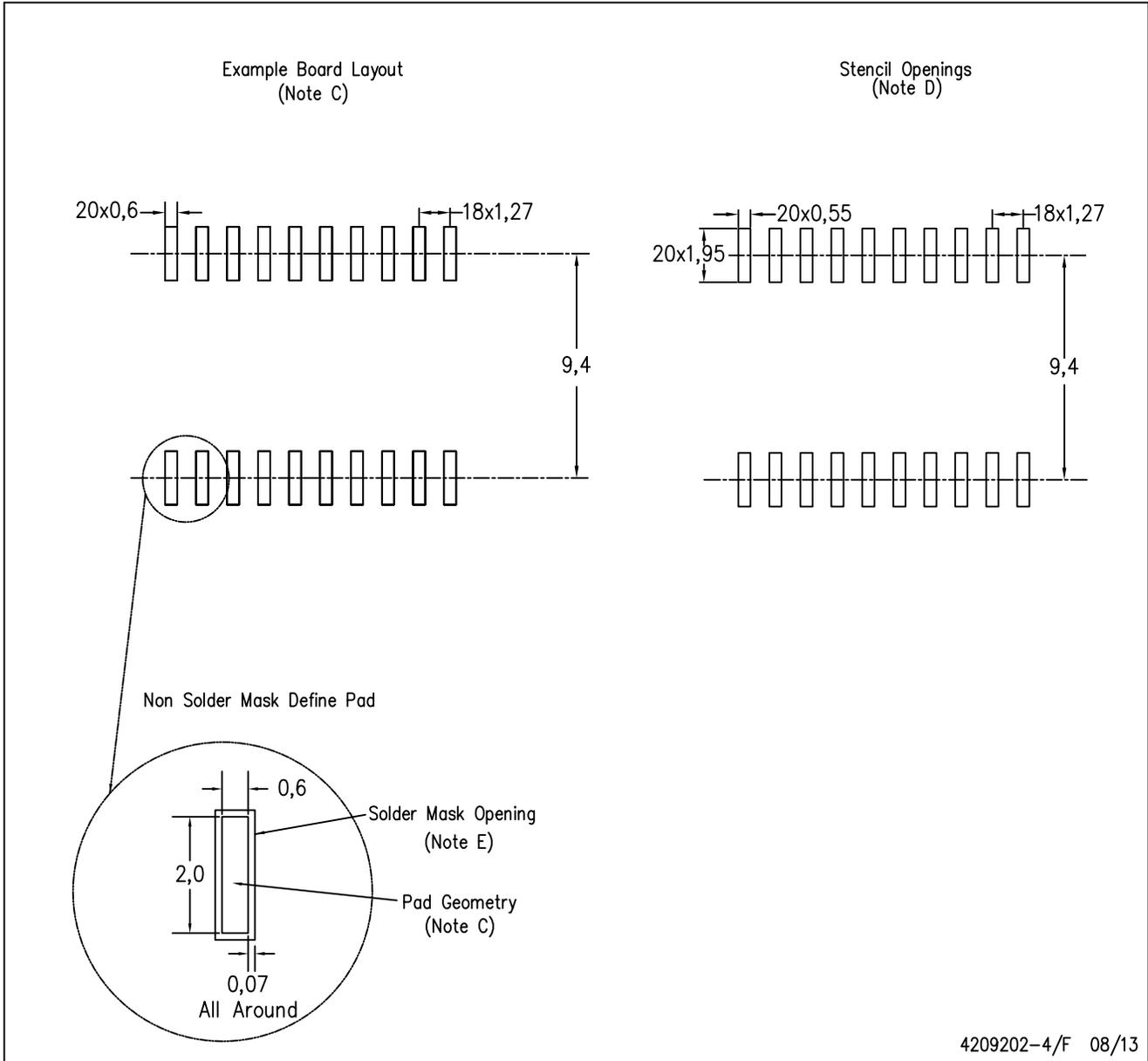
4209202-4/F   08/13

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Refer to IPC7351 for alternate board design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC-7525
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN
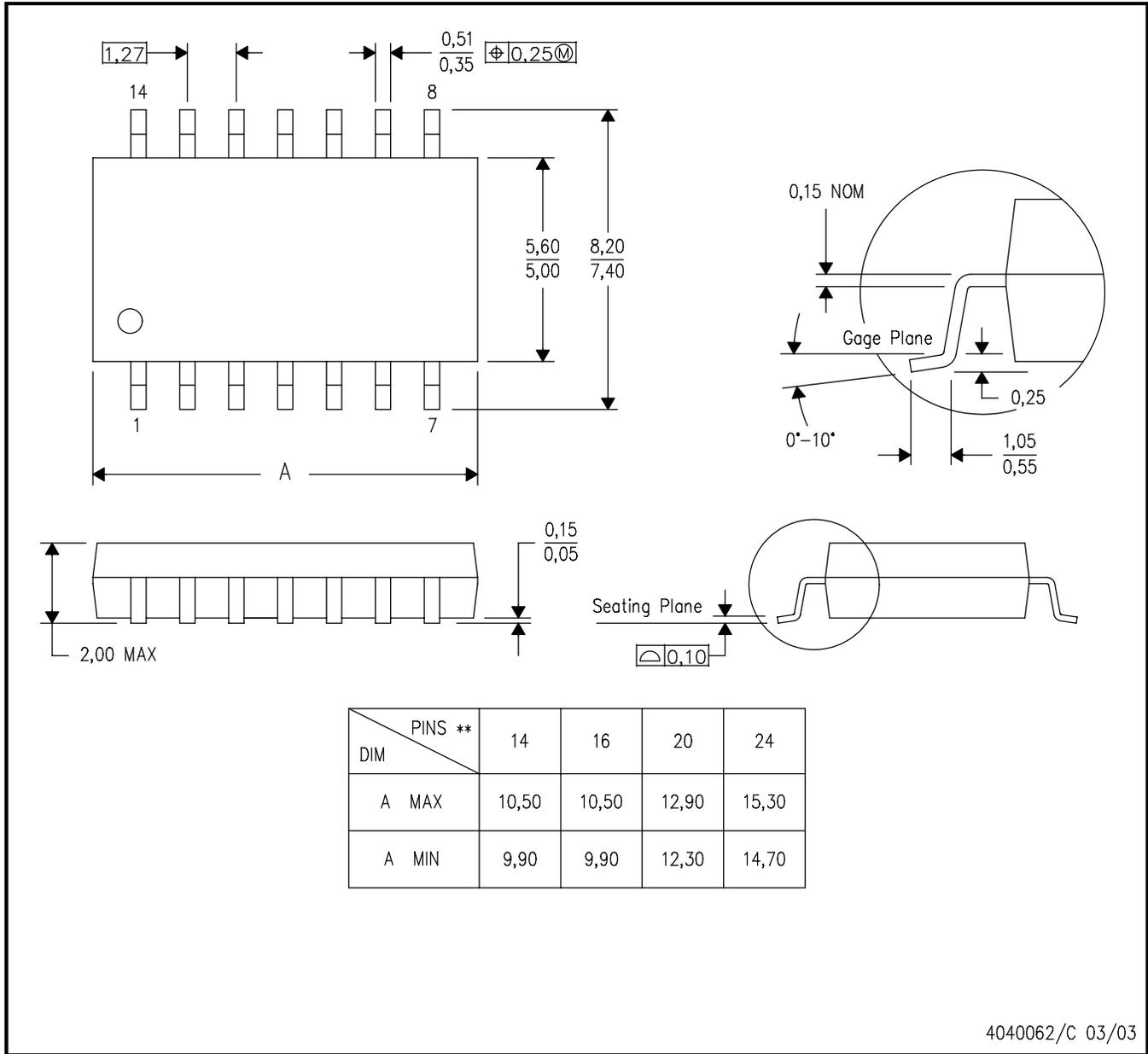
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		