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National Semiconductor

November 2005

CLC002
SMPTE 292M / 259M Serial Digital Cable Driver

General Description

The CLC002 SMPTE 292M / 259M serial digital cable driver is a monolithic, high-speed cable driver designed for use in SMPTE 292M / 259M serial digital video and ITU-T G.703 serial digital data transmission applications. The CLC002 drives 75Ω transmission lines (Belden 8281, Belden 1694A or equivalent) at data rates up to 1.485 Gbps.

The CLC002 provides two selectable slew rates for SMPTE 259M and SMPTE 292M compliance. The output voltage swing is adjustable via a single external resistor.

The CLC002 is powered from a single 3.3V supply. Power consumption is typically 125mW in SD mode and 149mW in HD mode.

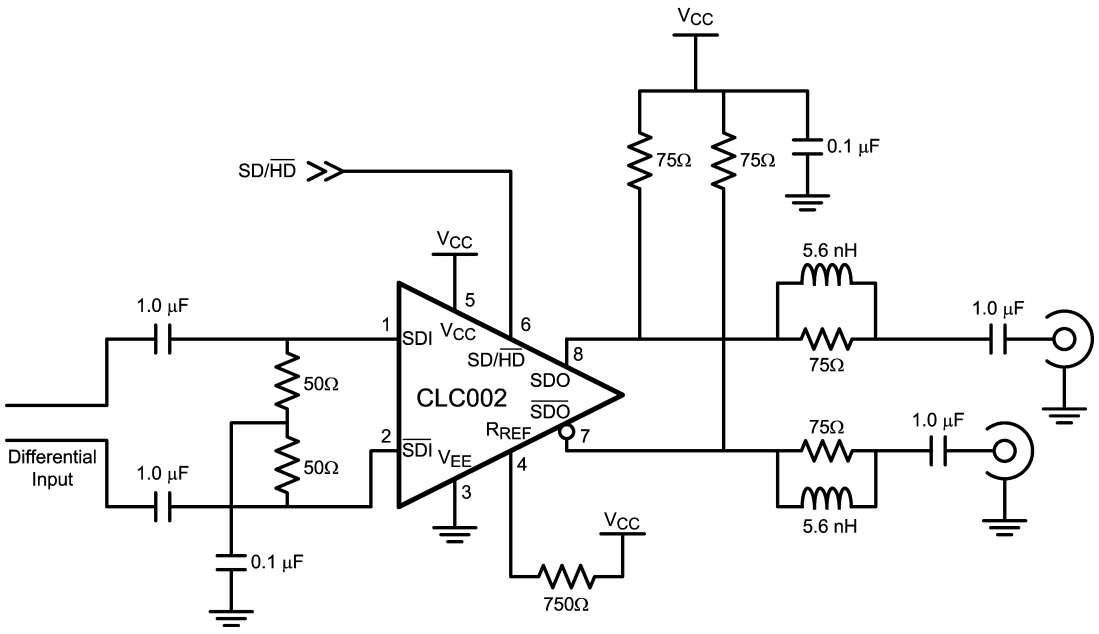
Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Data rates to 1.485 Gbps
- Differential input
- 75Ω differential output
- Selectable slew rate
- Adjustable output amplitude
- Single 3.3V supply operation
- Operating temperature range: Commercial 0˚C to +70˚C (CLC002MA) or Industrial –40˚C to +85˚C (CLC002TMA)
- Typical power consumption: 125mW in SD mode and 149mW in HD mode
- Replaces the GS1528 and GS1528A

Applications

- SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital interfaces
- Sonet/SDH and ATM interfaces
- Digital routers and switches
- Distribution amplifiers
- Buffer applications
- Set top boxes
- Security cameras

Typical Application



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Absolute Maximum Ratings (Note 1)

Supply Voltage:	−0.5V to 3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Output Current	28mA
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature	+150˚C
Lead Temperature (Soldering 4 Sec)	+260˚C
Package Thermal Resistance	
θ_{JA} 8-pin SOIC	+125˚C/W
θ_{JC} 8-pin SOIC	+105˚C/W
ESD Rating (HBM)	5kV
ESD Rating (MM)	250V

Recommended Operating Conditions

Supply Voltage (V_{CC} − V_{EE}):	3.3V ±5%
Operating Free Air Temperature (T_A)	
CLC002MA	0˚C to +70˚C
CLC002TMA	−40˚C to +85˚C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2, 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, $\overline{SDI}$	1.6 + V_{SDI}/2		V_{CC} − V_{SDI}/2	V
V_{SDI}	Input Voltage Swing	Differential		100		2000	mV_{P-P}
V_{CMOUT}	Output Common Mode Voltage		SDO, $\overline{SDO}$		V_{CC} − V_{SDO}		V
V_{SDO}	Output Voltage Swing	Single-ended, 75Ω load, R_{REF} = 750Ω 1%		750	800	850	mV_{P-P}
		Single-ended, 75Ω load, R_{REF} = 590Ω 1%		900	1000	1100	mV_{P-P}
	SD/$\overline{HD}$ Input Voltage	Min for SD	SD/$\overline{HD}$	2.4			V
		Max for HD				0.8	V
	SD/$\overline{HD}$ Input Current				3.7		µA
I_{CC}	Supply Current	SD/$\overline{HD}$ = 0, (Note 5)			45	49	mA
		SD/$\overline{HD}$ = 1, (Note 5)			38	43	mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{SDI}	Input Data Rate	(Note 4)	SDI, $\overline{SDI}$			1485	Mbps
t_{jit}	Additive Jitter	1.485 Gbps	SDO, $\overline{SDO}$		26		ps_{P-P}
		270 Mbps			18		ps_{P-P}
t_r,t_f	Output Rise Time, Fall Time	SD/$\overline{HD}$ = 0, 20% − 80%, (Note 6)			120	220	ps
		SD/$\overline{HD}$ = 1, 20% − 80%		400	560	800	ps
	Mismatch in Rise/Fall Time	(Note 4)				30	ps
t_{OS}	Output Overshoot	(Note 4)				8	%
RL_{SDO}	Output Return Loss	(Note 7)		15	20		dB

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.

Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25˚C.

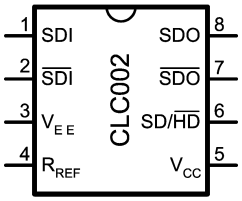
Note 4: Specification is guaranteed by characterization.

Note 5: Maximum I_{CC} is measured at V_{CC} = +3.465V and T_A = +70˚C.

Note 6: Specification is guaranteed by characterization and verified by test.

Note 7: Output return loss is dependent on board design. The CLC002 meets this specification on the SD002 evaluation board from 5MHz to 1.5GHz.

Connection Diagram



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8-Pin SOIC
Order Number CLC002MA or CLC002TMA
See NS Package Number M08A

Pin Descriptions

Pin #	Name	Description
1	SDI	Serial data true input.
2	$\overline{SDI}$	Serial data complement input.
3	V_{EE}	Negative power supply (ground).
4	R_{REF}	Output driver level control. Connect a resistor to V_{CC} to set output voltage swing.
5	V_{CC}	Positive power supply (+3.3V).
6	SD/$\overline{HD}$	Output slew rate control. Output rise/fall time complies with SMPTE 292M when low and SMPTE 259M when high.
7	$\overline{SDO}$	Serial data complement output.
8	SDO	Serial data true output.

Device Operation

INPUT INTERFACING

The CLC002 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range. SDI and $\overline{SDI}$ are self-biased at approximately 2.1V with V_{CC} = 3.3V. *Figure 1* shows the differential input stage for SDI and $\overline{SDI}$.

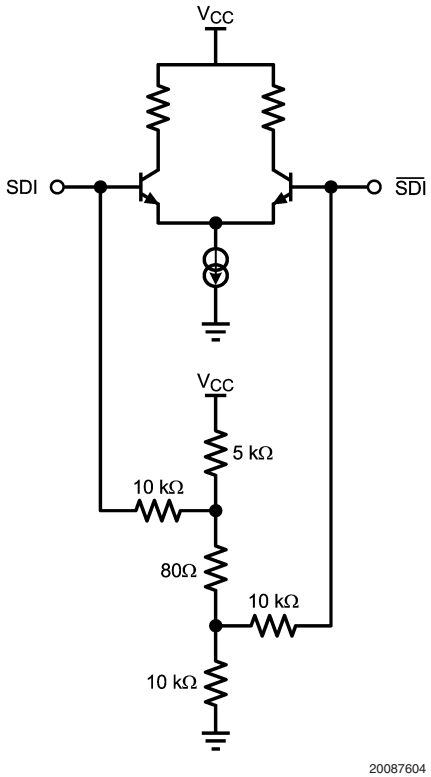

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FIGURE 1. Differential Input Stage for SDI and $\overline{SDI}$.

Device Operation (Continued)

OUTPUT INTERFACING

The CLC002 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75Ω AC-coupled coaxial cable (with R_{REF} = 750Ω). Output level is controlled by the value of the R_{REF} resistor connected between pin 4 and V_{CC}.

The R_{REF} resistor should be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network should be removed to minimize parasitic capacitance.

OUTPUT SLEW RATE CONTROL

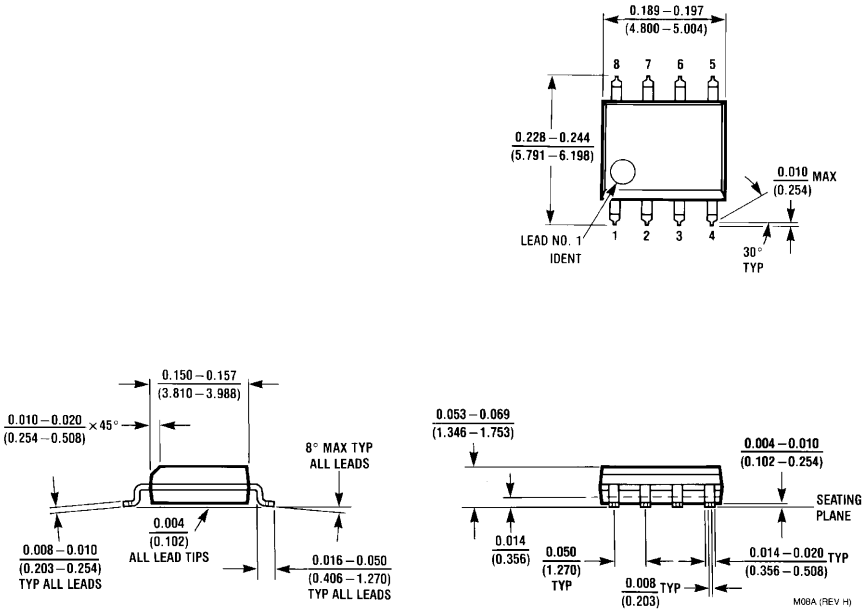
The CLC002 output rise and fall times are selectable for either SMPTE 259M or SMPTE 292M compliance via pin 6, SD/$\overline{HD}$. For slower rise and fall times, or SMPTE 259M compliance, SD/$\overline{HD}$ is set high. For faster rise and fall times, or SMPTE 292M compliance, SD/$\overline{HD}$ is set low.

REPLACING THE GENNUM GS1528

The CLC002 is form-fit-function compatible with the Gennum GS1528 and GS1528A.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
Order Number CLC002MA or CLC002TMA
NS Package Number M08A

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