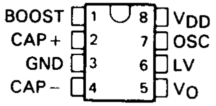
# LTC1044
# SWITCHED-CAPACITOR VOLTAGE CONVERTER

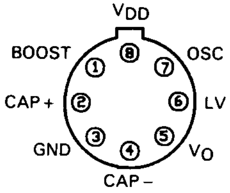
D3193, JANUARY 1989

- **Plug-In Compatible with the 7660 with These Additional Features:**
    - **Operation to 9 V Over Full Temperature Range with No External Protection Diodes**
    - **Boost Pin for Higher Switching Frequency**
    - **2 1/2 Times Lower Quiescent Power**
    - **Efficient Voltage Doubler**
- **No-Load Supply Current at 5 V . . . 200 µA Max**
- **Open-Circuit Voltage Conversion Efficiency . . . 97% Min**
- **Power Conversion Efficiency . . . 95% Min**
- **Operating Supply Voltage Range . . . 1.5 V to 9 V**
- **Commercial Device Operates from −40°C to 85°C**

**LTC1044M . . . JG PACKAGE**
**LTC1044C . . . D, JG, OR P PACKAGE**
**(TOP VIEW)**



**L PACKAGE**
**(TOP VIEW)**



## description

The LTC1044 is a monolithic CMOS switched-capacitor voltage converter manufactured using CMOS silicon-gate technology. The LTC1044 provides several voltage conversion functions; the input voltage can be inverted ($V_O = -V_I$), doubled ($V_O = 2V_I$), divided ($V_O = V_I/2$), or multiplied ($V_O = \pm nV_I$).

Designed to be pin-for-pin and functionally compatible with the 7660, the LTC1044 offers significant new design and performance advantages while still maintaining compatibility with existing 7660 designs.

The LTC1044M is characterized for operation over the full military temperature range of −55°C to 125°C. The LTC1044C is characterized for operation from −40°C to 85°C.

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### absolute maximum ratings over operating free-air temperature range[†]

| | |
|---|---|
| Supply voltage, $V_{DD}$ | 9.5 V |
| Input voltage range (pins 1, 6, and 7, see Note 1) | −0.3 V to $V_{DD}$ + 0.3 V |
| Input current, $I_I$ (pin 6) | 20 µA |
| Duration of output short circuit ($V_{CC+} \leq 5.5$ V) | unlimited |
| Operating free-air temperature range: LTC1044M | −55°C to 125°C |
| LTC1044C | −40°C to 85°C |
| Storage temperature range | −65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package | 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package | 260°C |
| L package | 300°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | LTC1044M | | LTC1044C | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{DD}$ | Supply voltage ($R_L$ = 10 kΩ, see Note 1) | 1.5 | 9 | 1.5 | 9 | V |
| $V_I$ | Input voltage (pins 1, 6, and 7, see Note 2) | −0.3 | $V_{DD}$+0.3 | −0.3 | $V_{DD}$+0.3 | V |
| $T_A$ | Operating free-air temperature | −55 | 125 | −40 | 85 | °C |

NOTES: 1. The LTC1044 operates with alkaline, mercury, or NiCad 9-V batteries, even when the initial battery voltage is slightly higher than 9 V.
2. Connecting any input terminal to voltages substantially greater than $V_{DD}$ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted, see Figure 1)

| PARAMETER | | TEST CONDITIONS | $T_A$† | LTC1044M | | | LTC1044C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $r_o$ | Output resistance | $I_O$ = 20 mA, $f_{osc}$ = 5 kHz | 25°C | | | 100 | | | 100 | Ω |
| | | | Full range | | | 150 | | | 130 | |
| | | $V_{DD}$ = 2 V, $I_L$ = 3 mA, $f_{osc}$ = 1 kHz | Full range | | | 400 | | | 325 | |
| $f_{osc}$ | Oscillator frequency | $V_{DD}$ = 5 V, $C_{osc}$ = 1 pF, See Note 3 | Full range | 5 | | | 5 | | | kHz |
| | | $V_{DD}$ = 2 V, $C_{osc}$ = 1 pF, See Note 3 | | 1 | | | 1 | | | |
| $\eta_P$ | Power efficiency | $R_L$ = 5 kΩ, $f_{osc}$ = 5 kHz | 25°C | 95 | 98 | | 95 | 98 | | % |
| $\eta_{VO}$ | Voltage conversion efficiency | $R_L = \infty$ | 25°C | 97 | 99.9 | | 97 | 99.9 | | % |
| $I_{osc}$ | Oscillator sink or source current | $V_{osc}$ = 0 or $V_{DD}$, Pin 1 at 0 V | Full range | | | 3 | | | 3 | μA |
| | | $V_{osc}$ = 0 or $V_{DD}$, Pin 1 at $V_{DD}$ | | | | 20 | | | 20 | |
| $I_{DD}$ | Supply current | $R_L = \infty$, Pins 1 and 7 no connection | 25°C | | 60 | 200 | | 60 | 200 | μA |
| | | $R_L = \infty$, Pins 1 and 7 $V_{DD}$ = 3 V | | | 20 | | | 20 | | |

† Full range is −55°C to 125°C for the LTC1044M and −40°C to 85°C for the LTC1044C.

NOTE 3: $f_{osc}$ is tested with $C_{osc}$ at 100 pF to minimize the effects of test fixture capacitance loading. The 1-pF frequency is correlated to this 100-pF test point and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

## PARAMETER MEASUREMENT INFORMATION

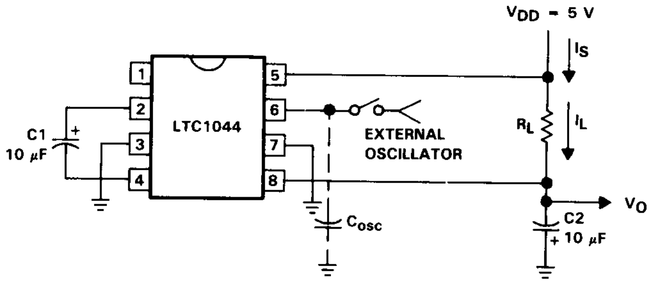

FIGURE 1. TEST CIRCUIT

## TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

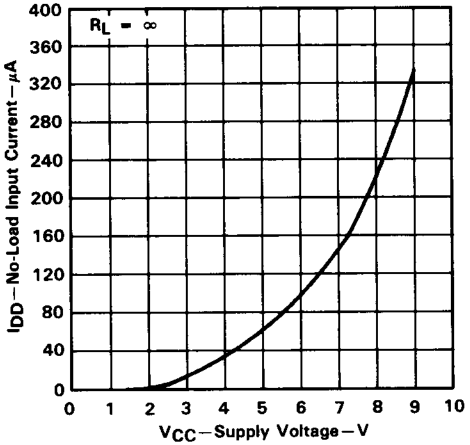

FIGURE 2

OUTPUT RESISTANCE
vs
SUPPLY VOLTAGE

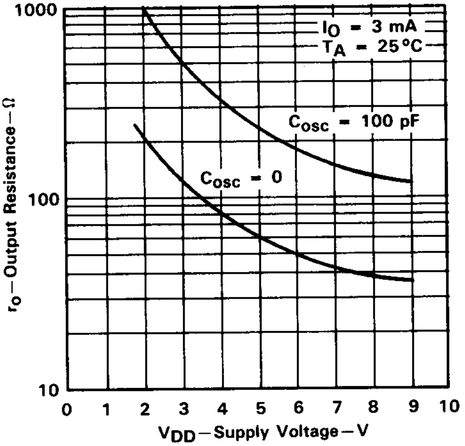

FIGURE 3

OUTPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

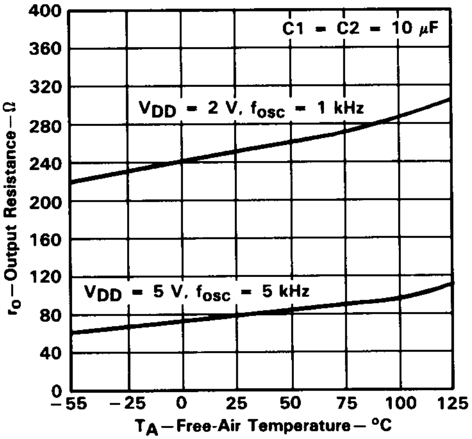

FIGURE 4

OUTPUT RESISTANCE
vs
OSCILLATOR FREQUENCY

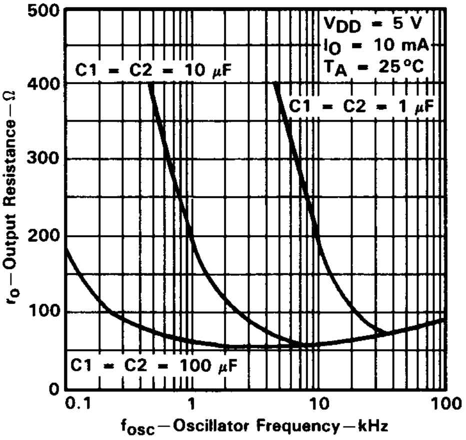

FIGURE 5

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the two devices.

## TYPICAL CHARACTERISTICS†

OSCILLATOR FREQUENCY
vs
EXTERNAL CAPACITOR

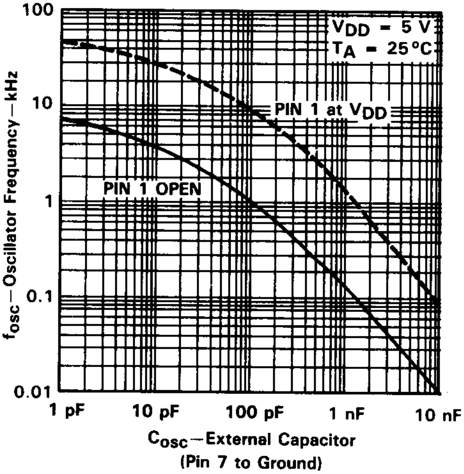

FIGURE 6

OSCILLATOR FREQUENCY
vs
SUPPLY VOLTAGE

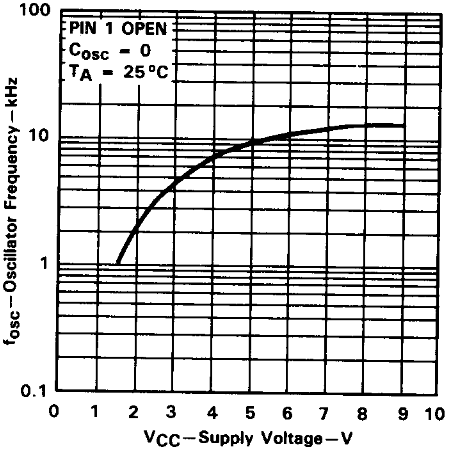

FIGURE 7

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

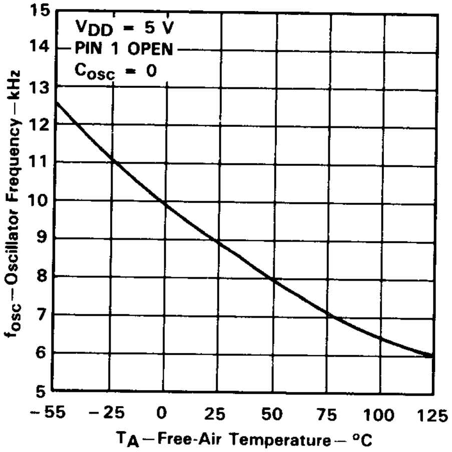

FIGURE 8

POWER CONVERSION EFFICIENCY
vs
OSCILLATOR FREQUENCY

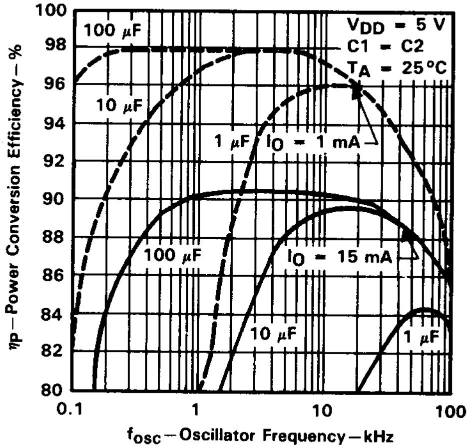

FIGURE 9

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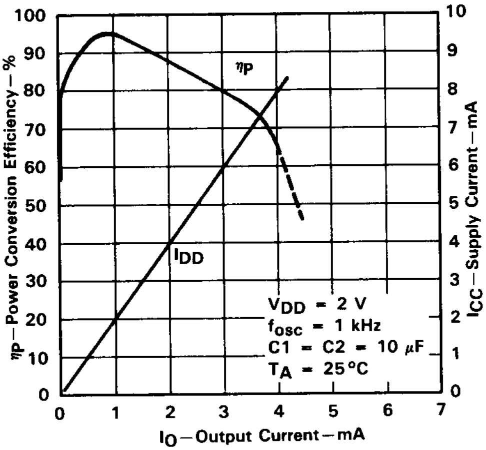
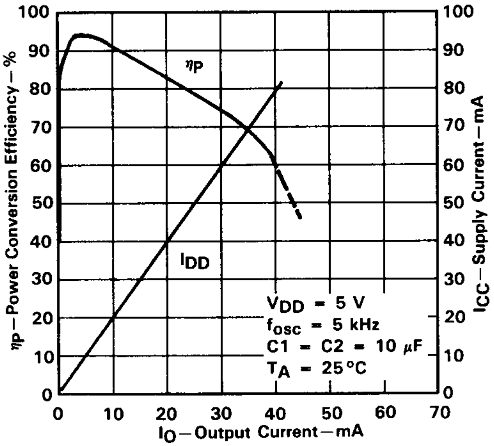
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the two devices.

## TYPICAL CHARACTERISTICS



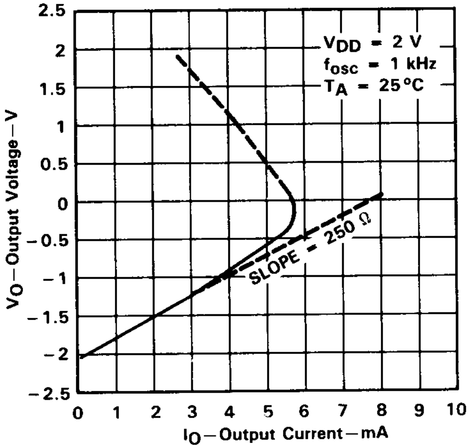
POWER CONVERSION EFFICIENCY and SUPPLY CURRENT vs OUTPUT CURRENT

FIGURE 10



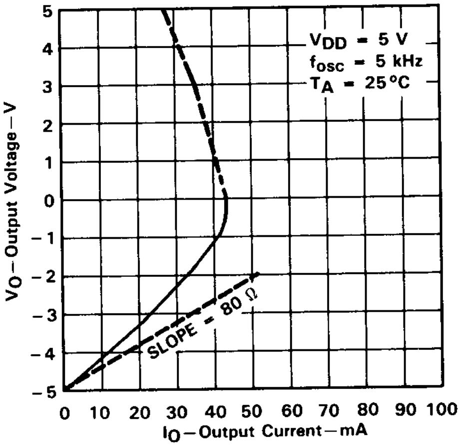
POWER CONVERSION EFFICIENCY and SUPPLY CURRENT vs OUTPUT CURRENT

FIGURE 11



OUTPUT VOLTAGE vs OUTPUT CURRENT

FIGURE 12



OUTPUT VOLTAGE vs OUTPUT CURRENT

FIGURE 13

## TYPICAL APPLICATION DATA

### theory of operation

To understand the theory of operation of the LTC1044, a review of a basic switched-capacitor building block is helpful. In Figure 14, when the switch is in the left position, capacitor C1 charges to voltage V1. The total charge on C1 is $q1 = C1 \bullet V1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $q2 = C1 \bullet V2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is calculated as follows:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is calculated as follows:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{eq}}$$

where $R_{eq}$ is defined as $R_{eq} = 1/fC1$. The equivalent circuit for the switched-capacitor network is shown in Figure 15.

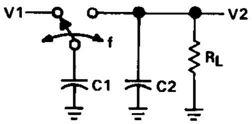
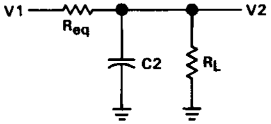


FIGURE 14. SWITCHED-CAPACITOR BUILDING BLOCK



NOTE: $R_{eq} = \frac{1}{fC1}$

FIGURE 15. SWITCHED-CAPACITOR EQUIVALENT CIRCUIT

Examination of Figure 16 shows that the LTC1044 has the same switching action as the basic switched-capacitor building block, with the addition of finite switch on-state resistance and output voltage ripple.

The simple theory, although not exact, helps illustrate how the device operates. For example, it explains how the LTC1044 behaves in Figure 9. The loss, and hence the efficiency, is determined by the output impedance. As frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term, and power efficiency drops. Figure 9 shows this effect for various capacitor values.

Note also that power efficiency decreases as frequency increases. This is caused by internal switching losses that occur because some finite charge is lost in each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant, and the power efficiency starts to decrease.

## TYPICAL APPLICATION DATA

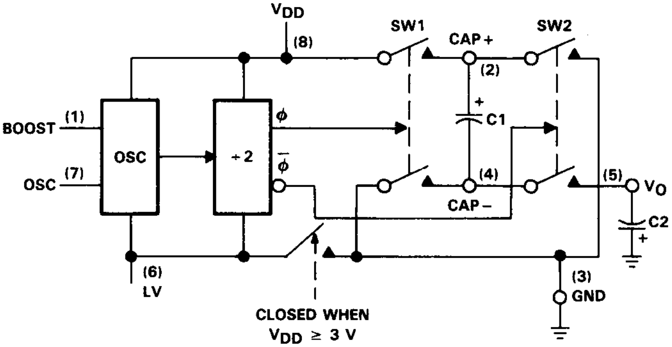


FIGURE 16. LTC1044 SWITCHED-CAPACITOR VOLTAGE CONVERTER BLOCK DIAGRAM

### LV (pin 6)

The internal logic of the LTC1044 runs between $V_{DD}$ and LV (pin 6). For $V_{DD} \geq 3$ V, an internal switch shorts LV to GND (pin 3). The LV pin can be tied to ground or left floating. For $V_{DD} \leq 3$ V, the LV pin should be tied to GND.

### OSC (pin 7) and BOOST (pin 1)

The switching frequency can be raised, lowered, or driven from an external source. Figure 17 shows a functional diagram of the oscillator circuit. By connecting the boost pin (pin 1) to $V_{DD}$, the charge and discharge current is increased, thereby increasing the frequency by a factor of approximately 7. Increasing the frequency decreases output impedance and ripple for higher load currents. Loading pin 7 with more capacitance lowers the frequency. Using the boost pin (pin 1) in conjunction with external capacitance on pin 7 allows the user to select the frequency over a wide range.

Driving the LTC1044 from an external frequency source can easily be achieved by driving pin 7 and leaving the boost pin open, as shown in Figure 18. The output current from pin 7 is small, typically 0.5 µA, so a logic gate can drive this current. Using a CMOS logic gate is preferable because it can operate over a wide supply voltage range (3 V to 15 V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 17. For 5-V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 18).

## TYPICAL APPLICATION DATA

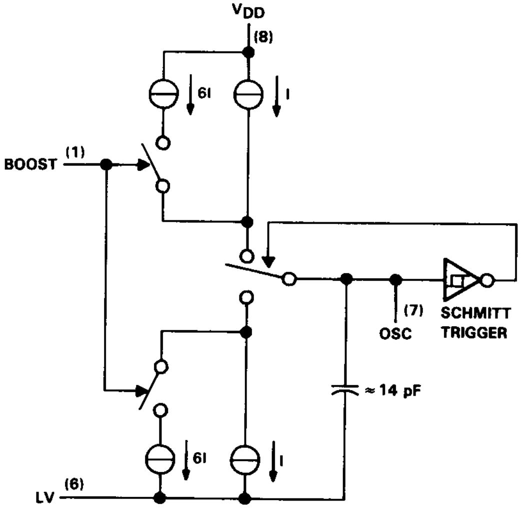


FIGURE 17. OSCILLATOR

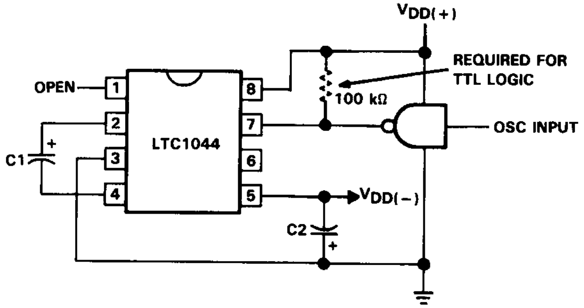


FIGURE 18. EXTERNAL CLOCKING

### external diode ($D_X$)

Previous circuits of this type have required a diode between $V_O$ (pin 5) and the external capacitor C2 for voltages above 6.5 V (5 V for military temperature range). The improvements in the LTC1044 circuit design and Texas Instruments LinCMOS™ silicon-gate process have eliminated the need for this diode. The LTC1044 operates from 1.5 V to 9 V without the protection diode over all temperature ranges. The LTC1044 will operate without any problems in existing LTC7660 designs that use the protection diode as long as the maximum recommended supply voltage of 9 V is not exceeded.

LinCMOS is a trademark of Texas Instruments Incorporated.

## TYPICAL APPLICATION DATA

### capacitor selection

External capacitors C1 and C2 are not critical. They do not have to be high quality or have tight tolerance, nor is matching required. Aluminum or tantalum electrolytics are excellent choices, with cost and size being the only consideration.

### negative voltage converter

Figure 19 shows a typical connection that provides a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges without the need for external diodes. The LV pin (pin 6) is shown grounded, but for $V_{DD} \geq 3$ V, it may be floated, since LV is internally switched to ground (pin 3) for $V_{DD} \geq 3$ V.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80-Ω resistor. The 80-Ω output impedance is composed of two terms—the equivalent switched-capacitor resistance (see Theory of Operation) and a term related to the on-state resistance of the MOS switches. At an oscillator frequency of 10 kHz and C1 = 10 µF, the first term is:

$$R_{eq} = \frac{1}{(f_{osc}/2) \times C1} = \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\ \Omega$$

Notice that the equation for $R_{eq}$ is not a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a $2\pi$ term. While the exact expression for output impedance is extremely complex, the dominant effect of the capacitor is clearly shown in the typical curves of output impedance and power efficiency versus frequency. For C1 = C2 = 10 µF, the output impedance goes from 60 Ω at $f_{OSC}$ = 10 kHz to 200 Ω at $f_{OSC}$ = 1 kHz. As the 1/fC term becomes large compared to the switch on-state resistance term, the output resistance is determined by 1/fC only.

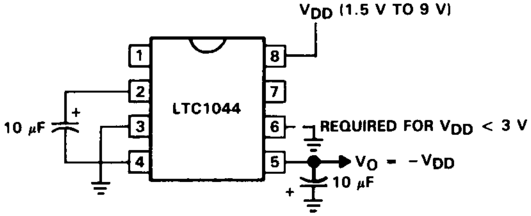


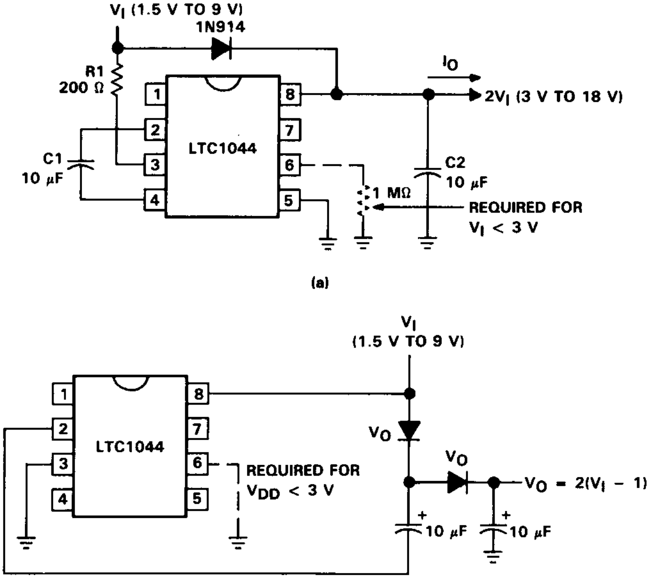
FIGURE 19. NEGATIVE VOLTAGE CONVERTER

### voltage doubling

Figure 20 illustrates two methods of voltage doubling. In Figure 20(a), doubling is achieved by simply rearranging the connection of the two external capacitors. When the input voltage is less than 3 V, an external 1-MΩ resistor is required to ensure that the oscillator starts; it is not required for higher input voltages.

In this application, the ground input (pin 3) is taken above $V_{DD}$ (pin 8) during power-on, making it prone to latch-up. The latch-up, while not destructive, prevents the circuit from doubling. Resistor R1 is added to eliminate this problem; in most cases, 200 Ω is sufficient. It may be necessary in a particular application to increase this value to guarantee start-up. The voltage drop across R1 is $V_{R1} = 2 \times I_O \times R2$. If this voltage exceeds two diode drops (1.4 V for silicon, 0.8 V for Schottky), the circuit in Figure 20(a) is recommended because it will never have a start-up problem.

## TYPICAL APPLICATION DATA



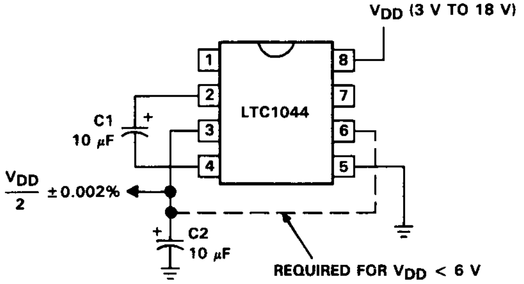
(a)

(b)

FIGURE 20. VOLTAGE DOUBLER

### ultra-precision voltage divider

An ultra-precision voltage divider is shown in Figure 21. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100 nA. However, with a slight loss in accuracy, the load current can be increased.



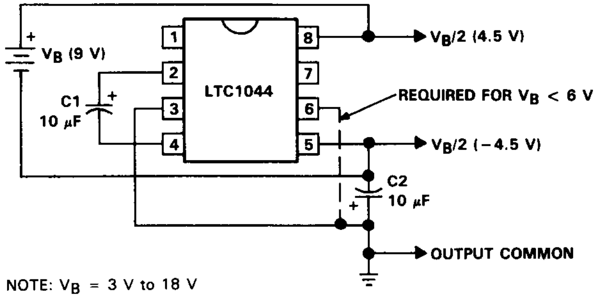
NOTE: $T_A$ = MIN to MAX, $I_O \leq$ 100 nA

FIGURE 21. ULTRA-PRECISION VOLTAGE DIVIDER

## TYPICAL APPLICATION DATA

### battery splitter

Obtaining positive and negative supplies from a single battery or single power supply is a common need in many systems. Where current requirements are small, the circuit shown in Figure 22 is a simple solution. It provides symmetrical positive and negative output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6 V, pin 6 should also be connected to pin 3, as shown by the dashed line.

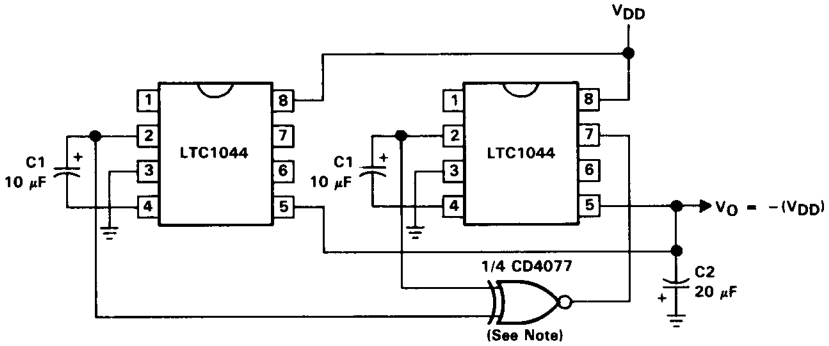


NOTE: $V_B$ = 3 V to 18 V

FIGURE 22. BATTERY SPLITTER

### paralleling for lower output resistance

Figures 23, 24, and 25 illustrate the flexibility of the LTC1044. Figure 23 shows two LTC1044s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the size of C1 or increasing the frequency is more beneficial than the paralleling circuit shown.



NOTE: The exclusive NOR gate synchronizes both LTC1044s to minimize ripple.

FIGURE 23. PARALLELING FOR LOWER OUTPUT RESISTANCE

## TYPICAL APPLICATION DATA

Figures 24 and 25 "stack" two LTC1044s to provide even higher voltages. As shown schematically in Figure 24, a negative voltage doubler or tripler can be achieved depending upon how pin 8 of the second LTC1044 is connected. Figure 25 illustrates a similar circuit that can be used to obtain positive tripling, or even quadrupling [the doubler circuit appears in Figure 20(a)]. In both of these circuits, the available output current is a function of the product of the individual power conversion efficiencies and the voltage step-up ratio.

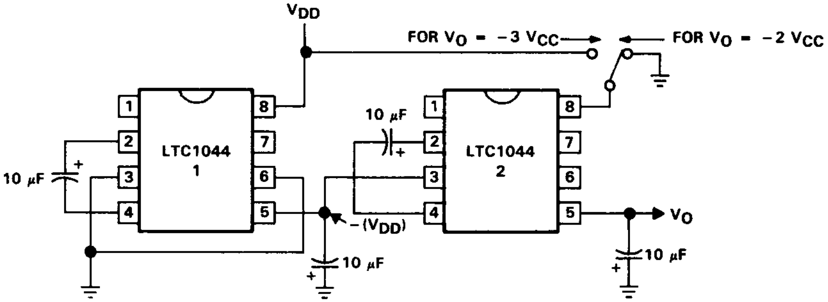
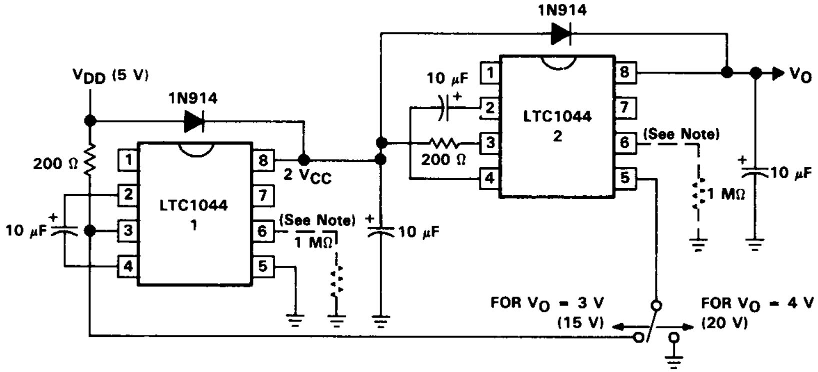


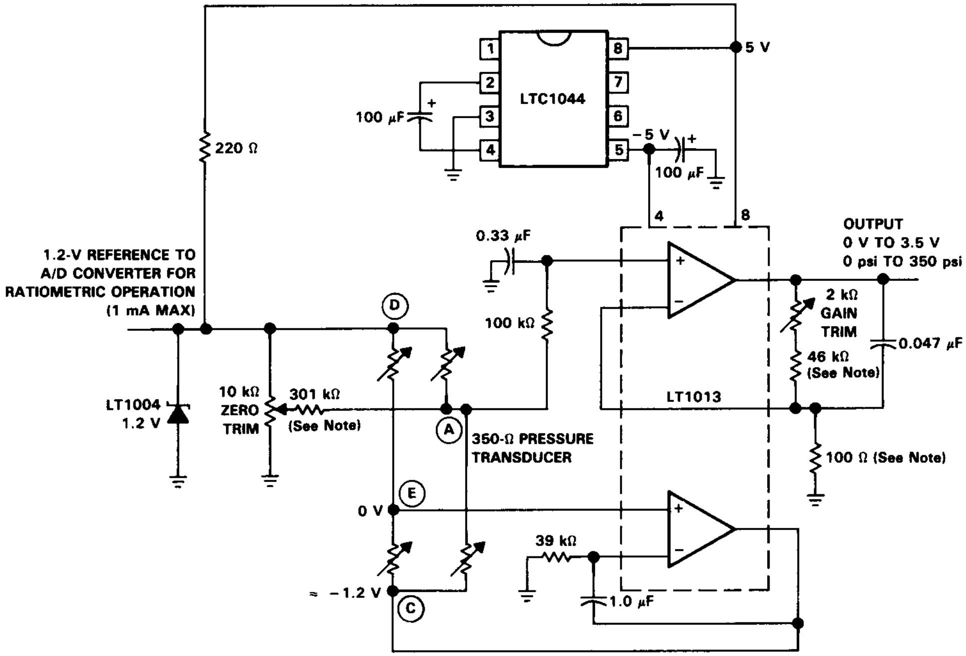
FIGURE 24. STACKING FOR HIGHER VOLTAGE



NOTE: Required for $V_{DD} < 3$ V

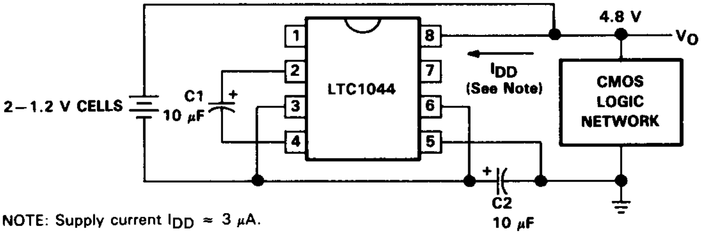
FIGURE 25. VOLTAGE TRIPLER/QUADRUPLER

## TYPICAL APPLICATION DATA



NOTE: 1% film resistor pressure transducer BLH/DHF-350 (Circled letter is pin number)

FIGURE 26. SINGLE 5-V STRAIN GAUGE BRIDGE SIGNAL CONDITIONER



NOTE: Supply current $I_{DD}$ ≈ 3 μA.

FIGURE 27. GENERATING CMOS LOGIC SUPPLY FROM 2 MERCURY BATTERIES

## TYPICAL APPLICATION DATA

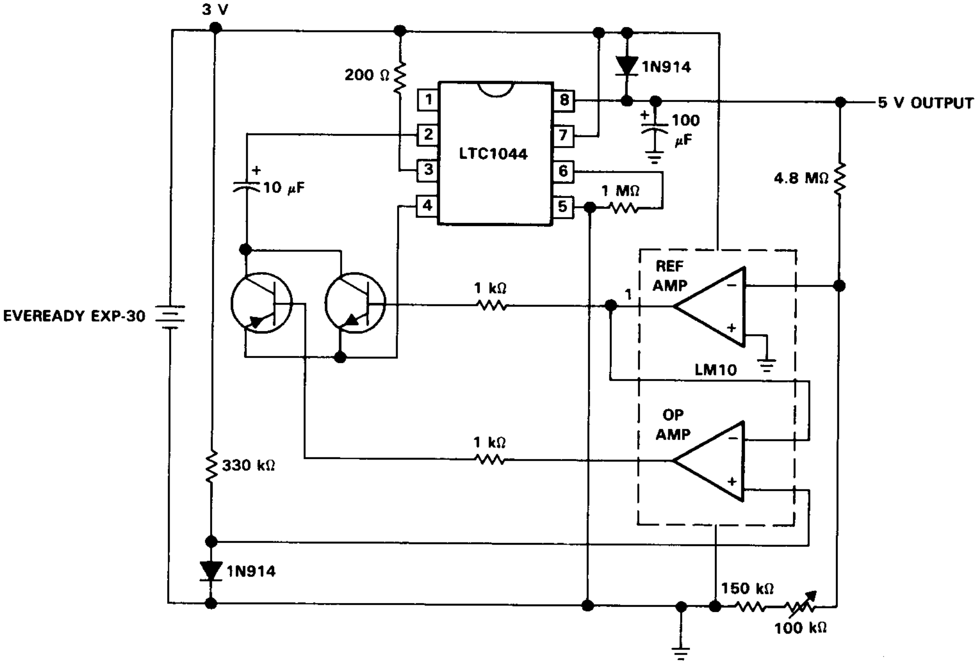
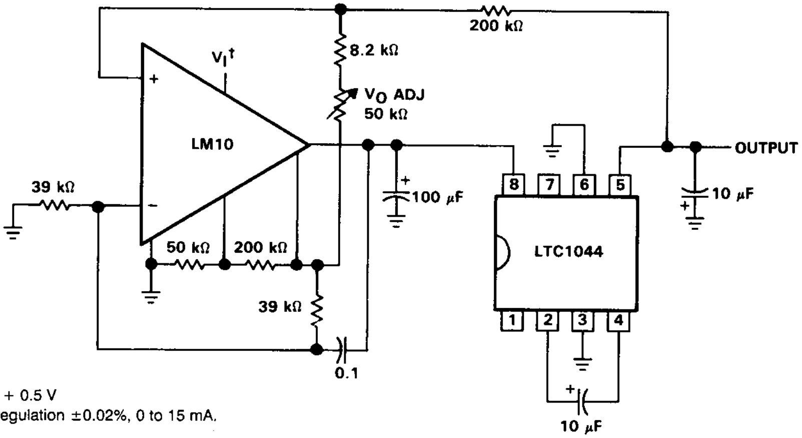


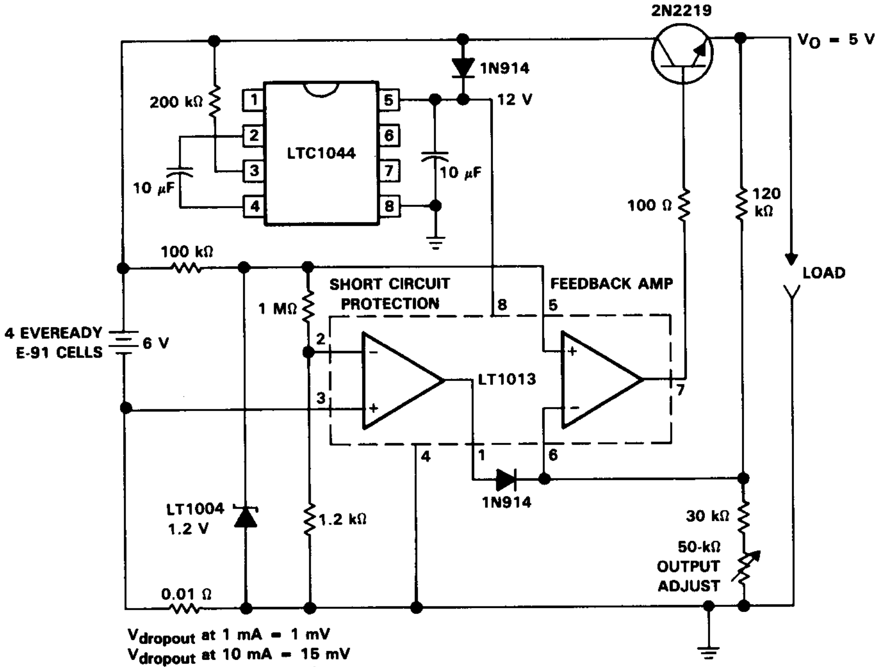
FIGURE 28. REGULATED OUTPUT 3-V TO 5-V CONVERTER



†$V_I \geq |-V_O| + 0.5$ V
NOTE: Load regulation ±0.02%, 0 to 15 mA.

FIGURE 29. LOW-OUTPUT-IMPEDANCE VOLTAGE CONVERTER

## TYPICAL APPLICATION DATA



$V_{dropout}$ at 1 mA = 1 mV
$V_{dropout}$ at 10 mA = 15 mV
$V_{dropout}$ at 100 mA = 95 mA

FIGURE 30. LOW-DROPOUT 5-V REGULATOR