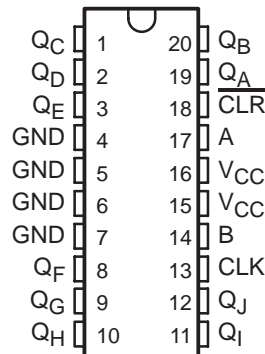


74ACT11898 10-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SCAS144 – OCTOBER 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Fully Synchronous Data Transfers
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE
(TOP VIEW)



description

The 74ACT11898 features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level on the rising edge of the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low provided the minimum setup and hold time requirements are met. Clocking occurs on the low-to-high transition of the clock input.

The 74ACT11898 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUTS			
CLR	CLK	A	B	Q _A	Q _B	...	Q _J
L	X	X	X	L	L		L
H	L	X	X	Q _{A0}	Q _{B0}		Q _{J0}
H	↑	H	H	H	Q _{AN}		Q _{IN}
H	↑	L	X	L	Q _{AN}		Q _{IN}
H	↑	X	L	L	Q _{AN}		Q _{IN}

H = high level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

Q_{A0}, Q_{B0}, Q_{J0} = the level of Q_A, Q_B, Q_J respectively, before the indicated steady-state input conditions were established.

Q_n, Q_{in} = the level of Q_A or Q_J before the most recent ↑ transition of the clock; indicates a one-bit shift.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



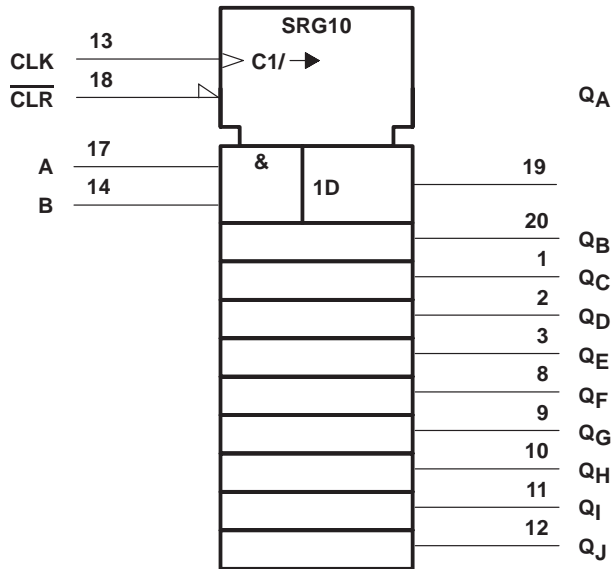
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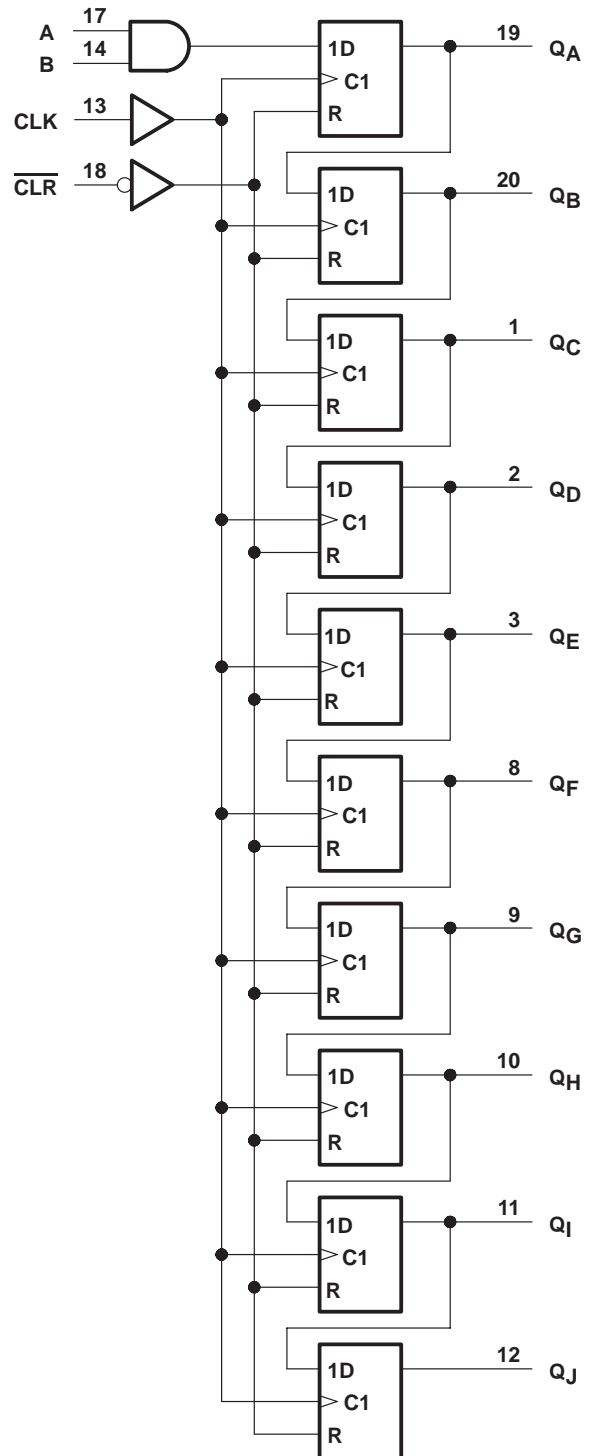
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 250 mA
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4		4.4		V	
		5.5 V	5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	$I_{OH} = -75 \text{ mA}^\ddagger$	5.5 V			3.85			
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1	V	
		5.5 V			0.1	0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V				1.65		
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5	± 5	μA	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1	± 1	μA	
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8	80	μA	
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9	1	mA	
C_i	$V_I = V_{CC}$ or GND	5 V			4		pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC} .



74ACT11898

10-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

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timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	40	0	40	ns
t_w	Pulse duration	$\overline{\text{CLR}}$ low	4.5	4.5		ns
		CLK high or low	12.5	12.5		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	10	10		ns
		$\overline{\text{CLR}}$ inactive	1.5	1.5		
t_h	Hold time, data after $\text{CLK}\uparrow$	0		0		ns

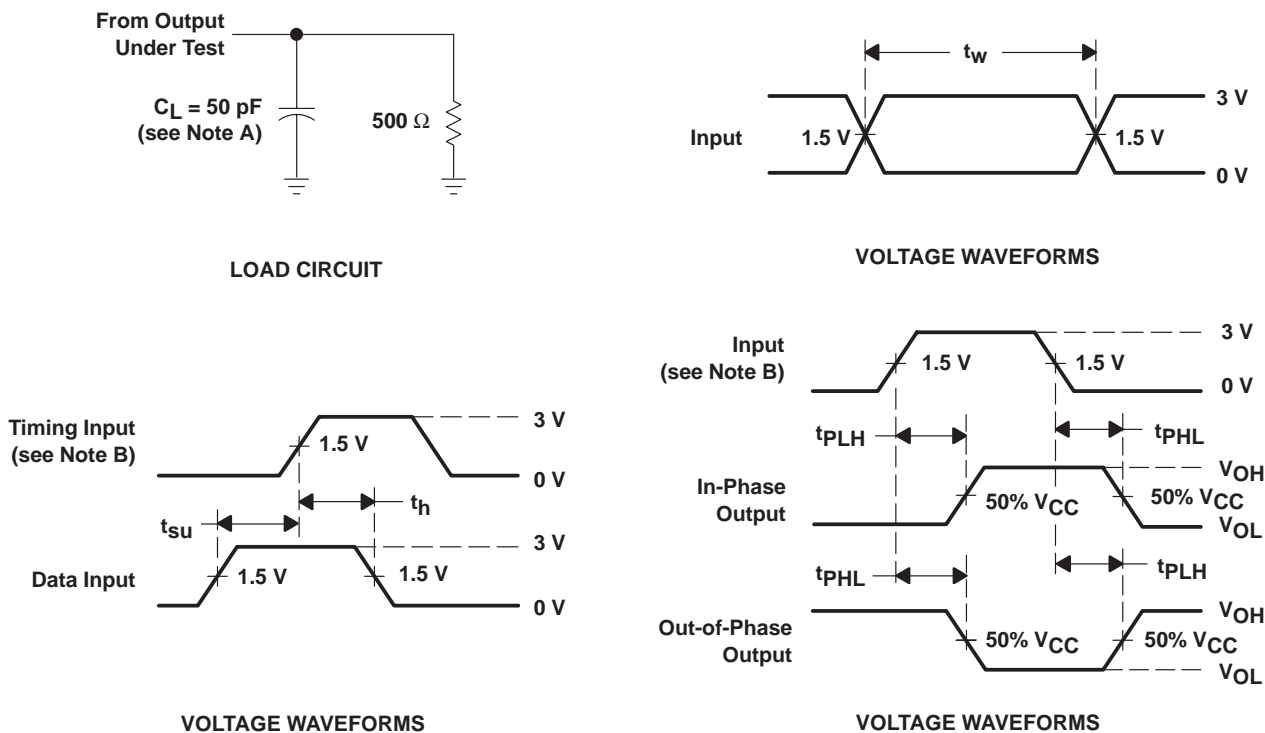
switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			20	65		40		MHz
t_{PHL}	$\overline{\text{CLR}}$	Any Q	4.6	6.7	11.1	3.8	12.1	ns
t_{PLH}	CLK	Any Q	4.1	5.5	8.8	2.7	9.7	ns
t_{PHL}			4.4	6.3	9.4	3.1	10.6	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	117	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT11898DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ACT11898DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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