

SN74F2244

25-Ω OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SDFS095B – NOVEMBER 1993 – REVISED JANUARY 1996

- 3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

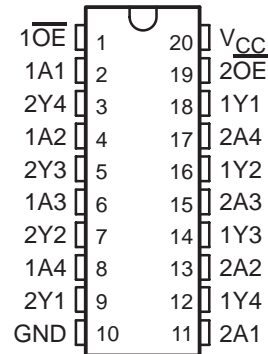
description

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 25-Ω resistors in the lower output circuit reduce ringing and eliminate the need for external resistors.

The SN74F2244 is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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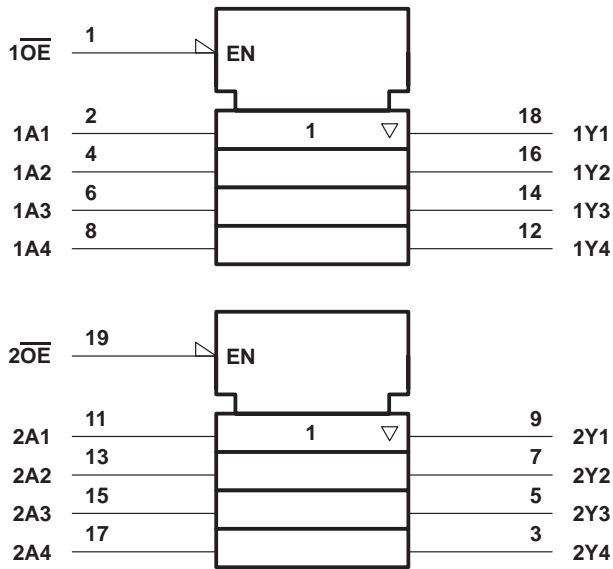
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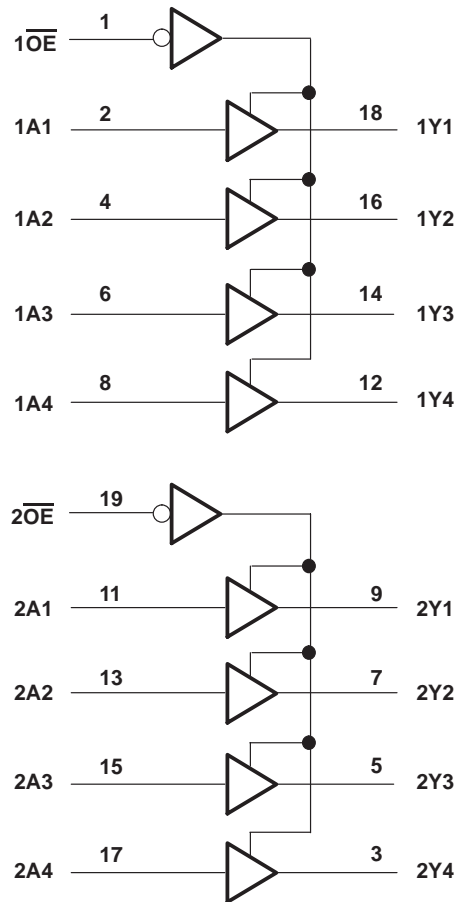
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-1.2 V to 7 V
Input current range, I_I	-30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Current into any output in the low state, I_O	30 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded if the input current ratings are observed.



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recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current			12	mA
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
V _{OH}		V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.4	2.8		V
		V _{CC} = 4.5 V	I _{OH} = -15 mA	2	2.3		
		V _{CC} = 4.75 V,	I _{OH} = -3 mA	2.7			
V _{OL}		V _{CC} = 4.5 V,	I _{OL} = 1 mA		0.2	0.5	V
		V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.5	0.75	
I _I		V _{CC} = 5.5 V,	V _I = 0.5 V			0.1	mA
I _{OZH}		V _{CC} = 5.5 V,	V _O = 7 V			50	μA
I _{OZL}		V _{CC} = 5.5 V,	V _O = 2.7 V			-50	μA
I _{IH}		V _{CC} = 5.5 V,	V _I = 2.7 V			20	μA
I _{IL}	Any \overline{OE} input	V _{CC} = 5.5 V,	V _I = 0.5 V			-1	mA
	Any A input					-1.6	
I _{OS} ‡		V _{CC} = 5.5 V,	V _O = 0	-100		-225	mA
I _{CC}		V _{CC} = 5.5 V, Outputs open	Outputs high		40	60	mA
			Outputs low		60	90	
			Outputs disabled		60	90	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 PF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C		V _{CC} = 4.5 V TO 5.5 V, C _L = 50 PF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN TO MAX§		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.5	7	1.5	7	ns
t _{PHL}			2.5	8	2	8	
t _{PZH}	\overline{OE}	Y	1.5	9	1	9.5	ns
t _{PZL}			2.5	11.5	2.5	12	
t _{PHZ}	\overline{OE}	Y	1.5	9	1	9.5	ns
t _{PLZ}			1.5	8.5	1.5	9.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



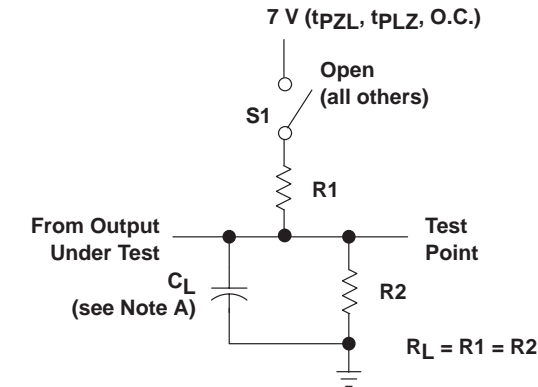
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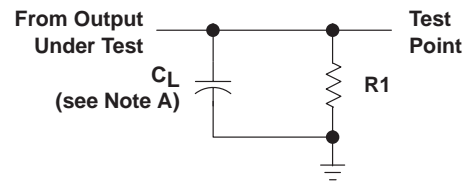
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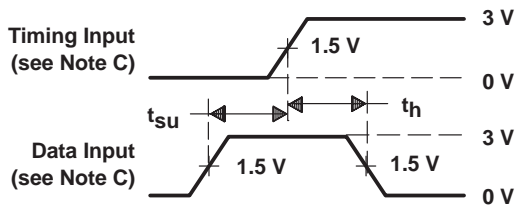
PARAMETER MEASUREMENT INFORMATION



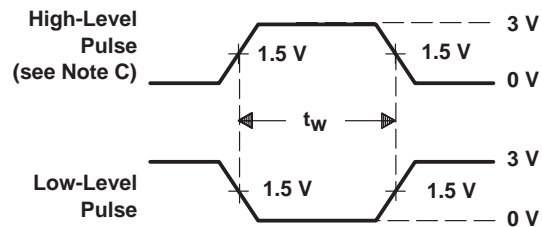
LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS



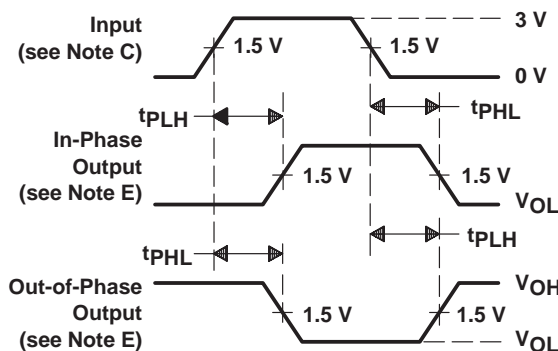
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



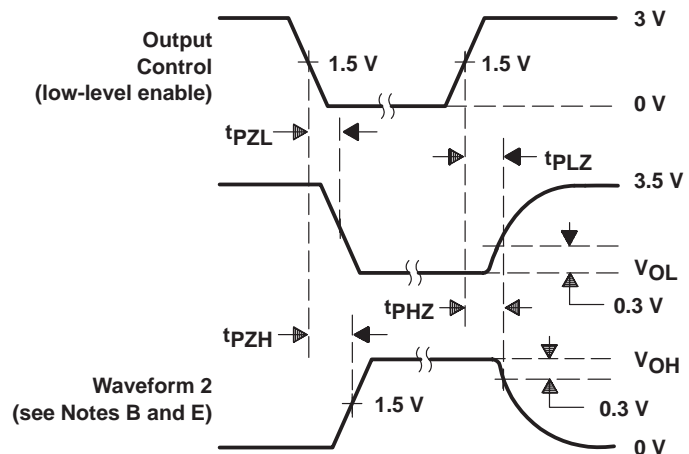
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74F2244DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
SN74F2244DBR	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
SN74F2244DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74F2244DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74F2244N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

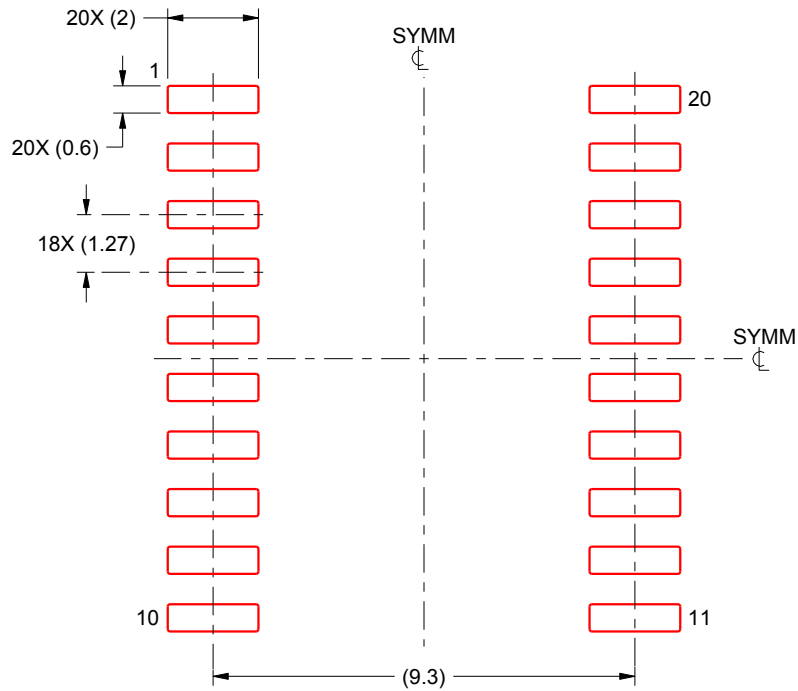
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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