National Semiconductor

September 2001

CLC428
Dual Wideband, Low Noise, Voltage Feedback Op Amp

General Description

The National CLC428 is a very high speed dual op amp that offers a traditional voltage-feedback topology featuring unity gain stability and slew enhanced circuitry. The CLC428's ultra low noise and very low harmonic distortion combine to form a very wide dynamic range op amp that operates from a single (5 to 12V) or dual (±5V) power supply.

Each of the CLC428's closely matched channels provides a 160MHz unity gain bandwidth with an ultra low input voltage noise density (2nV/$\sqrt{Hz}$). Very low 2nd/3rd harmonic distortion (-62dB) make the CLC428 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (16ns to 0.1%), the CLC428 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi-resolution analog-to-digital converters. Combining the CLC428's two tightly matched amplifiers in a single eight-pin SOIC reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

To reduce design times and assist in board layout, the CLC428 is supported by an evaluation board and a SPICE simulation model available from National.

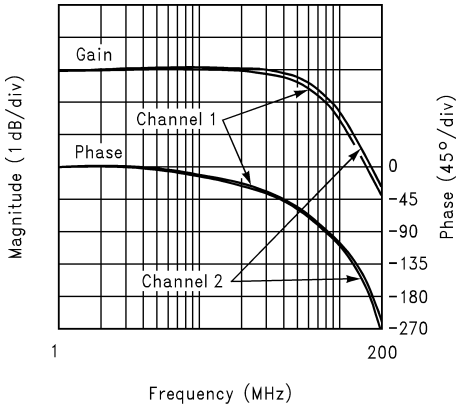
Features

- Wide unity gain bandwidth: 160MHz
- Ultra low noise: 2.0nV/$\sqrt{Hz}$
- Low Distortion: −78dBc 2nd (2MHz)
- Low Distortion: −62/−72dBc (10MHz)
- Settling time: 16ns to 0.1%
- Supply voltage range: ±2.5 to ±5 or single supply
- High output current: ±70mA

Applications

- General purpose dual op amp
- Low noise integrators
- Low noise active filters
- Diff-in/diff-out instrumentation amp
- Driver/receiver for transmission systems
- High speed detectors I/Q channel amplifiers

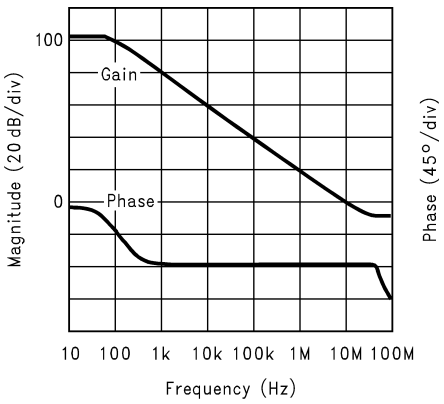
Channel Matching



DS012710-1

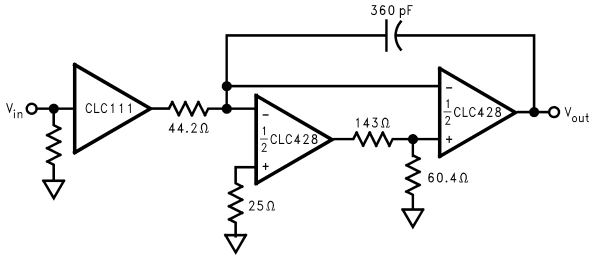
Typical Application

Frequency & Phase Response



DS012710-3

5-Decade Integrator



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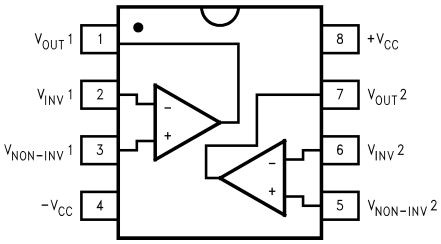
Connection Diagram



Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC428AJP	CLC428AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC428AJE	CLC428AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±7V
Short Circuit Current	(see note 6)
Common-Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	±10V
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C

Operating Ratings

Package	Thermal Resistance (θ_{JC})	(θ_{JA})
MDIP	60˚C/W	115˚C/W
SOIC	40˚C/W	115˚C/W

Electrical Characteristics

V_{CC} = ±5 V, A_V = +2V/V, R_f =100Ω, R_g = 100Ω, R_L = 100Ω; unless specified.

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Ambient Temperature		CLC428AJ	+25˚C	+25˚C	0 to +70˚C	−40 to +85˚C	
Frequency Domain Response							
	Gain Bandwidth Product	$V_{OUT} < 0.5V_{PP}$	135	100	80	70	MHz
	-3dB Bandwidth, A_V = +1	$V_{OUT} < 0.5V_{PP}$	160	120	90	80	MHz
	A_V = +2	$V_{OUT} < 0.5V_{PP}$	80	50	40	35	MHz
		$V_{OUT} < 5.0V_{PP}$	40	25	22	20	MHz
	Gain Flatness	$V_{OUT} < 0.5V_{PP}$					
	Peaking	DC to 200MHz	0.0	0.6	0.8	1.0	dB
	Rolloff	DC to 20MHz	0.05	0.5	0.7	0.7	dB
	Linear Phase Deviation	DC to 20MHz	0.2	1.0	1.5	1.5	deg
Time Domain Response							
	Rise and Fall Time	1V Step	5.5	7.5	9.0	10.0	ns
	Settling Time	2V Step to 0.1%	16	20	24	24	ns
	Overshoot	1V Step	1	5	10	10	%
	Slew Rate	5V Step	500	300	275	250	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion	$1V_{PP}$, 10MHz	−62	−50	−45	−43	dBc
	3rd Harmonic Distortion	$1V_{PP}$, 10MHz	−72	−60	−56	−56	dBc
	Equivalent Input Noise						
	Voltage	1MHz to 100MHz	2.0	2.5	2.8	2.8	$nV/\sqrt{Hz}$
	Current	1MHz to 100MHz	2.0	3.0	3.6	4.6	$pA/\sqrt{Hz}$
	Crosstalk	Input Referred, 10MHz	−62	−58	−58	−58	dB
Static, DC Performance							
	Open-Loop Gain		60	56	50	50	dB
	Input Offset Voltage (Note 3)		1.0	2.0	3.0	3.5	mV
	Average Drift		5	-	15	20	µV/˚C
	Input Bias Current (Note 3)		1.5	25	40	65	µA
	Average Drift		150	-	600	700	nA/˚C
	Input Offset Current		0.3	3	5	5	µA
	Average Drift		5	-	25	50	nA/˚C
	Power Supply Rejection Ratio (Note 4)		66	60	55	55	dB
	Common-Mode Rejection Ratio		63	57	52	52	dB
	Supply Current (Note 3)	Per Channel, R_L = ∞	11	12	13	15	mA

Electrical Characteristics (Continued)

V_{CC} = ±5 V, A_V = +2V/V, R_f =100Ω, R_g = 100Ω, R_L = 100Ω; unless specified.

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Miscellaneous Performance							
	Input Resistance	Common-Mode	500	250	125	125	kΩ
		Differential-Mode	200	50	25	25	kΩ
	Input Capacitance	Common-Mode	2.0	3.0	3.0	3.0	pF
		Differential-Mode	2.0	3.0	3.0	3.0	pF
	Output Resistance	Closed-Loop	0.05	0.1	0.2	0.2	Ω
	Output Voltage Range	R_L = ∞	±3.8	±3.5	±3.3	±3.3	V
		R_L = 100Ω	±3.5	±3.2	±2.6	±1.3	V
	Input Voltage Range	Common- Mode	±3.7	±3.5	±3.3	±3.3	V
	Output Current		±70	±50	±40	±20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: J-level: spec. is 100% tested at +25˚C, sample tested at +85˚C.

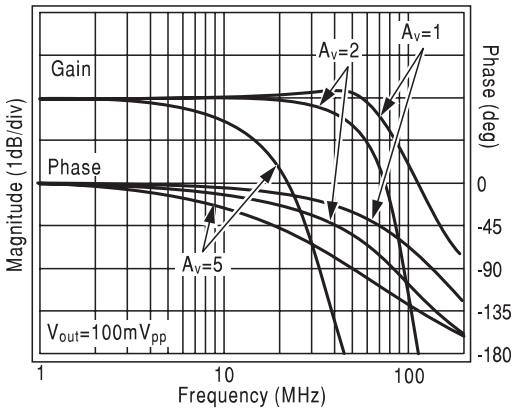
Note 4: J-level: spec. is 100% tested at +25˚C.

Note 5: Specifications guaranteed using 0.5V_{PP} but tested at 0.1 V_{PP}.

Note 6: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

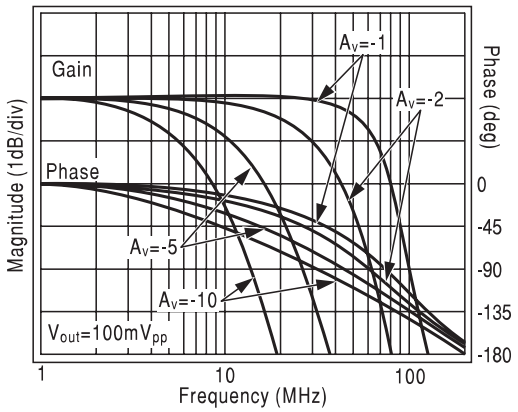
Typical Performance Characteristics (T_A = +25˚, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified)

Non-Inverting Frequency Response



DS012710-4

Inverting Frequency Response



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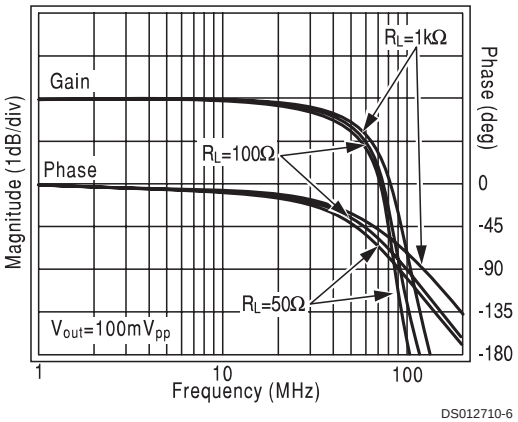
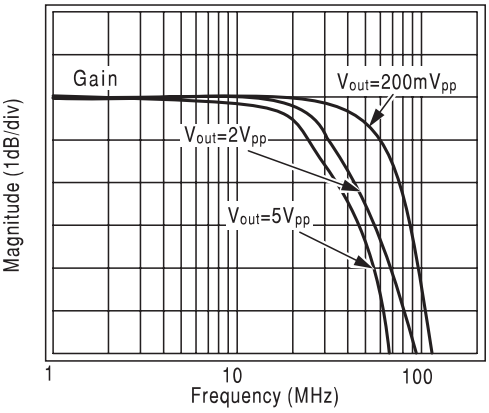
Frequency Response vs. Load Resistance



DS012710-6

Frequency Response vs. Output Amplitude



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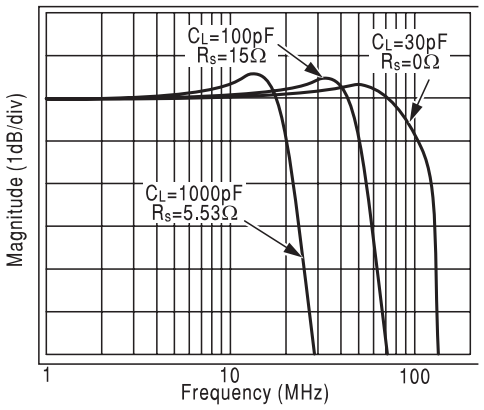
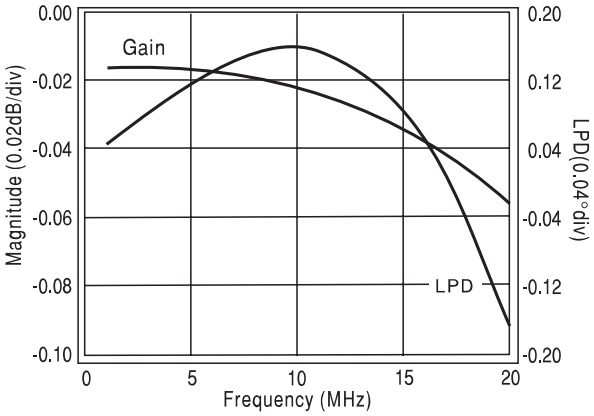
Typical Performance Characteristics (T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified) (Continued)

Frequency Response vs. Capacitive Load



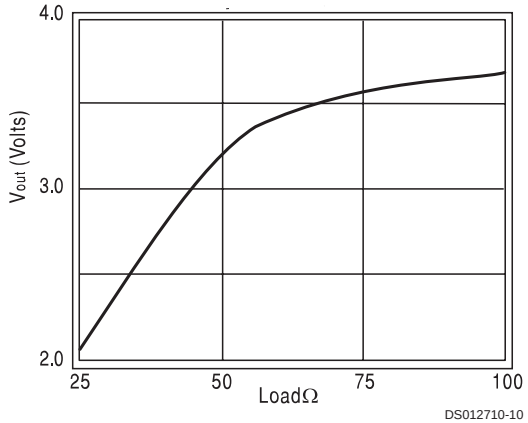
DS012710-8

Gain Flatness & Linear Phase Deviation



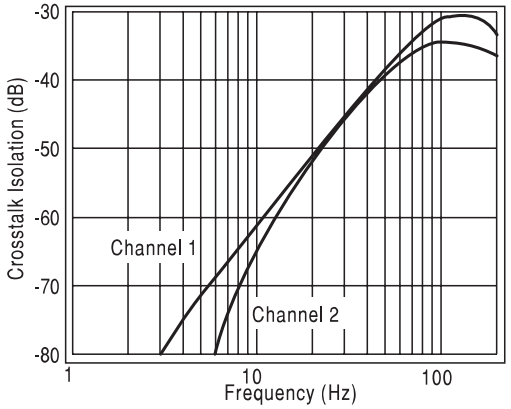
DS012710-9

Maximum Output Voltage vs. Load



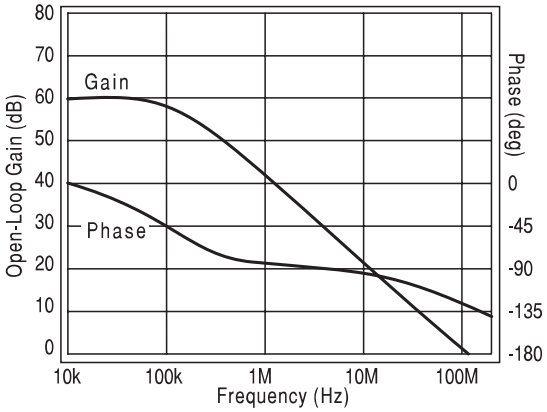
DS012710-10

Channel-to-Channel Crosstalk



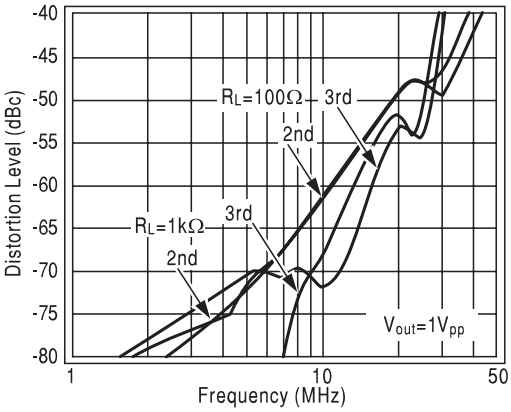
DS012710-11

Open-Loop Gain & Phase



DS012710-12

2nd and 3rd Harmonic Distortion



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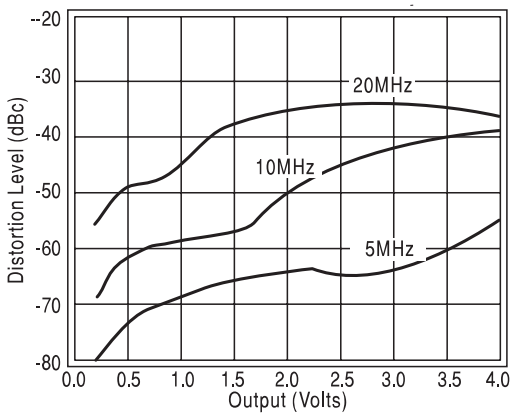
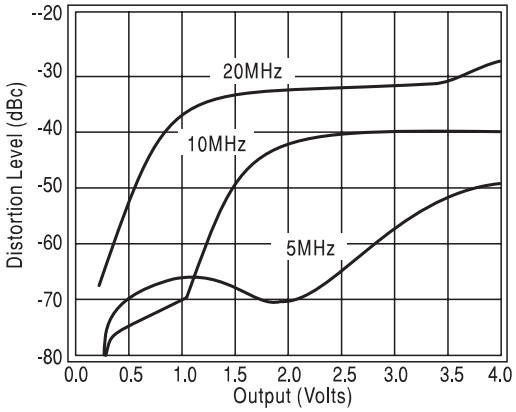
Typical Performance Characteristics (T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified) (Continued)

2nd Harmonic Distortion vs. Output Voltage



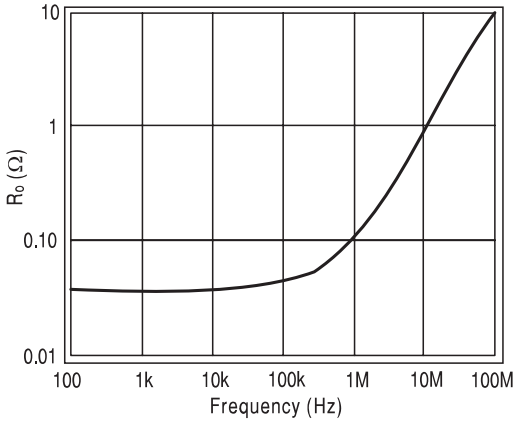
DS012710-14

3rd Harmonic Distortion vs. Output Voltage



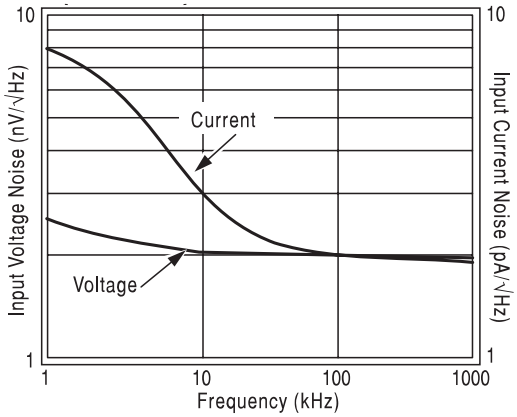
DS012710-15

Closed-Loop Output Resistance



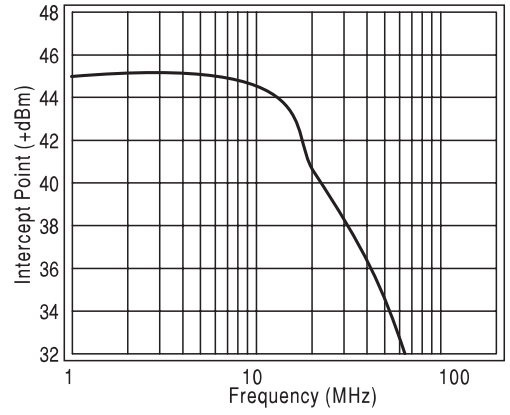
DS012710-16

Equivalent Input Noise



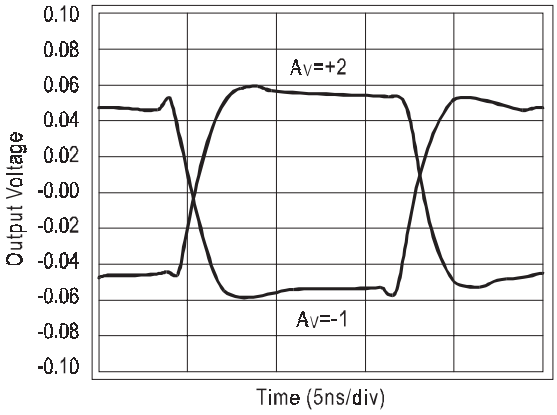
DS012710-17

2-Tone, 3rd Order Intermodulation Intercept



DS012710-18

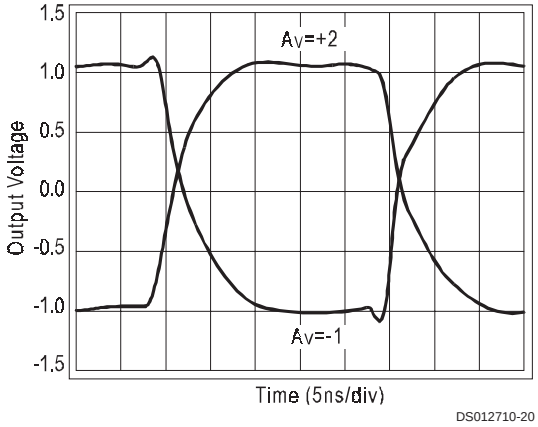
Pulse Response (V_{OUT} = 100V)



DS012710-19

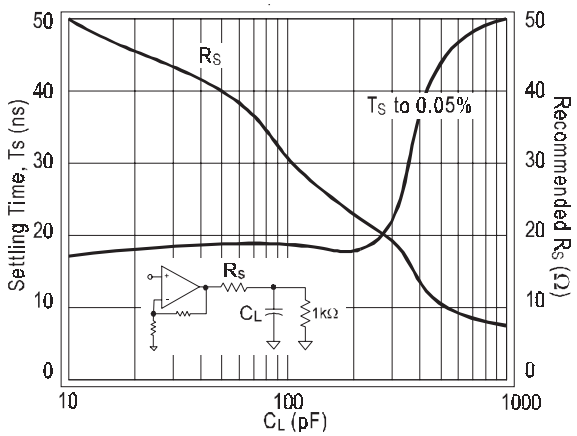
Typical Performance Characteristics (T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified) (Continued)

Pulse Response (V_{OUT} = 2V)



DS012710-20

Settling Time vs. Capacitive Load



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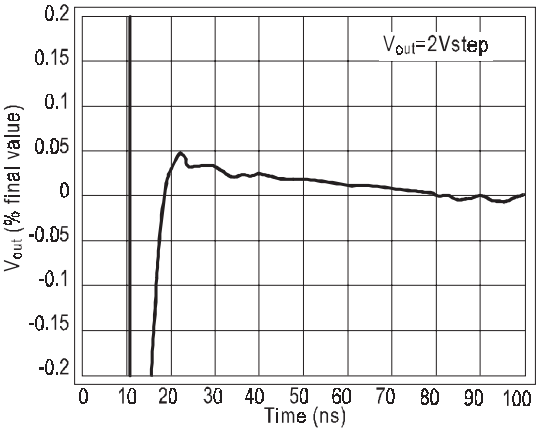
Short-Term Settling Time



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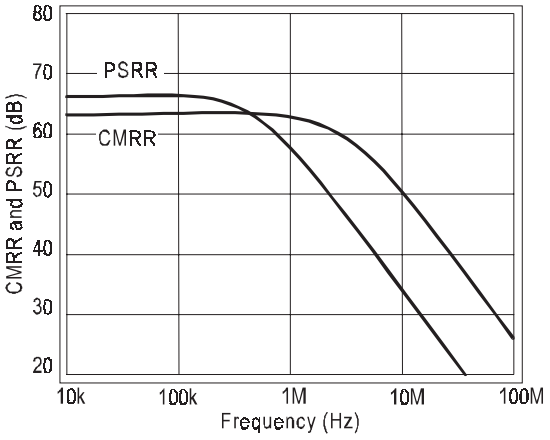
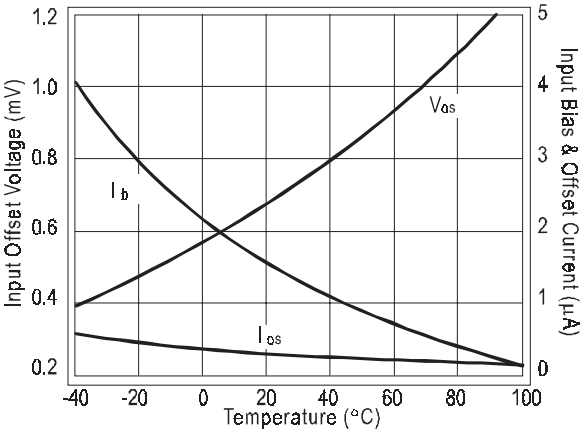
CMRR and PSRR



DS012710-23

Typical DC Errors vs. Temperature



DS012710-24

Application Division

Low Noise Design

Ultimate low noise performance from circuit designs using the CLC428 requires the proper selection of external resistors. By selecting appropriate low valued resistors for R_f and R_g, amplifier circuits using the CLC428 can achieve output noise that is approximately the equivalent voltage input noise of 2.0 nV/$\sqrt{Hz}$ multiplied by the desired gain (A_V).

Each amplifier in the CLC428 has an equivalent input noise resistance which is optimum for matching source impedances of approximately 1k. Using a transformer, any source can be matched to achieve the lowest noise design.

For even lower noise performance than the CLC428, consider the CLC425 or CLC426 at 1.05 and 1.6nV/$\sqrt{Hz}$, respectively.

DC Bias Currents and Offset Voltages

Cancellation of the output offset voltage due to input bias currents is possible with the CLC428. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (Vos) multiplied by the desired gain (Av). Comlinear Application Note OA-7 offers several solutions to further reduce the output offset.

Output and Supply Considerations

With ±5V supplies, the CLC428 is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the CLC428's output current capability, typically 80mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled 'Settling Time vs. Capacitive Load' in the Typical Performance section.

Layout

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. National suggests the 730038 (through-hole) or the 730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

Analog Delay Circuit (All-Pass Network)

The circuit in *Figure 1* implements an all-pass network using the CLC428. A wide bandwidth buffer (CLC111) drives the circuit and provides a high input impedance for the source. As shown in *Figure 2*, the circuit provides a 13.1ns delay (with R = 40.2Ω, C = 47pF). R_f and R_g should be of equal and low value for parasitic insensitive operation.

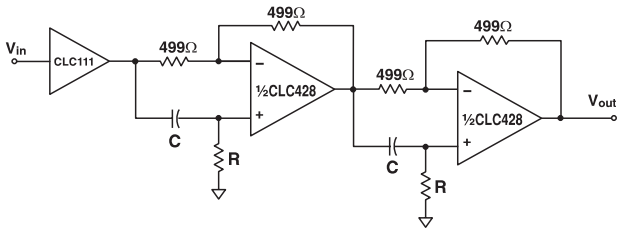


FIGURE 1.

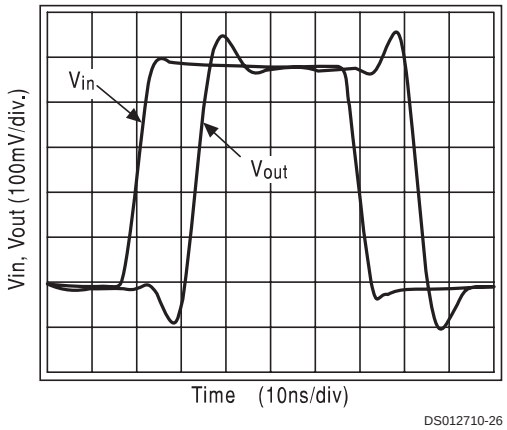


FIGURE 2. Delay Circuit Response to 0.5V Pulse

The circuit gain is +1 and the delay is determined by the following equations.

$$\tau_{delay} = 2(2RC + T_d) \quad (1)$$

$$T_d = \frac{1}{360}\frac{d\phi}{df}; \quad (2)$$

where T_d is the delay of the op amp at A_V=+1.

The CLC428 provides a typical delay of 2.8ns at its −3dB point.

Full Duplex Digital or Analog Transmission

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The CLC428's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in *Figure 3*, one of the CLC428's amps is used as a 'driver' and the other as a difference 'receiver' amplifier. The output impedance of the 'driver' is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The 'driver' op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms differential amplifier for the signals transmitted by driver A_2 (B_2). If the coax cable is lossless and R_f equals R_g, receiver A_2 (B_1) will then reject the signals from driver A_1 (B_1) and pass the signals from driver B_1 (A_1).

Application Division (Continued)

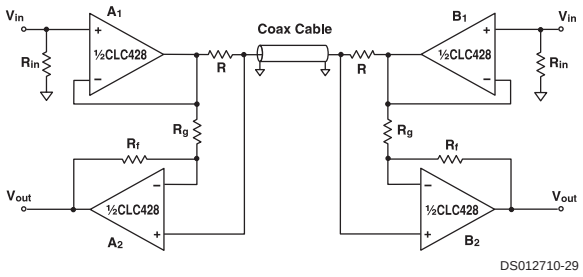


FIGURE 3.

The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2} V_{in_{A(B)}} \left[1 - \frac{R_f}{R_g}\right] + \frac{1}{2} V_{in_{B(A)}} \left[1 + \frac{R_f}{R_g}\right] \quad (3)$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of *Figure 4* shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

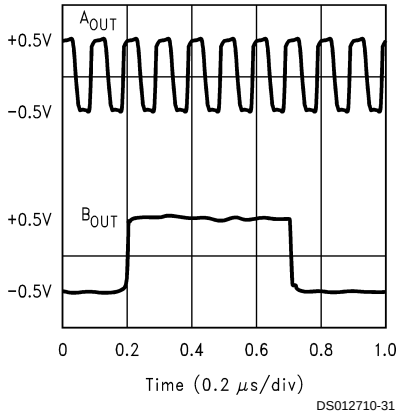


FIGURE 4.

Five Decade Integrator

A composite integrator, as shown in *Figure 5*, uses the CLC428 dual op amp to increase the circuits' usable frequency range of operation. The transfer function of this circuit is:

$$V_O = \frac{1}{RC} \int V_{IN}\, dt \quad (4)$$

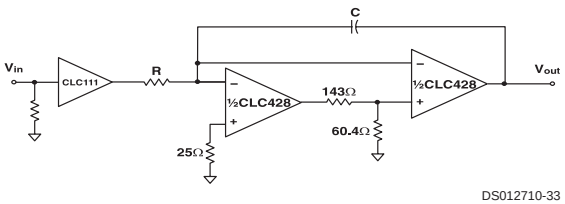


FIGURE 5.

A resistive divider made from the 143Ω and 60.4Ω resistors was chosen to reduce the loop-gain and stabilize the network. The CLC428 composite integrator provides integration over five decades of operation. R and C set the integrator's gain. *Figure 6* shows the frequency and phase response of the circuit in *Figure 5* with R = 44.2Ω and C = 360pF.

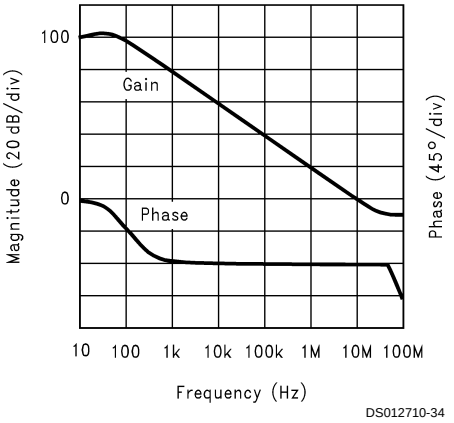


FIGURE 6.

Positive Peak Detector

The CLC428's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in *Figure 7*.

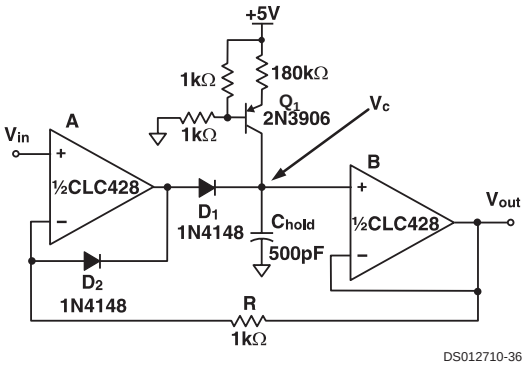


FIGURE 7.

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the circuit's performance is shown in *Figure 8* with a 1MHz sinusoidal input.

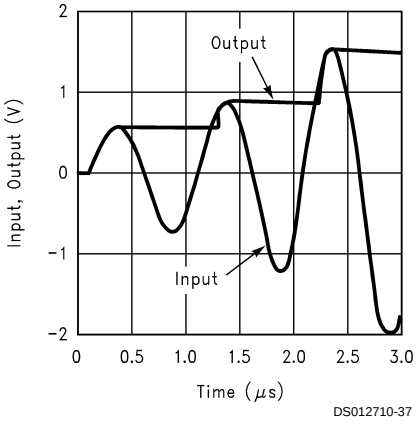


FIGURE 8.

Application Division (Continued)

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when V_{in} is less than V_C. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

Adjustable or Bandpass Equalizer

A 'boost' equalizer can be made with the CLC428 by summing a bandpass response with the input signal, as shown in *Figure 9*.

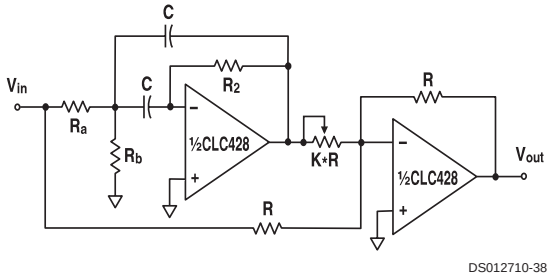


FIGURE 9.

The overall transfer function is shown in Eq. 5.

$$\frac{V_{out}}{V_{in}} = \left[\frac{R_b}{K(R_a + R_b)}\right] \frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} - 1 \quad (5)$$

To build a boost circuit, use the design equations Eq. 6 and Eq. 7.

$$\frac{R_2 C}{2} = \frac{Q}{\omega_o} \quad (6)$$

$$2C\,(R_a \| R_b) = \frac{1}{Q\omega_o}$$

Select R_2 and C using Eq. 6. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use Eq. 7 to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Eq. 8.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \quad (7)$$

Figure 10 shows an example of the response of the circuit of Figure 9, where f_o is 2.3MHz. The component values are as follows: R_a=2.1KΩ, R_2 = 68.5Ω, R_2 = 4.22kΩ, R = 500Ω, KR = 50Ω, C = 120pF.

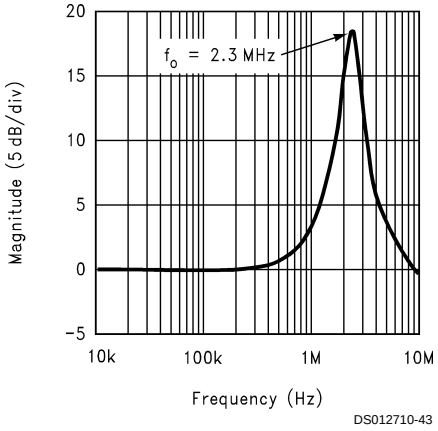
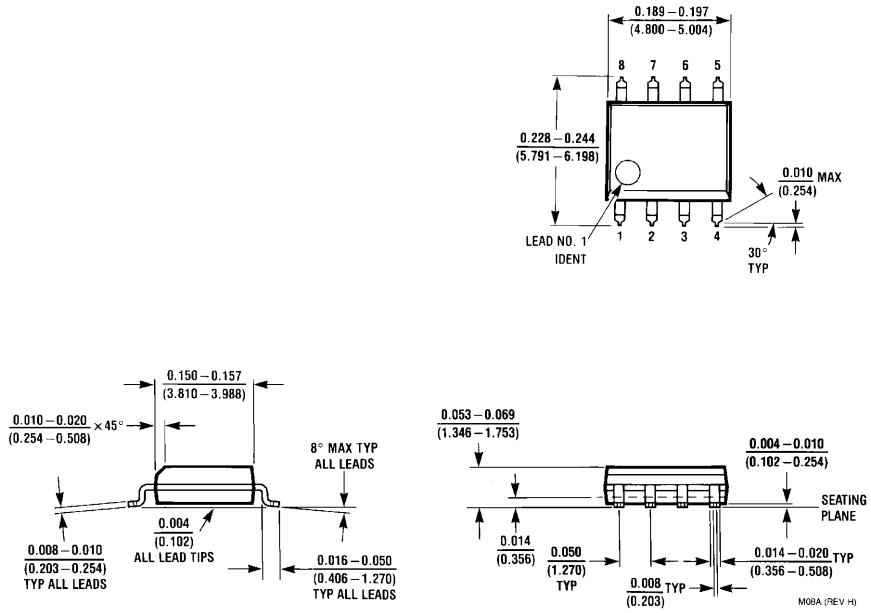
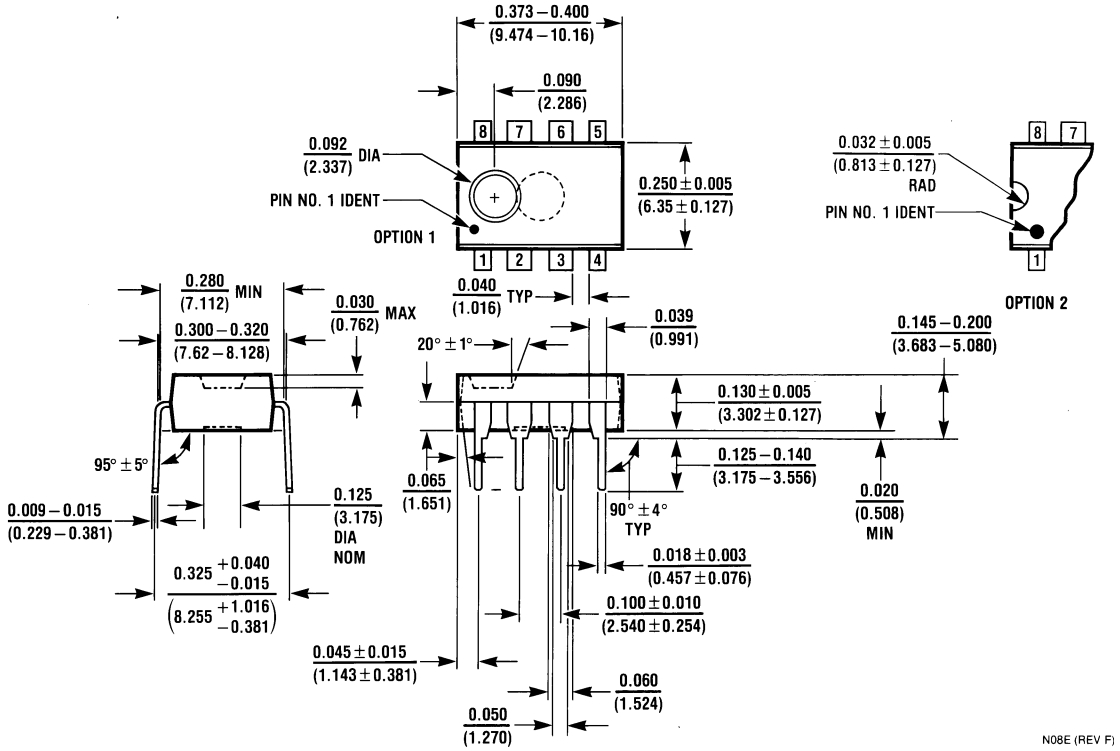


FIGURE 10.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



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