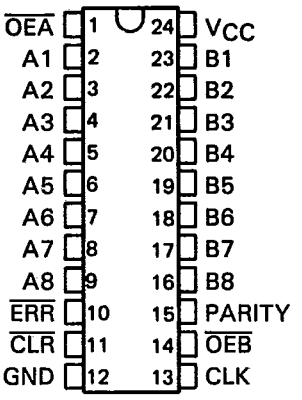
SN74ALS29833, SN74ALS29834
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

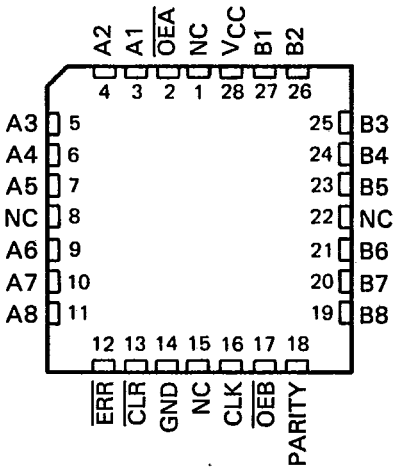
D2990, FEBRUARY 1987—REVISED JULY 1987

- **Functionally Similar to AMD AM29833 and AM29834**
- **High-Speed Bus Transceivers with Parity Generator/Checker**
- **Parity Error Flag with Open-Collector Outputs**
- **Has a Register for Storage of the Parity Error Flag**
- **Choice of True ('ALS29833) or Inverting ('ALS29834) Logic**
- **Package Options Include Plastic "Small Outline" Package, Plastic Chip Carriers, and Standard Plastic 300-mil Dips**

SN74ALS' . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS' . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

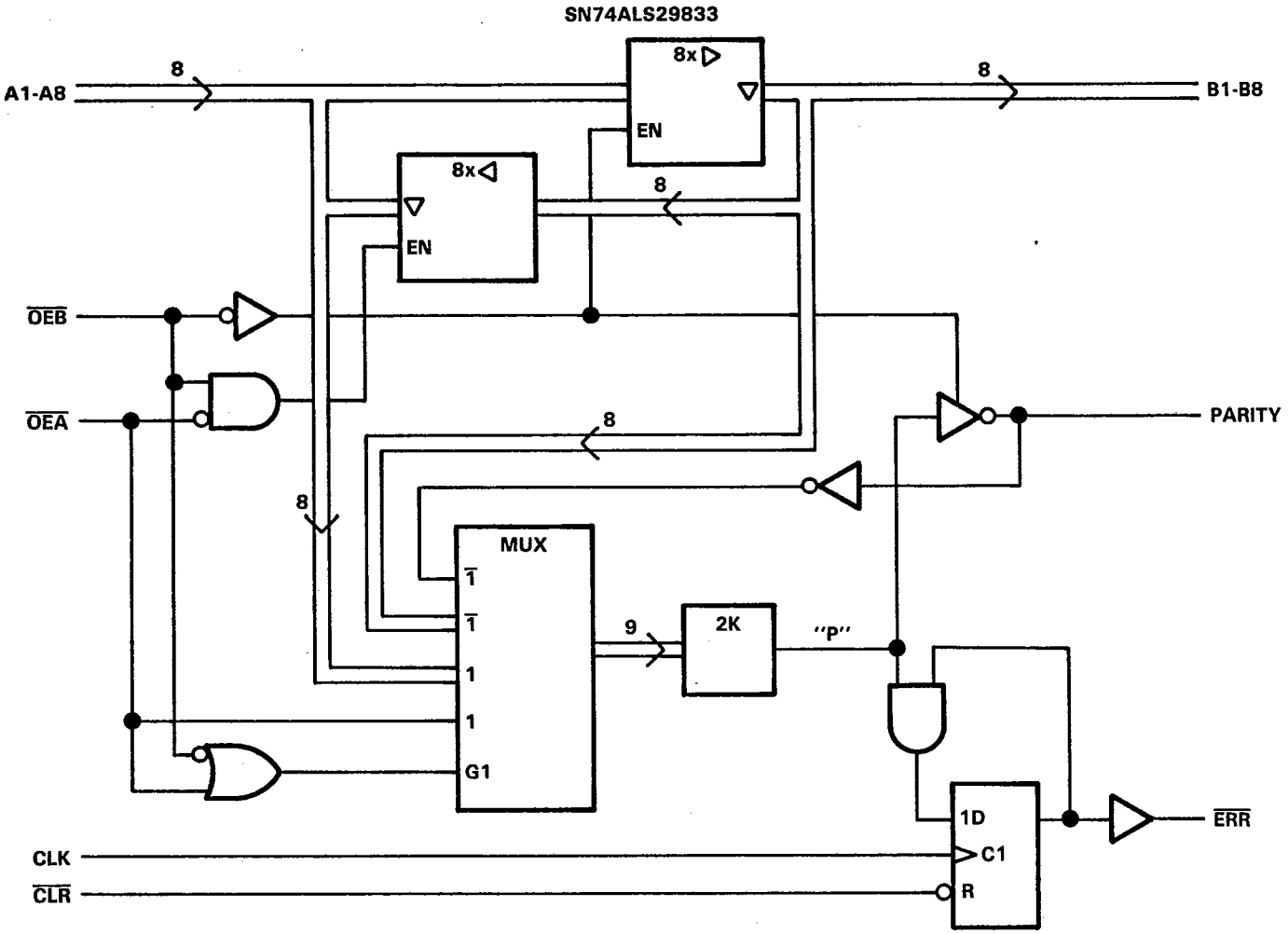
The SN74ALS29833 and SN74ALS29834 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY), and monitors the parity of the I/O ports with an open-collector parity error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74ALS833 and SN74ALS834 are characterized for operation from 0°C to 70°C.

SN74ALS29833
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	Bi† Σ of H's	A	B	PARITY	$\overline{ERR}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A Data to B Bus and Generate Parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation‡
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ In this mode the $\overline{ERR}$ output, when clocked, shows inverted parity of the A bus.

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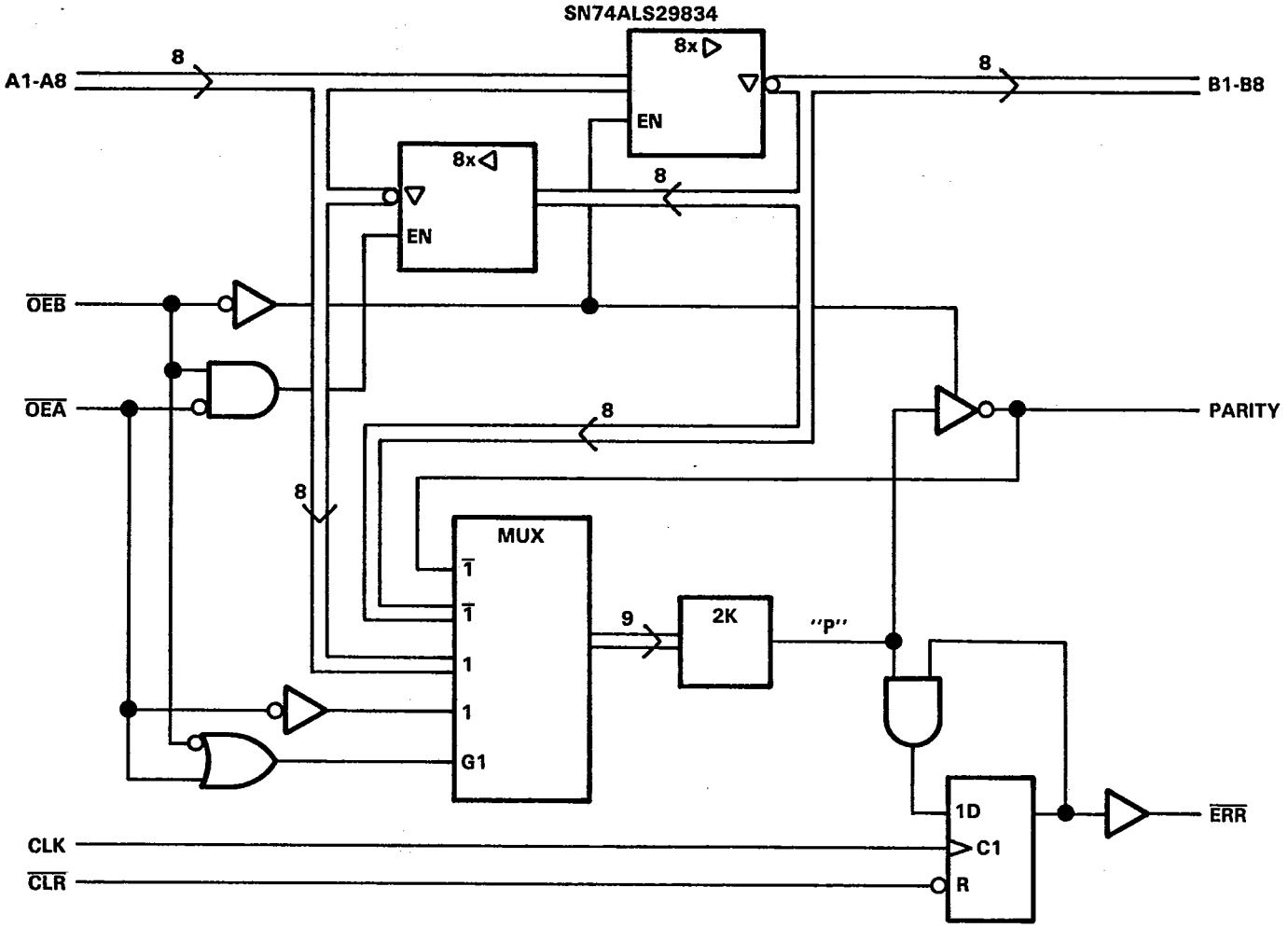
logic diagram (positive logic)

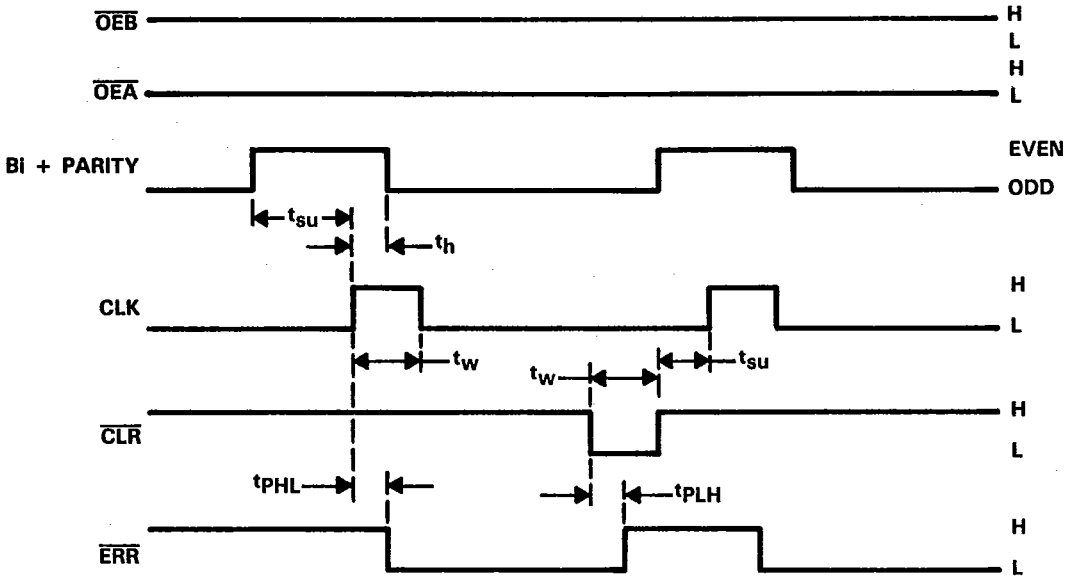


FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	Bi† Σ of L's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ Data to B Bus and Generate Parity
H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output state assumes a high output pre-state.
§ In this mode the $\overline{ERR}$ output, when clocked, shows noninverted parity of the A bus.

error flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	SAMPLE
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	CLEAR

$\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$				5.5	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	CLK high	10			ns
		CLK low	10			
		$\overline{CLR}$ low	10			
t_{su}	Setup time before CLK↑	Bi and PARITY	15			ns
		$\overline{CLR}$ inactive	15			
t_h	Hold time, Bi and PARITY after CLK↑		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.75 V	I_{OH} = −15 mA	2.4			V
			I_{OH} = −24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.75 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}‡	Data	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.2	mA
	Control					−0.75	
I_O§		V_{CC} = 5.25 V,	V_O = 0	−75		−250	mA
I_{CC}		V_{CC} = 5.25 V			70	100	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

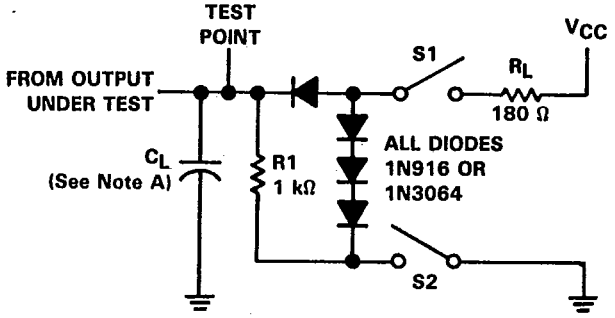
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = MIN to MAX		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 50 pF		4.5	6		8	ns
t_{PHL}					5.5	7		10	
t_{PLH}			C_L = 300 pF		9	12		15	
t_{PHL}					10	14		16	
t_{PLH}	A	PARITY	C_L = 50 pF		10	13		15	ns
t_{PHL}					12	15		19	
t_{PLH}			C_L = 300 pF		15	19		22	
t_{PHL}					18	22		25	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		11	15		19	ns
t_{PZL}					11	15		19	
t_{PZH}			C_L = 300 pF		25	32		35	
t_{PZL}					25	32		35	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 5 pF		4	6		9	ns
t_{PLZ}					4	6		9	
t_{PHZ}			C_L = 50 pF		9	12		15	
t_{PLZ}					4	8		10	
t_{PHL}	CLK	$\overline{ERR}$	C_L = 50 pF		10	13		16	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	C_L = 50 pF		16	20		25	ns
t_{PLH}	$\overline{OEA}$	PARITY	C_L = 50 pF		11	14		17	ns
t_{PHL}					12	15		19	
t_{PLH}			C_L = 300 pF		15	19		22	
t_{PHL}					17	22		25	

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = MIN to MAX		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 50 pF		6	8		10	ns
t_{PHL}					6	8		10	
t_{PLH}			C_L = 300 pF		10	13		15	
t_{PHL}					10	13		15	
t_{PLH}	A	PARITY	C_L = 50 pF		10	13		17	ns
t_{PHL}					10	13		17	
t_{PLH}			C_L = 300 pF		16	20		25	
t_{PHL}					16	20		25	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		12	15		19	ns
t_{PZL}					12	15		19	
t_{PZH}			C_L = 300 pF		25	32		35	
t_{PZL}					25	32		35	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 5 pF		4	6		9	ns
t_{PLZ}					4	6		9	
t_{PHZ}			C_L = 50 pF		9	12		15	
t_{PLZ}					4	8		10	
t_{PHL}	CLK	$\overline{ERR}$	C_L = 50 pF		10	13		16	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	C_L = 50 pF		19	24		28	ns
t_{PLH}	$\overline{OEA}$	PARITY	C_L = 50 pF		12	15		19	ns
t_{PHL}					12	15		19	
t_{PLH}			C_L = 300 pF		17	22		25	
t_{PHL}					17	22		25	

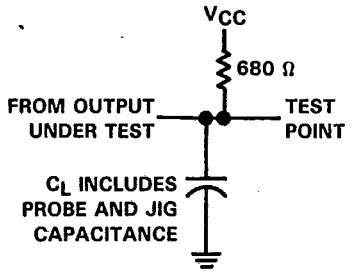
PARAMETER MEASUREMENT INFORMATION



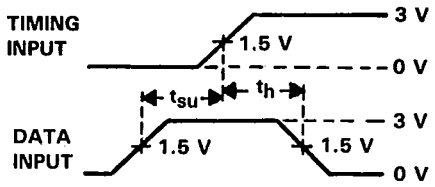
LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

SWITCH POSITION TABLE

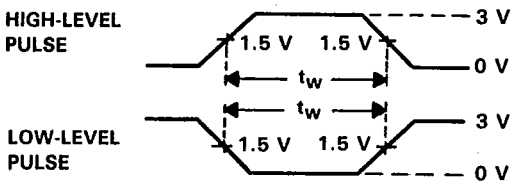
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



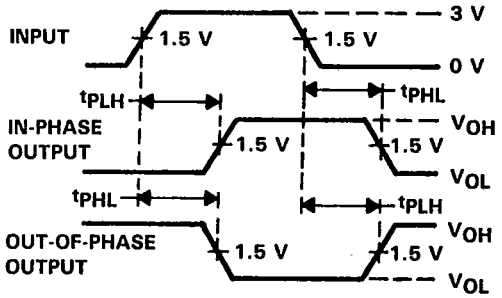
LOAD CIRCUIT 2 ERROR FLAG OUTPUT



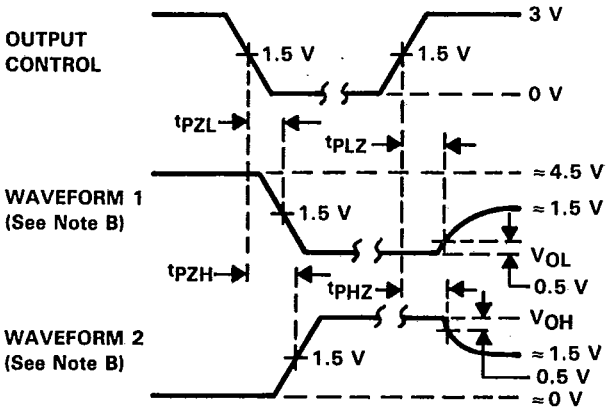
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1