



MOTOROLA

Dual 2-Wide AND/OR/INVERT Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30401

Military 54LS51



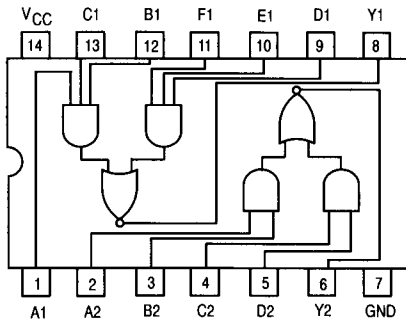
AVAILABLE AS:

- 1) JAN: JM38510/30401BXA
- 2) SMD: N/A
- 3) 883: 54LS51/BXAJC

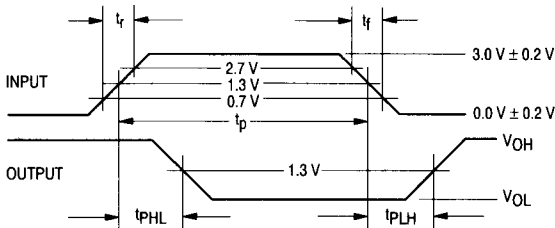
X = CASE OUTLINE AS FOLLOWS:
 PACKAGE: CERDIP: C
 CERFLAT: D
 LCC: 2

THE LETTER "M" APPEARS
 BEFORE THE / ON LCC.

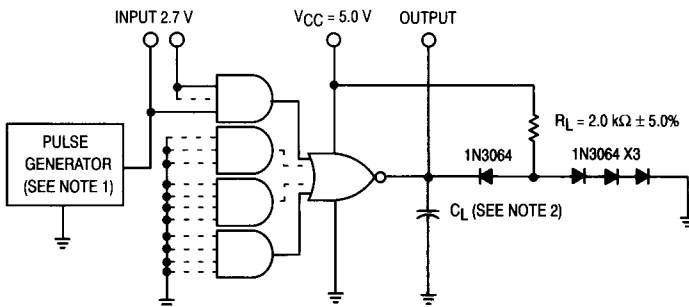
LOGIC DIAGRAM



WAVEFORMS



AC TEST CIRCUIT



PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
A2	2	2	3	GND
B2	3	3	4	VCC
C2	4	4	6	VCC
D2	5	5	8	GND
Y2	6	6	9	VCC
GND	7	7	10	GND
Y1	8	8	12	VCC
D1	9	9	13	VCC
E1	10	10	14	GND
F1	11	11	16	VCC
B1	12	12	18	VCC
C1	13	13	19	GND
VCC	14	14	20	VCC

BURN-IN CONDITIONS:

VCC = 5.0 V MIN/6.0 V MAX

NOTES:

- The pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $PRR \leq 1.0$ MHz, $t_p = 0.5$ μ s and $Z_{OUT} = 50$ Ω .
- $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance, without package in test fixture.
- $R_L = 2.0$ k Ω $\pm 5.0\%$.
- Voltage measurements are to be made with respect to network ground terminal.
- Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

54LS51

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = - 400 μA, V _{IL} = 0.7 V, V _{IN} = 5.5 V on other inputs.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V, V _{IN} = 0 V on other inputs.
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs = 0 V.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs = 0 V.
I _{IL}	Logical "0" Input Current	- 150	- 380	- 150	- 380	- 150	- 380	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs = 5.5 V.
I _{OS}	Output Short Circuit Current	- 15	- 100	- 15	- 100	- 15	- 100	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), V _{OUT} = 0 V.
I _{CCH}	Power Supply Current		1.6		1.6		1.6	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
I _{CCL}	Power Supply Current		2.8		2.8		2.8	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL} t _{PHL}	Propagation Delay /Data-Output Output High-Low	3.0 —	22 20	3.0 —	30 25	3.0 —	30 25	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH} t _{PLH}	Propagation Delay /Data-Output Output Low-High	3.0 —	19 20	3.0 —	30 25	3.0 —	30 25	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTE:

1. The limits specified for C_L = 15 pF are guaranteed but not tested.

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