MOTOROLA

4-Bit Up/Down Binary Counter With Clear

ELECTRICALLY TESTED PER:
MIL-M-38510/31508

Military 54LS193

The 54LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High-Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High-Speed Termination Effects

AVAILABLE AS:

1) JAN: JM38510/31508BXA
2) SMD: 7600601
3) 883: 54LS193/BXAJC

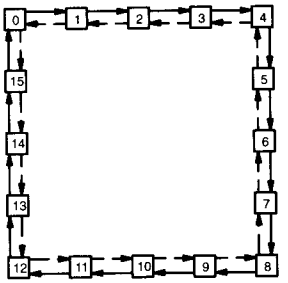
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

Pin Names		Loading (Note a) HIGH	Loading (Note a) LOW
CP_U	Count UP Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock	0.5 U.L.	0.25 U.L.
MR	Pulse Input Asynchronous Master Reset	0.5 U.L.	0.25 U.L.
$\overline{PL}$	(Clear) Input Asynchronous Parallel Load	0.5 U.L.	0.25 U.L.
P_n	(Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_n	Parallel Data Inputs	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5 U.L.
	Terminal Count Up (Carry) Output (Note b)		

NOTES:
a. One TTL Unit Load (U.L.) = 40 µA HIGH/ 1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

STATE DIAGRAM



LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$

$\overline{TC}_D = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
P_1	1	1	2	V_{CC}
Q_1	2	2	3	V_{CC}
Q_0	3	3	4	V_{CC}
CP_D	4	4	5	V_{CC}
CP_U	5	5	7	V_{CC}
Q_2	6	6	8	V_{CC}
Q_3	7	7	9	V_{CC}
GND	8	8	10	GND
P_3	9	9	12	V_{CC}
P_2	10	10	13	V_{CC}
$\overline{PL}$	11	11	14	GND
$\overline{TC}_U$	12	12	15	OPEN
$\overline{TC}_D$	13	13	17	V_{CC}
MR	14	14	18	GND
P_0	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

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FUNCTIONAL DESCRIPTION

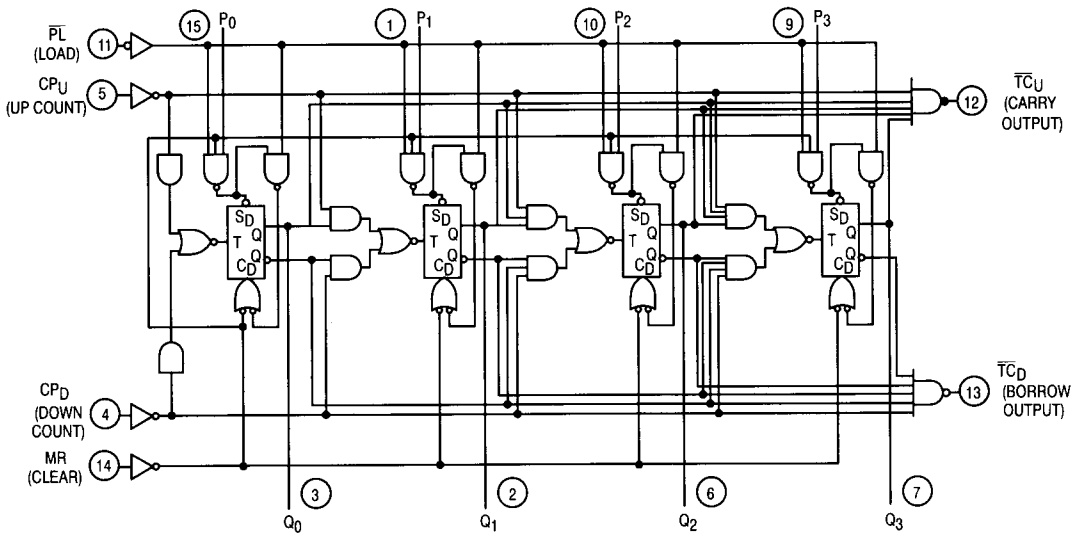
The 'LS192 and 'LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the 'LS192 decade counter and 'LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) Outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the 'LS192, 15 for the 'LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM



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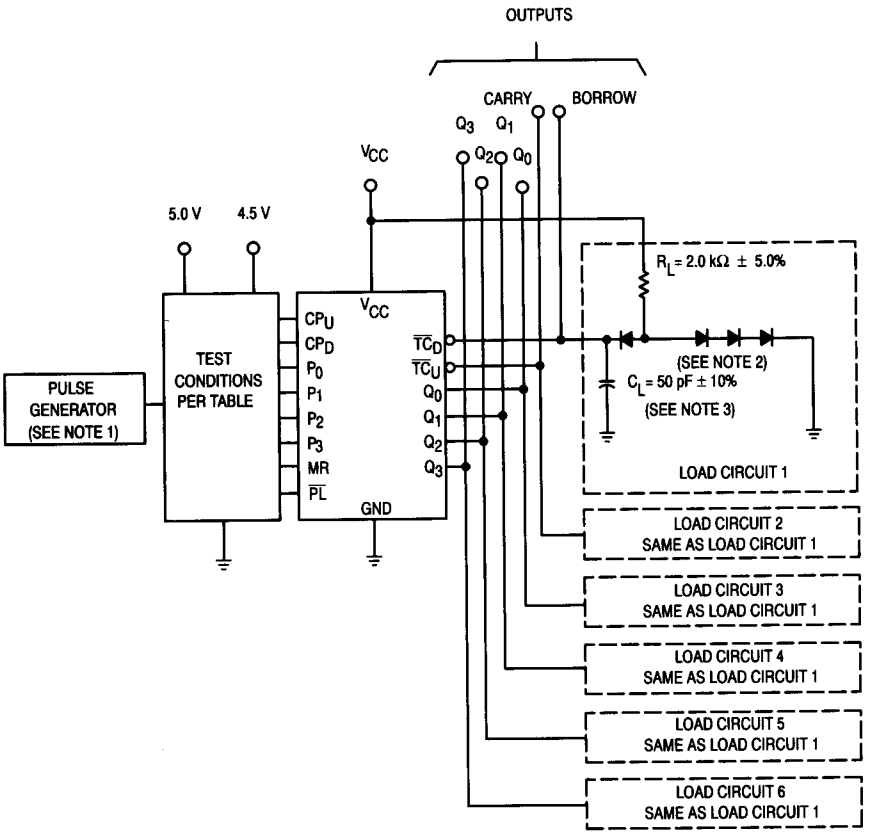
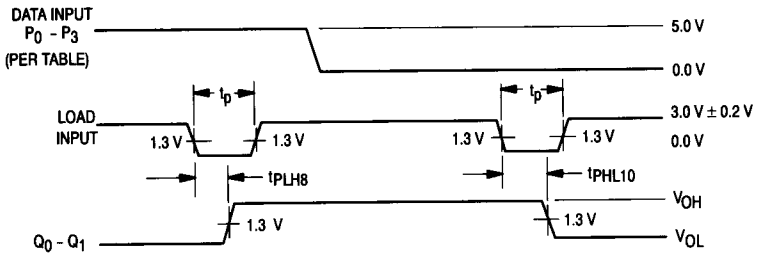
AC TEST CIRCUIT

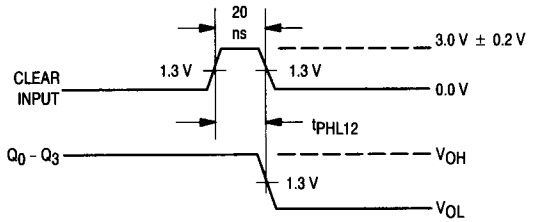


WAVEFORMS

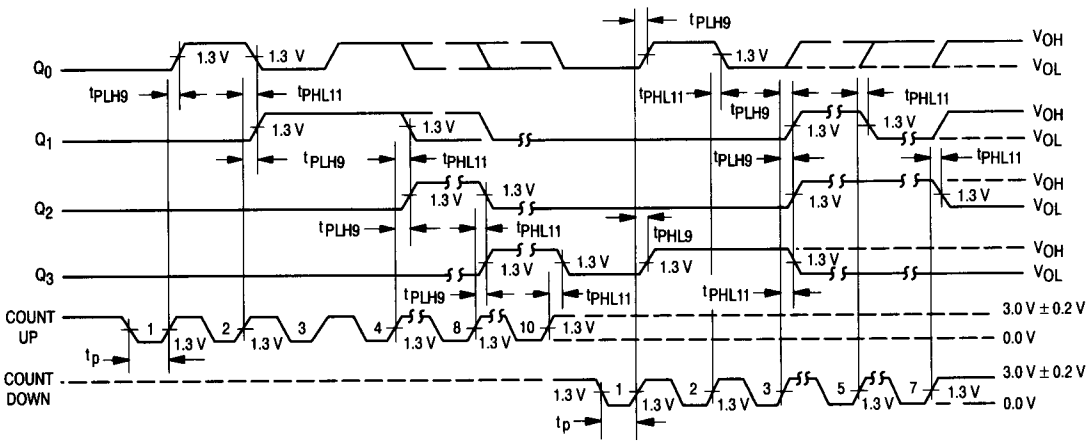


REFERENCE NOTES ON PAGE 5-271

CLEAR SWITCHING VOLTAGE WAVEFORM



SERIAL LOADED VOLTAGE WAVEFORMS



NOTES:

1. The load and count pulse generators have the following characteristics: V_{gen} = 3.0 V, t_p = 0.5 µs, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns between 0.7 V and 2.7 V and PRR ≤ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. Voltage values are with respect to ground terminal.
5. f_{MAX}: $t_r = t_f \leq 6.0$ ns.
6. The clear pulse generator has the following characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns between 0.7 V and 2.7 V, $t_{w(clear)}$ = 20 ns.
7. R_L = 2.0 kΩ ± 5.0%.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = – 0.4 mA, V_{IN} = 2.0 V, other inputs are open, MR & $\overline{PL}$ = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 0.7 V, other inputs are open, P_0, P_3 & MR = 0.7 V or 2.0 V.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, MR & $\overline{PL}$ = 5.5 V or 2.7 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	– 120	– 360	– 120	– 360	– 120	– 360	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, $\overline{PL}$ & MR = GND, other inputs are open.
I_{IL}	Logical "0" Input Current	– 120	– 360	– 120	– 360	– 120	– 360	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V ($\overline{PL}$), other inputs are open.
I_{IL}	Logical "0" Input Current	– 120	– 360	– 120	– 360	– 120	– 360	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V ($\overline{TC}$ & MR), other inputs are open.
I_{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		34		34		34	mA	V_{CC} = 5.5 V, V_{IN} = GND ($\overline{PL}$ & MR), other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL10} t_{PHL10}	Propagation Delay /Data-Output $\overline{PL}$ to Q Outputs	3.0 —	45 40	3.0 —	63 58	3.0 —	63 58	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH8} t_{PLH8}	Propagation Delay /Data-Output $\overline{PL}$ to Q Outputs	3.0 —	45 40	3.0 —	63 58	3.0 —	63 58	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL11} t_{PHL11}	Propagation Delay CP_D or CP_U to Q Outputs	3.0 —	52 47	3.0 —	73 68	3.0 —	73 68	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH9} t_{PLH9}	Propagation Delay CP_D or CP_U to Q Outputs	3.0 —	43 38	3.0 —	60 55	3.0 —	60 55	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL12} t_{PHL12}	Propagation Delay MR (Clear) to Q Outputs	3.0 —	40 35	3.0 —	56 51	3.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX}	Input Clock Frequency	22		22		22		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
f_{MAX}	Input Clock Frequency	25						MHz	V_{CC} = 5.0 V, C_L = 15 pF.

NOTE:
1. The limit specified for C_L = 15 pF are guaranteed but not tested.

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