INTEGRATED CIRCUITS

UNITRODE

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters

- Low Start Up Current (<0.5mA)

- Trimmed Oscillator Discharge Current

- Automatic Feed Forward Compensation

- Pulse-by-Pulse Current Limiting

- Enhanced Load Response Characteristics

- Under-Voltage Lockout With Hysteresis

- Double Pulse Suppression

- High Current Totem Pole Output

- Internally Trimmed Bandgap Reference

- 500kHz Operation
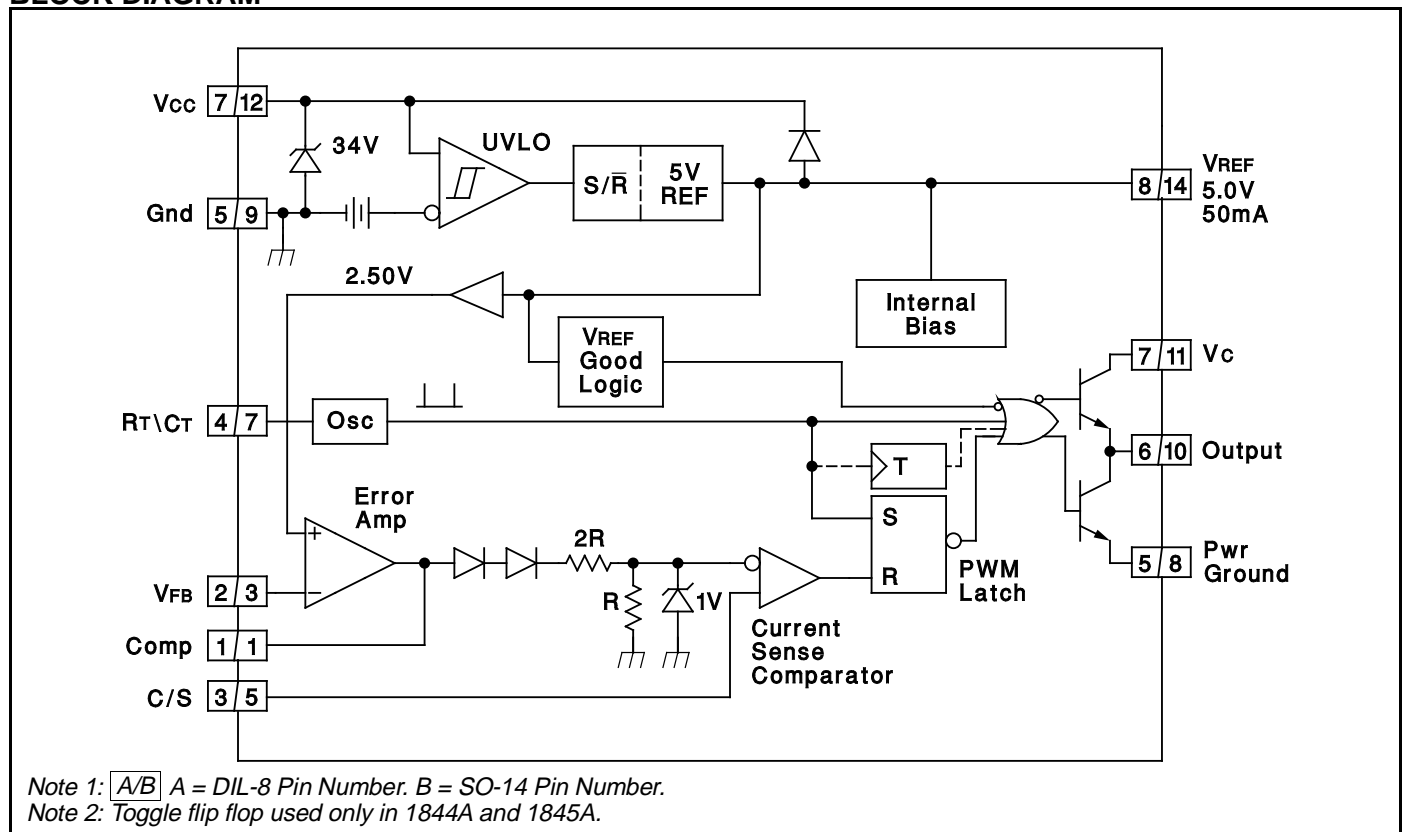
- Low R_O Error Amp

DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for V_{CC} over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

BLOCK DIAGRAM

Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844A and 1845A.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (Icc mA). . . . . Self Limiting
Output Current . . . . ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) . . . . -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at TA ≤ 25°C (DIL-8) 1W
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . 300°C

Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW) J or N, D8 Package

Comp	1	8	VREF
VFB	2	7	Vcc
ISENSE	3	6	Output
RT/CT	4	5	Gnd

SOIC-14 (TOP VIEW) D Package

Comp	1	14	VREF
N/C	2	13	N/C
VFB	3	12	Vcc
N/C	4	11	Vc
ISENSE	5	10	Output
N/C	6	9	Gnd
RT/CT	7	8	Pwr Gnd

PLCC-20, LCC-20 (TOP VIEW) Q, L Packages

PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
VFB	5
N/C	6
ISENSE	7
N/C	8-9
RT/CT	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
Vc	17
Vcc	18
N/C	19
VREF	20
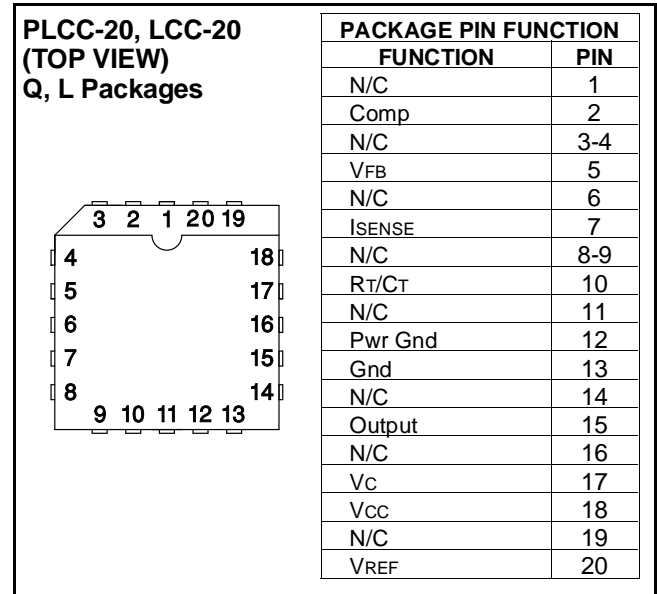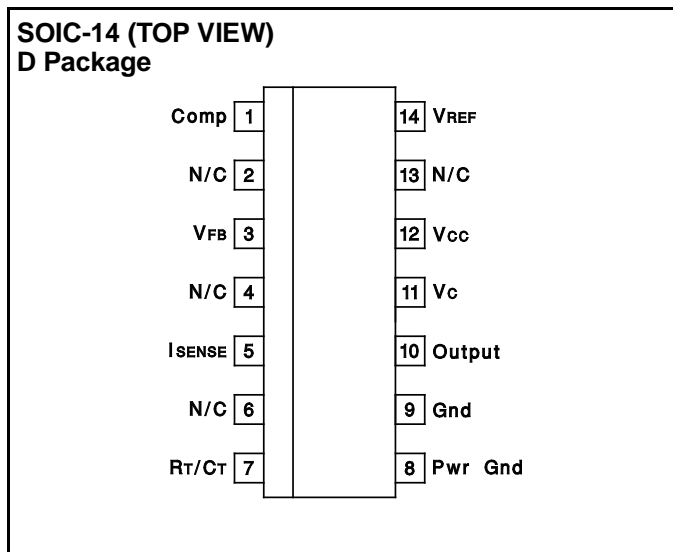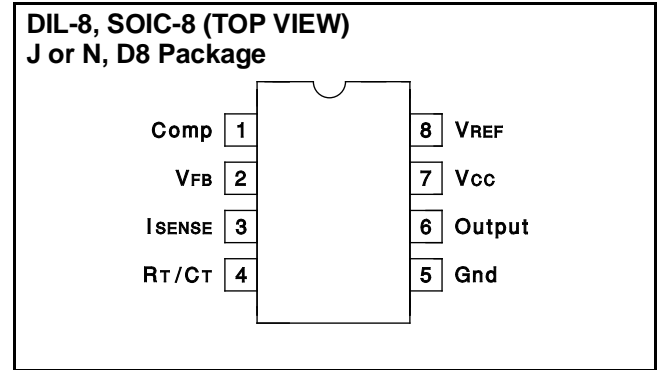
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for -55°C ≤ TA ≤ 125°C for the UC184xA; -40°C ≤ TA ≤ 85°C for the UC284xA; 0 ≤ TA ≤ 70°C for the UC384xA; Vcc = 15V (Note 5); RT = 10k; CT = 3.3nF; TA = TJ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	TJ = 25°C, Io = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ VIN ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ Io ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz TJ = 25°C (Note 2)		50			50		µV
Long Term Stability	TA = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	TJ = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ Vcc ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	TMIN ≤ TA ≤ TMAX (Note 2)		5			5		%
Amplitude	VPIN 4 peak to peak (Note 2)		1.7			1.7		V
Discharge Current	TJ = 25°C, VPIN 4 = 2V (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA
	VPIN 4 = 2V (Note 8)	7.5		8.8	7.6		8.8	mA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for -55°C ≤ TA ≤ 125°C for the UC184xA; -40°C ≤ TA ≤ 85°C for the UC284xA; 0 ≤ TA ≤ 70°C for the UC384xA; VCC = 15V (Note 5); RT = 10k; CT = 3.3nF; TA = TJ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amp Section								
Input Voltage	VPIN 1 = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
AVOL	2 ≤ VO ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	TJ = 25°C (Note 2)	0.7	1		0.7	1		MHz
PSRR	12 ≤ VCC ≤ 25V	60	70		60	70		dB
Output Sink Current	VPIN 2 = 2.7V, VPIN 1 = 1.1V	2	6		2	6		mA
Output Source Current	VPIN 2 = 2.3V, VPIN 1 = 5V	-0.5	-0.8		-0.5	-0.8		mA
VOUT High	VPIN 2 = 2.3V, RL = 15k to ground	5	6		5	6		V
VOUT Low	VPIN 2 = 2.7V, RL = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	VPIN 1 = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ VCC ≤ 25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	VPIN 3 = 0 to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	ISINK = 20mA		0.1	0.4		0.1	0.4	V
	ISINK = 200mA		15	2.2		15	2.2	V
Output High Level	ISOURCE = 20mA	13	13.5		13	13.5		V
	ISOURCE = 200mA	12	13.5		12	13.5		V
Rise Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
Fall Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	VCC = 5V, ISINK = 10mA		0.7	1.2		0.7	1.2	V
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After	x842A/4A	9	10	11	8.5	10	11.5	V
TurnOn	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	VPIN 2 = VPIN 3 = 0V		11	17		11	17	mA
VCC Zener Voltage	ICC = 25mA	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with VPIN2 = 0.

Note 4: Gain defined as: $A = \dfrac{\Delta V_{PIN\,1}}{\Delta V_{PIN\,3}}$; $0 \le V_{PIN\,3} \le 0.8V$.

Note 5: Adjust VCC above the start threshold before setting at 15V.

Note 6: Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.
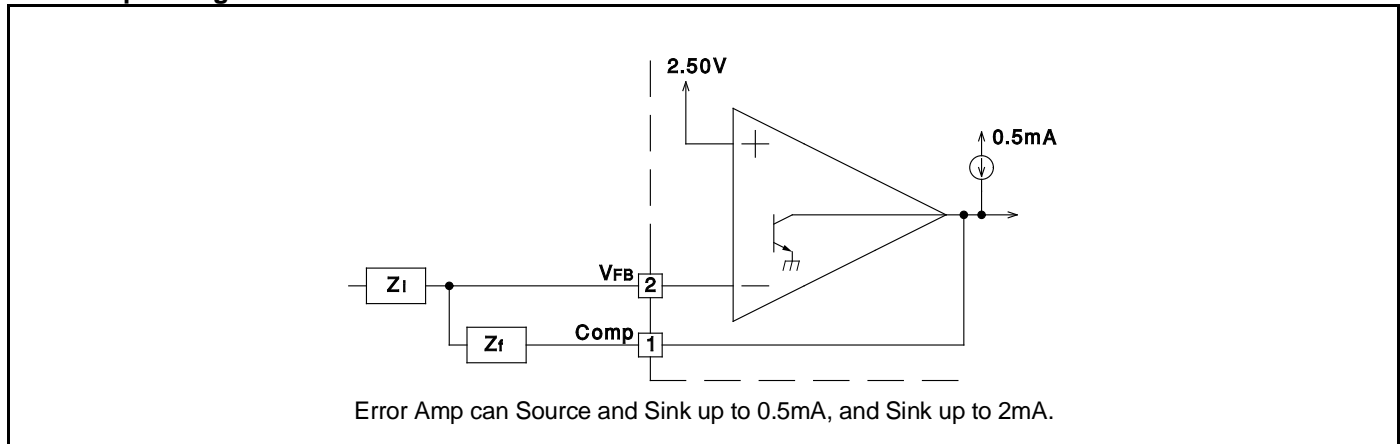
Note 7: "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

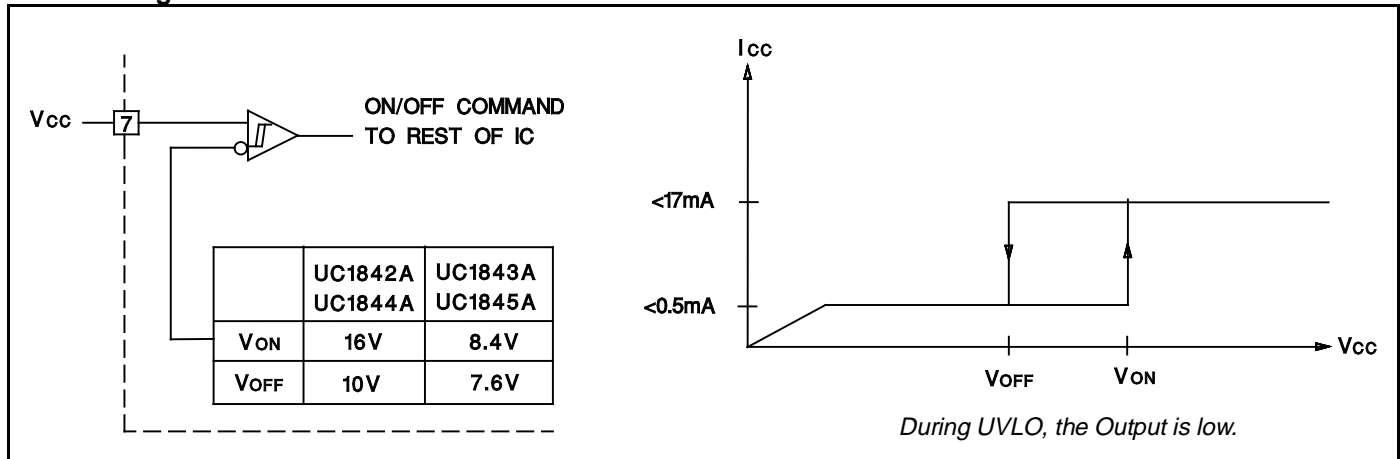$$Temp\ Stability = \frac{V_{REF}\,(max) - V_{REF}\,(min)}{T_J\,(max) - T_J\,(min)}.$$

VREF (max) and VREF (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

Note 8: This parameter is measured with RT = 10kΩ to VREF. This contributes approximately 300µA of current to the measurement. The total current flowing into the RT/CT pin will be approximately 300µA higher than the measured value.
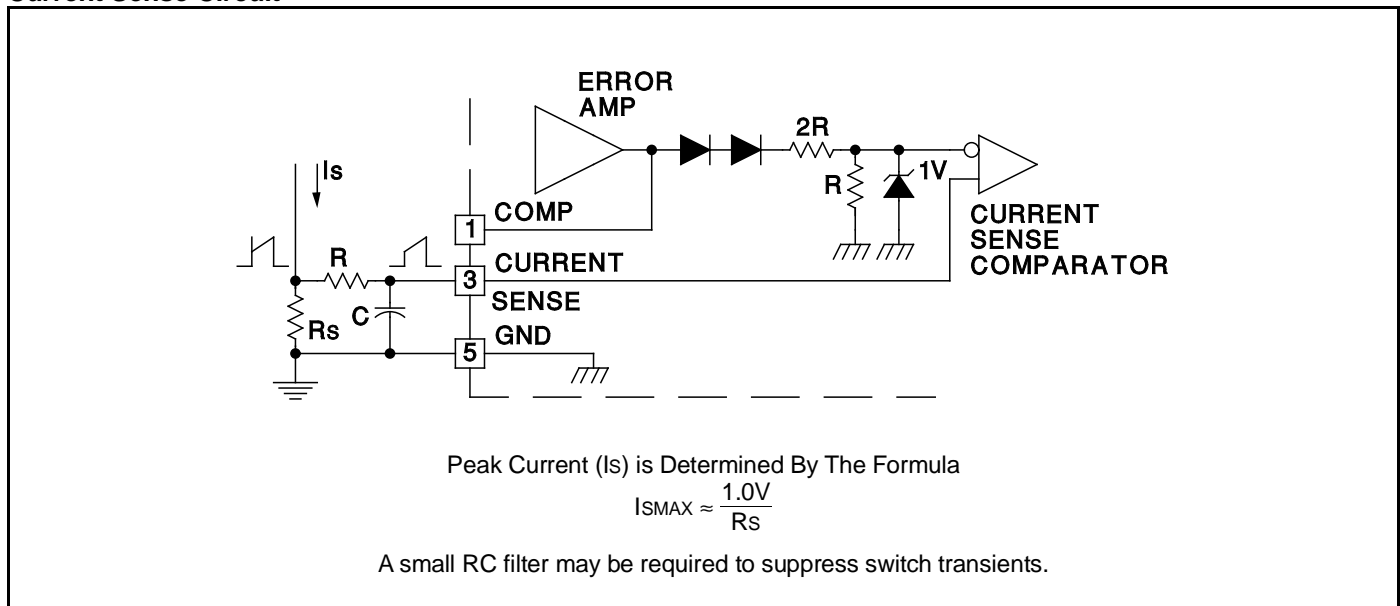
Error Amp Configuration

Error Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Under-Voltage Lockout

	UC1842A UC1844A	UC1843A UC1845A
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V

During UVLO, the Output is low.

Current Sense Circuit

Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{R_S}$$

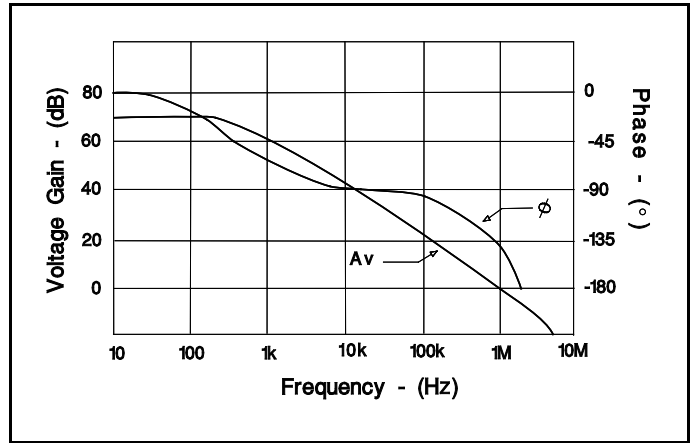A small RC filter may be required to suppress switch transients.

APPLICATIONS DATA (cont.)

Output Saturation Characteristics
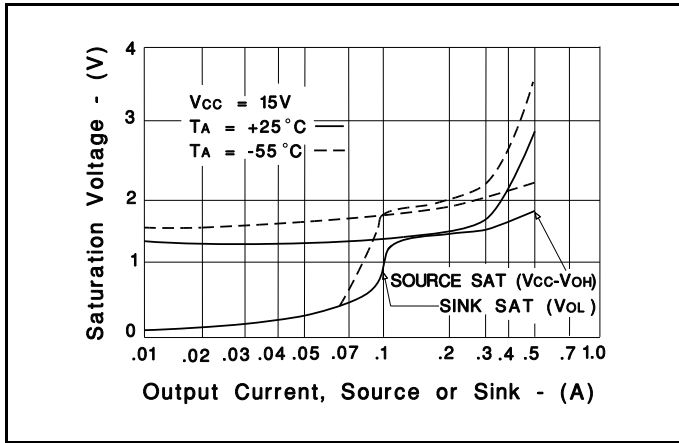
Error Amplifier Open-Loop Frequency Response

Oscillator Section

For $R_T > 5k$ $f \approx \dfrac{1.72}{R_T C_T}$

Oscillator Frequency vs Timing Resistance

Maximum Duty Cycle vs Timing Resistor
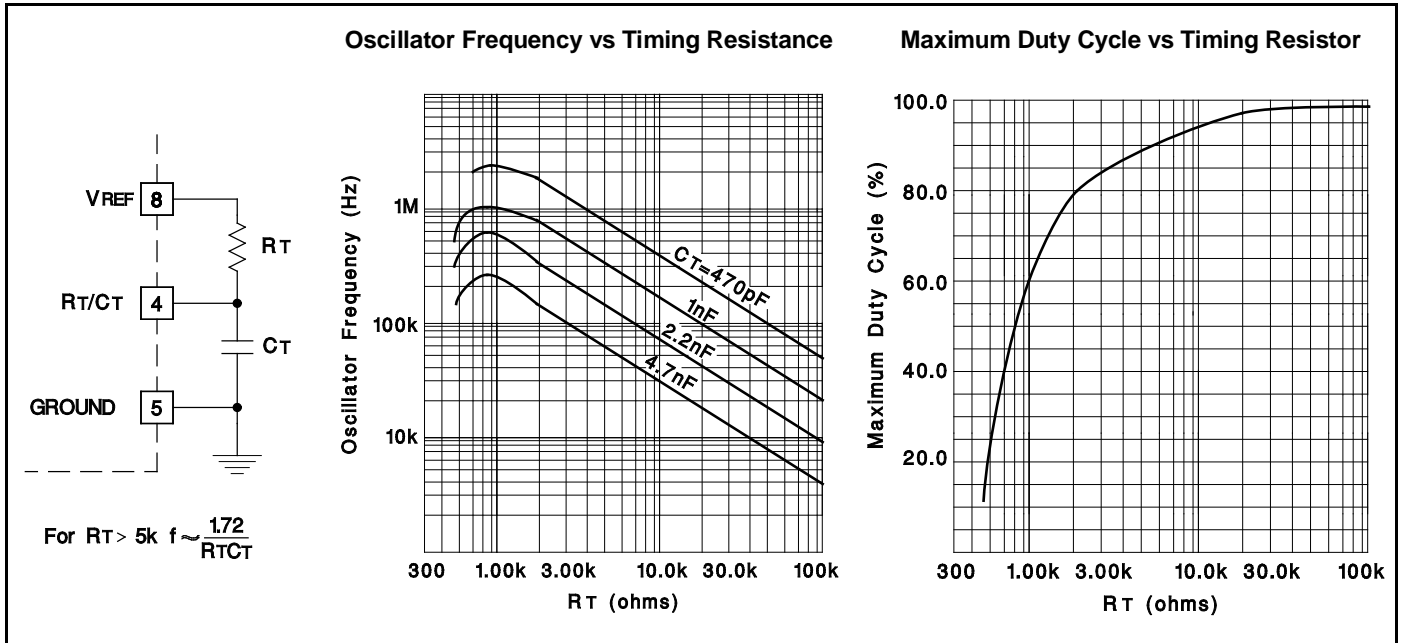
Open-Loop Laboratory Test Fixture

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

5
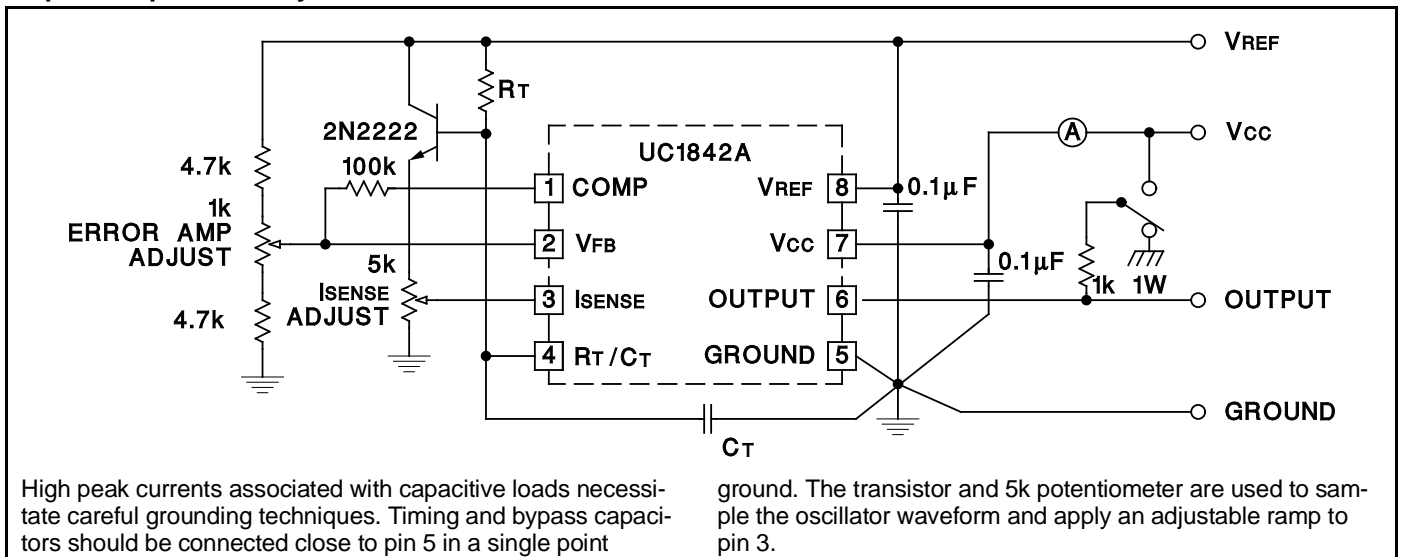
APPLICATIONS DATA (cont.)

Off-line Flyback Regulator

R1
5Ω
1W

117 VAC

VARO
VM 68

C1
250µF
250V

R2
56K
2W

R12
4.7k
2W

C9
3300pF
600V

T1
(NOTE 2)

D6
USD945

L1
(NOTE 2)

D4
1N3613

NP

N5

C10
4700µF
10V

C11
4700µF
10V

+5V

COM

R4
4.7k

R3
20k

D2
1N3612

D3
1N3612

D7
UFS1002

N12

C12
2200µF
16V

+12V

N12

± 12V COM

R5 150k

C14 100 pF

2 7
1
UC1844A
8 6
4 5

C2
100µF
25V

C3
22µF

R9
68Ω
3W

C4
47µF
25V

NC

D8
UES1002

C13
2200µF
16V

-12V

R7
22Ω

Q1
UFN833

C8
680pF
600V

R6
10k

USD1120

1k

R8

C5
.01µF

C6
.0022µF

C7
470pF

R13
20k

R10
0.55Ω
1W

D5
1N3613

R11
2.7k
2W

Power Supply Specifications

1. Input Voltage   95VAC to 130VA (50 Hz/60Hz)
2. Line Isolation   3750V
3. Switching Frequency 40kHz
4. Efficiency @ Full Load 70%

5. Output Voltage:
A. +5V, ±5%; 1A to 4A load
   Ripple voltage: 50mV P-P Max
B. +12V, ±3%; 0.1A to 0.3A load
   Ripple voltage: 100mV P-P Max
C. -12V ,±3%; 0.1A to 0.3A load
   Ripple voltage: 100mV P-P Max

Slope Compensation

V_{REF} 8

0.1µF

R_T

R_T/C_T 4

C_T

UC1842A/3A

R1

R2

I_{SENSE} 3

I_{SENSE}

C

R_{SENSE}

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

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Power Management

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UC3844A, CURRENT MODE PWM CONTROLLER
Device Status: Active

> <u>Description</u>
> <u>Features</u>
> <u>Datasheets</u>
> <u>Pricing/Samples/Availability</u>
> <u>Application Notes</u>
> <u>Applications</u>

Parameter Name	UC3844A
Shutdown	No
Output Type	Single, Totem Pole
Output Current (mA)	+/-1000
Frequency (max) (kHz)	500
Pulse - by - Pulse Isense	Yes
Reference Voltage (V)	5
Vref tol (%)	1
Startup Current (uA)	300
Duty Cycle (max) (%)	50
Operating Supply Current (mA)	11
Operating Supply (max) (V)	30
Operating Supply (min) (V)	10
PWM Outputs (#)	1
Error Amplifier GBW (mHz)	1

Description

**Unitrode Products
from Texas Instruments**

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for V_{CC} over 5V.

The difference between members of this family are shown in the table below.

Features

- Optimized For Off-line and DC To DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low R_O Error Amp

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: slus224.pdf (517 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (ºC)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
UC3844AD	D	14	0 TO 70	ACTIVE	1.09	1	Check stock or order
UC3844AD8	D	8	0 TO 70	ACTIVE	1.04	1	Check stock or order
UC3844AD8TR	D	8	0 TO 70	ACTIVE	0.97	1	Check stock or order
UC3844ADTR	D	14	0 TO 70	ACTIVE	1.02	1	Check stock or order
UC3844AN	P	8	0 TO 70	ACTIVE	0.99	1	Check stock or order

Application Reports

- DN-26 UC3842A LOW-COST START-UP AND FAULT PROTECTION CIRCUIT (SLUA162 - Updated: 11/04/1999)
- DN-27 UC1842/UC1842A FAMILY - SUMMARY OF FUNCTIONAL DIFFERENCES (SLUA163 - Updated: 11/04/1999)
- DN-29 UC3842A FAMILY - FREQUENCY FOLDBACK TECHNIQUE PROVIDES PROTECTION (SLUA165 - Updated: 11/04/1999)
- DN-30 PROGRAMMABLE ELECTRONIC CIRCUIT BREAKER (SLUA166 - Updated: 11/04/1999)
- DN-40 THE EFFECTS OF OSCILLATOR DISCHARGE CURRENT VARIATIONS ON MAXIMUM DUTY (SLUA173 - Updated: 11/04/1999)
- ELECTROSTATIC DISCHARGE APPLICATION NOTE (SSYA008 - Updated: 05/05/1999)
- THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS (SZZA017A - Updated: 09/10/1999)

Table Data Updated on: 8/15/2000

Table Data Updated on: 8/15/2000

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