- **Organization**
  TM124BBK32 . . . 1 048 576 × 32
  TM248CBK32 . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10 % Tolerance)**
- **72-pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124BBK32-Utilizes Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248CBK32-Utilizes Sixteen 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Distributed Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, In Four Blocks**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
TM124BBK32-60	60 ns	15 ns	110 ns
TM124BBK32-70	70 ns	18 ns	130 ns
TM124BBK32-80	80 ns	20 ns	150 ns
TM248CBK32-60	60 ns	15 ns	110 ns
TM248CBK32-70	70 ns	18 ns	130 ns
TM248CBK32-80	80 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  – TM124BBK32
  – TM248CBK32
- **Tin-Lead (Solder) Tabbed Versions Available:**
  – TM124BBK32S
  – TM248CBK32S

description

TM124BBK32

The TM124BBK32 is a dynamic random-access memory (DRAM) organized as four times 1048576 × 8 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400, 1048576 × 4-bit DRAMs, each in 20/26-lead plastic SOJ packages, mounted on a substrate together with decoupling capacitors. Each TMS44400 is described in the TMS44400 data sheet.

The TM124BBK32 is available in the single-sided BK leadless module for use with sockets.

The TM124BBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns and 80 ns. This device is rated for operation from 0°C to 70°C

TM248CBK32

The TM248CBK32 is a dynamic random-access memory organized as four times 2097152 × 8 in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS44400, 1048576 × 4-bit dynamic RAMs, each in 20/26-lead plastic SOJ packages SOJs, mounted on a substrate together with decoupling capacitors. Each TMS44400 is described in the TMS44400 data sheet.

The TM248CBK32 is available in the double-sided BK leadless module for use with sockets.

The TM248CBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns and 80 ns. This device is rated for operation from 0°C to 70°C

operation

TM124BBK32

The TM124BBK32 operates as eight TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM124BBK32 dictates the use of early write cycles to prevent contention on D and Q.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM248CBK32

The TM248CBK32 operates as sixteen TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM248CBK32 dictates the use of early write cycles to prevent contention on D and Q.

refresh

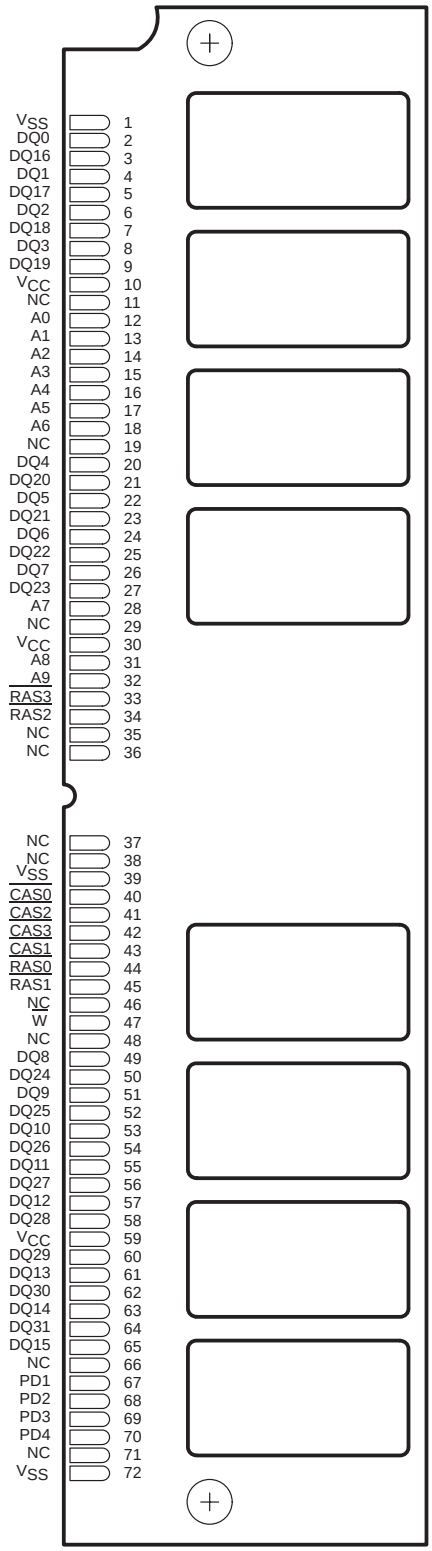
Refresh period is extended to 16 ms and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. A0-A9 address lines must be refreshed every 16 ms as required by the TMS44400 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124BBK32 AND TM248CBK32: Nickel plate and gold plate over copper.
Contact area for TM124BBK32S AND TM248CBK32S: Nickel plate and tin-lead over copper.

BK SINGLE IN-LINE MEMORY MODULE

(TOP VIEW)



TM124BBK32†

(SIDE VIEW)

TM248CBK32†

(SIDE VIEW)

PIN NOMENCLATURE

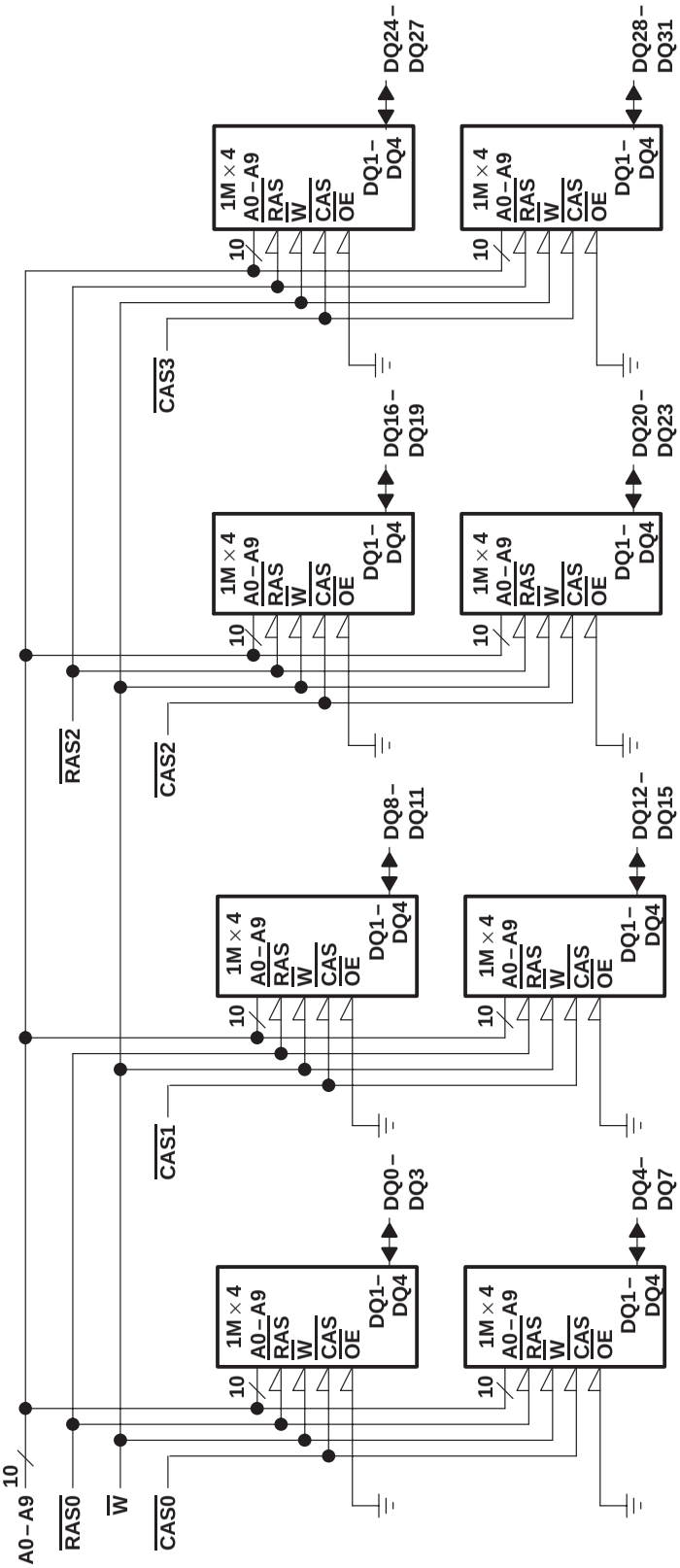
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT

SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124BBK32	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248CBK32	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are not drawn to scale.

functional block diagram (for TM124BBK32 and TM248CBK32, Side 1)



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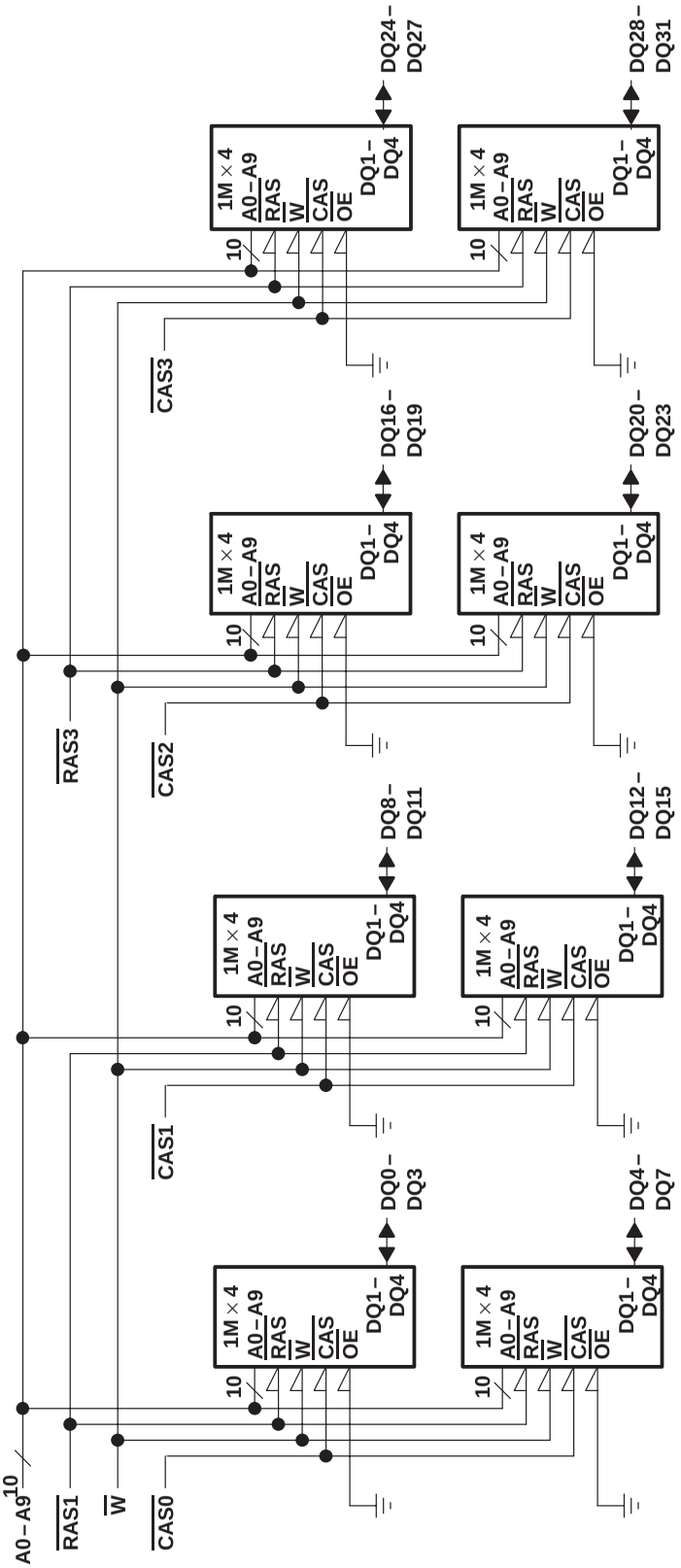
functional block diagram (for TM248CBK32, Side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 8 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124BBK32-60		'124BBK32-70		'124BBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		840		720		640	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8	
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	$\overline{V_{CC}}$ = 5.5 V, $t_{\overline{PC}}$ = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248CBK32-60		'248CBK32-70		'248CBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		±20		±20		±20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±20		±20		±20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		856		736		656	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		32		32		32	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		16		16		16	
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1680		1440		1280	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		736		656		576	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature f = 1 MHz (see Note 5)

		'124BBK32		'248CBK32		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		40		80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		28		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		14		28	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		56		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended range of supply voltage and operating free-air temperature

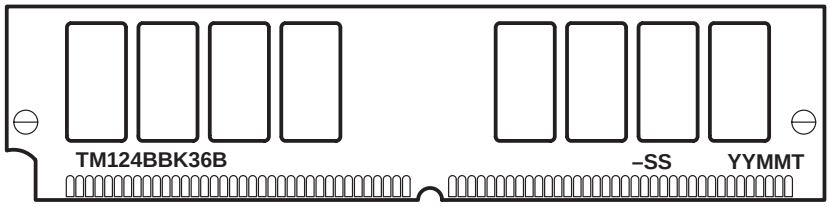
		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low	50		55		60		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 11)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PL}min, t_{ASC} should be ≥ 5 ns.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. Maximum value specified only to assure access time.

timing requirements over recommended range of supply voltage and operating free-air temperature (concluded)

		’124BBK32-60 ’248CBK32-60		’124BBK32-70 ’248CBK32-70		’124BBK32-80 ’248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

device symbolization (TM124BBK32 illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

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