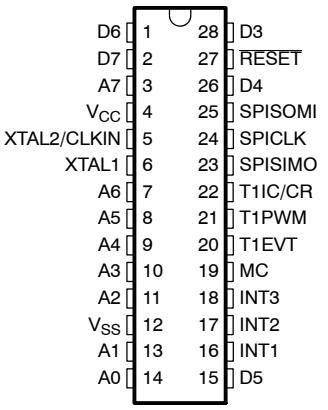
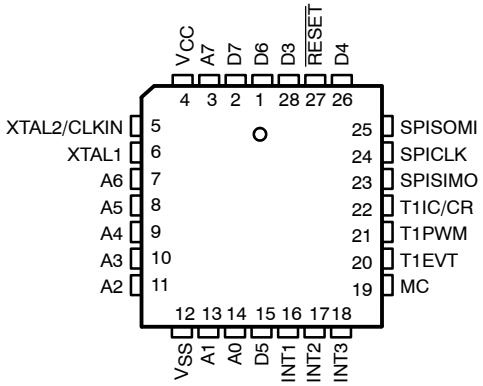
SPNS012F – MAY 1987 – REVISED FEBRUARY 1997

- CMOS/EEPROM/EPROM Technologies on a Single Device
  - Mask-ROM Devices for High-Volume Production
  - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
  - Reprogrammable-EPROM Devices for Prototyping Purposes
- Internal System Memory Configurations
  - On-Chip Program Memory Versions
    - ROM: 2K, 4K, or 8K Bytes
    - EPROM: 8K Bytes
  - Data EEPROM: 256 Bytes
  - Static RAM: 128 or 256 Bytes Usable as Registers
- Flexible Operating Features
  - Low-Power Modes: STANDBY and HALT
  - Commercial, Industrial, and Automotive Temperature Ranges
  - Clock Options
    - Divide-by-1 (2 MHz–5 MHz SYSCLK) Phase-Locked Loop (PLL)
    - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
  - Supply Voltage (V_{CC}) 5 V ±10%
- 16-Bit General Purpose Timer
  - Software Configurable as a 16-Bit Event Counter, or a 16-Bit Pulse Accumulator, or a 16-Bit Input Capture Functions, or Two Compare Registers, or a Self-Contained PWM Function
  - Software Programmable Input Polarity
  - 8-Bit Prescaler, Providing a 24-Bit Real-Time Timer
- On-Chip 24-Bit Watchdog Timer
  - EPROM/OTP Devices:
    - EPROM ’712A Standard Watchdog
    - EPROM ’712B Hard Watchdog
  - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- Flexible Interrupt Handling
  - Two Software Programmable Interrupt Levels
  - Global-and Individual-Interrupt Masking
  - Programmable Rising- or Falling-Edge Detect
  - Individual Interrupt Vectors
- Serial Peripheral Interface (SPI)
  - Variable-Length High-Speed Shift Register
  - Synchronous Master/Slave Operation
- TMS370 Series Compatibility
  - Register-to-Register Architecture
  - 128 or 256 General-Purpose Registers
  - 14 Powerful Addressing Modes
  - Instructions Upwardly Compatible With All TMS370 Devices
- CMOS/TTL Compatible I/O Pins/Packages
  - All Peripheral Function Pins Software Configurable for Digital I/O
  - 21 Bidirectional Pins, 1 Input Pin
  - 28-Pin Plastic and Ceramic DIP, or Leaded Chip Carrier (LCC) Packages
- Workstation/PC-Based Development System
  - C Compiler and C Source Debugger
  - Real-Time In-Circuit Emulation
  - Extensive Breakpoint/Trace Capability
  - Multi-Window User Interface
  - Microcontroller Programmer

JD AND N PACKAGES
(TOP VIEW)



FZ AND FN PACKAGES
(TOP VIEW)



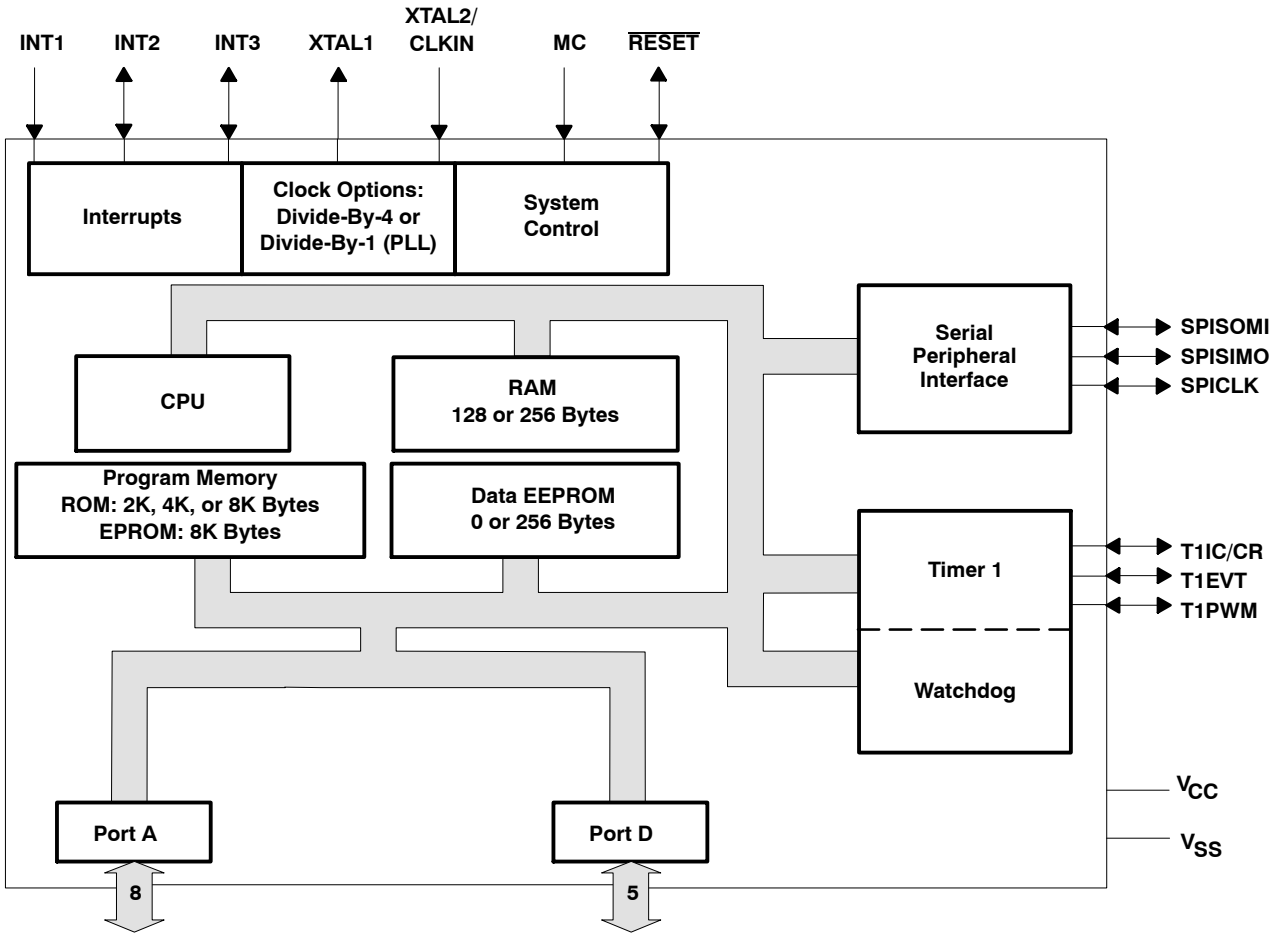
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Pin Descriptions

28 PINS DIP and LCC		I/O†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	14 13 11 10 9 8 7 3	I/O	Port A is a general-purpose bidirectional I/O port.
D3 D4 D5 D6 D7	28 26 15 1 2	I/O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
INT1 INT2 INT3	16 17 18	I I/O I/O	External interrupt (non-maskable or maskable)/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	22 21 20	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 PWM output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
SPISOMI SPISIMO SPICLK	25 23 24	I/O	SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin
$\overline{\text{RESET}}$	27	I/O	System reset bidirectional pin; as input pin, $\overline{\text{RESET}}$ initializes the microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates that an internal failure was detected by watchdog or oscillator fault circuit.
MC	19	I	Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V_{PP}
XTAL2/CLKIN XTAL1	5 6	I O	Internal oscillator crystal input/External clock source input Internal oscillator output for crystal
V_{CC}	4		Positive supply voltage
V_{SS}	12		Ground reference

† I = input, O = output

functional block diagram



description

The TMS370C010, TMS370C012, TMS370C311, TMS370C310, TMS370C312, TMS370C712, and SE370C712 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx1x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral-function modules and various on-chip memory configurations.

The TMS370Cx1x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx1x devices attractive for system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx1x devices contain the following on-chip peripheral modules:

- Serial peripheral interface (SPI)
- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx1x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		28 PIN PACKAGES
	ROM	EPROM	RAM	EEPROM	
TMS370C010A	4K	—	128	256	FN – PLCC N – PDIP
TMS370C012A	8K	—	256	256	FN – PLCC N – PDIP
TMS370C311A	2K	—	128	–	FN – PLCC N – PDIP
TMS370C310A	4K	—	128	–	FN – PLCC N – PDIP
TMS370C312A	8K	—	128	–	FN – PLCC N – PDIP
TMS370C712A, TMS370C712B	—	8K	256	256	FN – PLCC N –PDIP
SE370C712A†, SE370C712B†	—	8K	256	256	FZ – CLCC JD – CDIP

† System evaluators and development are for use only in prototype environment and their reliability has not been characterized.

The suffix letter (A or B) appended to the device names shown in the device column of Tables 1 and 2 indicates the configuration of the device. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE‡	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
EPROM B	Hard	Divide-by-1 (PLL)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

‡ Refer to the “device numbering conventions” section for device nomenclature and to the “device part numbers” section for ordering.

The 2K bytes, 4K bytes, and 8K bytes of mask-programmable ROM in the associated TMS370Cx1x devices are replaced in the TMS370C712 with 8K bytes of EPROM. All other available memory and on-chip peripherals are identical, with the exception of no data EEPROM on the TMS370C311, TMS370C310, and TMS370C312 devices. The OTP (TMS370C712) device and reprogrammable (SE370C712) device are available.

TMS370C712 OTP devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx1x family or for low volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C712 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C712 devices allow quick updates to breadboards and prototype systems while iterating initial designs.

description (continued)

The TMS370Cx1x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx1x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx1x family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

The SPI provides a convenient method of serial interaction for high-speed communications between simpler shift register-type devices, such as display drivers, analog-to-digital (A/D) converters, PLL, input/output (I/O) expansion, or other microcontrollers in the system.

The TMS370Cx1x family provides the system designer with economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx1x into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family XDS development tool communicates through a standard RS-232-C interface with an existing personal computer. This allows the use of the PC's editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive menus and screen windowing so that a system designer can begin developing software with minimal training. Precise real-time, in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reducing the time-to-market cycle.

The TMS370Cx1x family together with the TMS370 family XDS22, CDT370, design kit, starter kit, software tools, the SE370C712 reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU on the TMS370Cx1x device is the high-performance 8-bit TMS370 CPU module. The 'x1x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x1x instruction map is shown in Table 17 in the TMS370Cx1x instruction set overview section.

The '370Cx1x CPU architecture provides the following components:

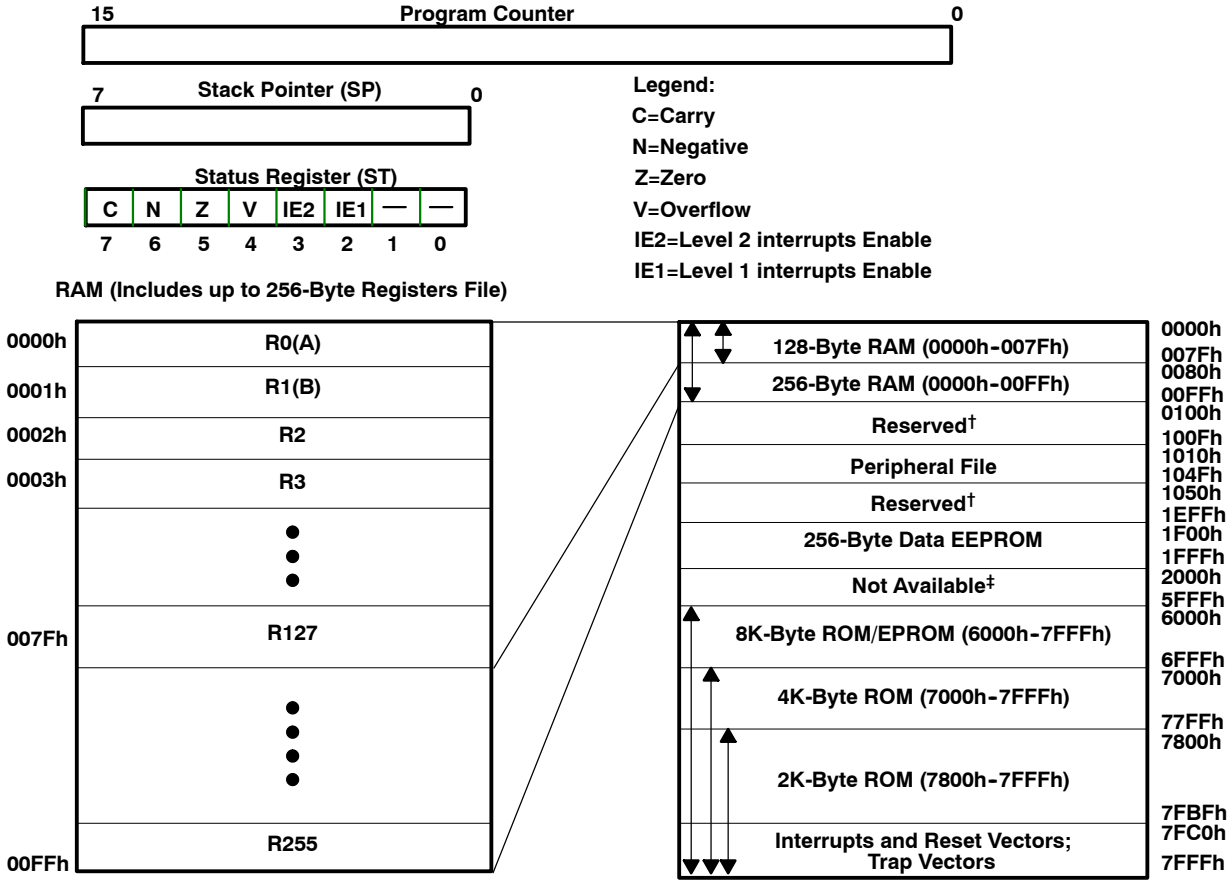
CPU registers:

- A stack pointer that points to the last entry in the memory stack
- A status register that monitors the operation of the instructions and contains the global interrupt-enable bits
- A program counter (PC) that points to the memory location of the next instruction to be executed

XDS and CDT are trademarks of Texas Instruments Incorporated.

central processing unit (CPU) (continued)

Figure 1 illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.
‡ Not available means the address space is not accessible.

Figure 1. Programmer's Model

A memory map includes:

- 128- or 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, or the stack
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
- 256-byte EEPROM module, that provides in-circuit programmability and data retention in power-off conditions
- 2K-, 4K-, or 8K-byte ROM or 8K-byte EPROM

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the status register (ST) contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

central processing unit (CPU) (continued)

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contains the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of the reset vector.

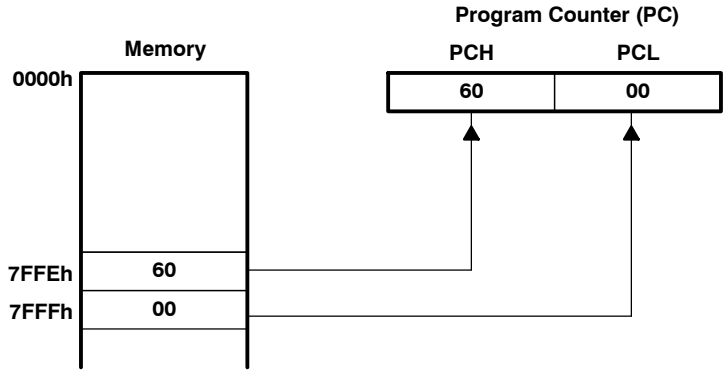


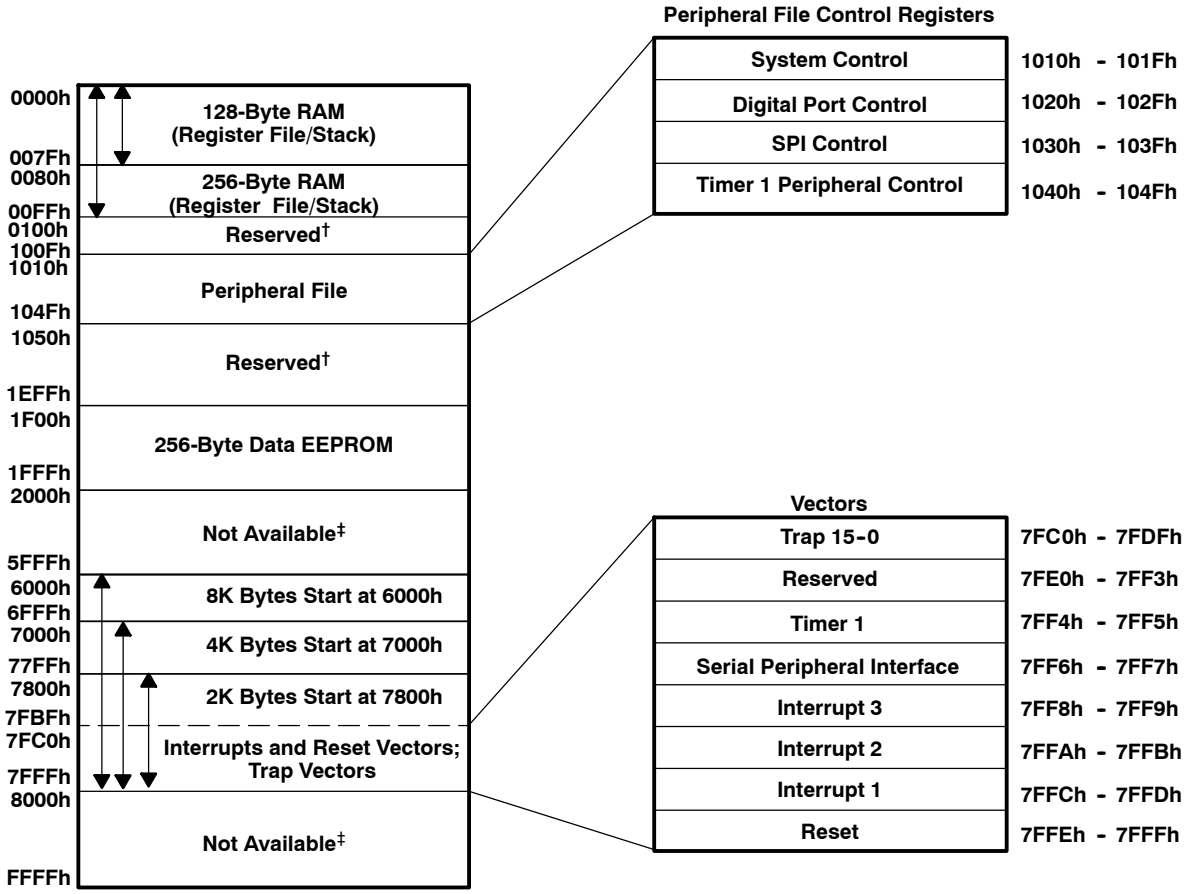
Figure 2. Program Counter After Reset

memory map

The TMS370Cx1x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx1x provides memory-mapped RAM, ROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1010h to 104Fh and is divided logically into four peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

TMS370Cx1x CPU (continued)



† Reserved means that the address space is reserved for future expansion.
‡ Not available means that the address space is not accessible.

Figure 3. TMS370Cx1x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx10, TMS370Cx11, and TMS370C312 contain 128 bytes of internal RAM mapped beginning at location 0000h (R0) and continuing through location 007Fh (R127) which is shown in Table 4 along with ’712 devices.

Table 4. RAM Memory Map

	’x10, ’x11 AND ’312	’712
RAM size	128 bytes	256 bytes
Memory mapped	0000h–007Fh	0000h–00FFh

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx1x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 5 shows the TMS370Cx1x PF address map.

Table 5. TMS370Cx1x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved
1010h–101Fh	P010–P01F	System and EPROM/EEPROM control registers
1020h–102Fh	P020–P02F	Digital I/O port control registers
1030h–103Fh	P030–P03F	SPI registers
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–10FFh	P050–P0FF	Reserved

data EEPROM

The TMS370Cx1x devices, containing 256 bytes of data EEPROM, have memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
  - Bit-, byte-, and block-write/erase modes
  - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
  - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 6.
  - In-circuit programming capability. There is no need to remove the device to program.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
  - Reset. All programming of the data EEPROM module is halted.
  - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
  - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 6. Data EEPROM and PROGRAM EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM Control Register
P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

program EPROM†

The TMS370C712 device contains 8K bytes of EPROM mapped, beginning at location 6000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
  - In-circuit programming capability if V_{PP} is applied to MC
  - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01Ch as shown in Table 6.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
  - Reset: All programming to the EPROM module is halted
  - Low-power modes
  - 13 V not applied to MC

program ROM†

The program ROM consists of 2K to 8K bytes of mask programmable read-only memory (see Table 7). The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication.

Table 7. Program ROM Memory Map

	'x11	'x10	'x12
ROM size	2K bytes	4K bytes	8K bytes
Memory mapped	7800h–7FFFh	7000h–7FFFh	6000h–7FFFh

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx1x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout . See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x1x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

† Memory addresses 7FF8h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh.

system reset (continued)

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4), the cold-start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 8 depicts the reset sources.

Table 8. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Register A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 4. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the ST.

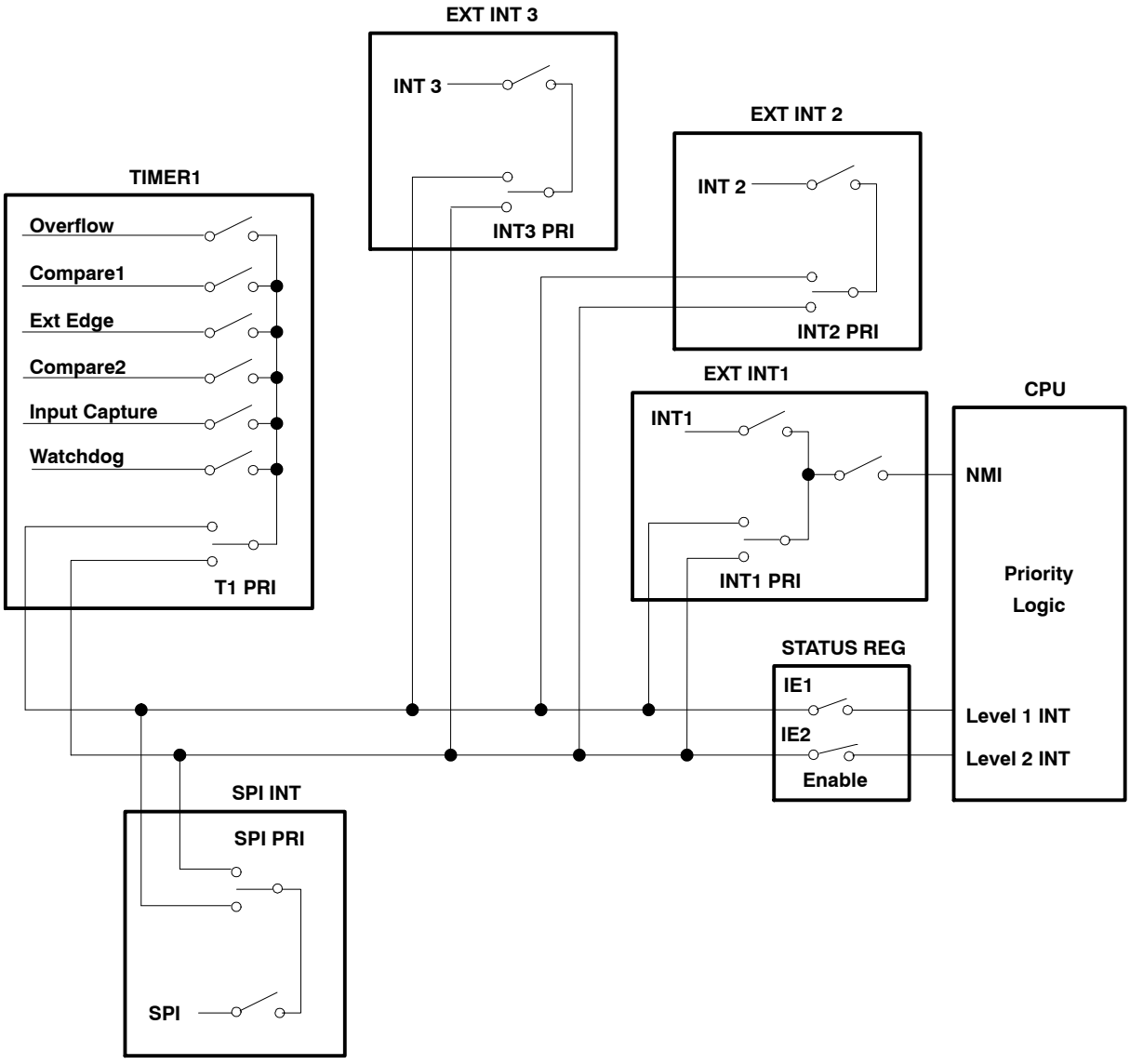


Figure 4. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority-interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending-interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx1x has five hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 9. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or to determine which interrupt source generated the associated system interrupt.

Two of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

Table 9. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External $\overline{\text{RESET}}$ Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}$‡	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3‡	7FF8h, 7FF9h	4
SPI Receiver (Rx)/Transmitter (Tx) Data Complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture 1 Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT§	7FF4h, 7FF5h	6

† Relative priority within an interrupt level
‡ Release microcontroller from STANDBY and HALT low-power modes
§ Release microcontroller from STANDBY low-power mode

privileged operation and EEPROM write protection override

The TMS370Cx1x family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx1x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is

privileged operation and EEPROM write protection override (continued)

set to 1 to enter the nonprivileged mode, disabling write operations to specific configuration-control bits within the PF. Table 10 displays the system-configuration bits which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 10. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.6	OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST

† The privilege bits are shown in a bold typeface in the peripheral file frame 1 section.

The write protect override (WPO) mode provides an external hardware method of overriding the write protection registers (WPRs) of data EEPROM on the TMS370Cx1x. WPO mode is entered by applying a 12-V input to the MC pin after the $\overline{\text{RESET}}$ pin input goes high (logic 1). The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or Program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of data EEPROM while the device remains in the application but only while requiring a 12 V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx1x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and Timer 1 remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on INT1, INT2, INT3, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx1x is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on the INT1, INT2, or INT3) is detected. The power-down mode-selection bits are summarized in Table 11.

low-power and IDLE modes (continued)

Table 11. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X †	IDLE

† Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x1x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 MCU. The 'x1x masked ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '712A EPROM has only the divide-by-4, while the '712B has divide-by-1.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option}: \quad \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option}: \quad \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 12 contains system-configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded areas.

Table 12. Peripheral File Frame 1: System-Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	**AUTO WAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	V_{PPS}	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 13 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 14 shows the port configuration register setup.

Table 13. Peripheral File Frame 2: Digital Port-Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0)†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

† D3 as SYSCLK, set port D control register 2 = 08h.

Table 14. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
D	3 – 7	Data Out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

programmable timer 1

The programmable Timer 1 (T1) module of the TMS370Cx1x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The Timer 1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent), or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 5.

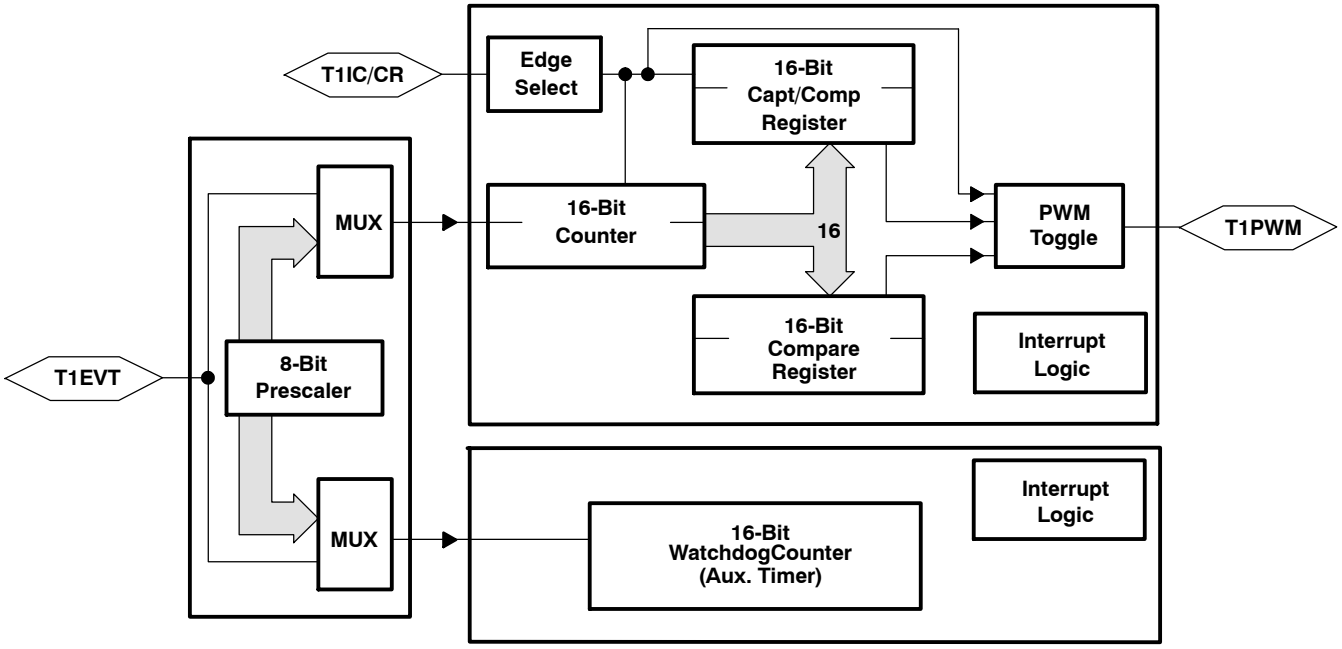


Figure 5. Timer 1 Block Diagram

- Three T1 I/O pins
  - T1IC/CR: T1 input capture / counter-reset input pin, or general-purpose bidirectional I/O pin
  - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
  - Dual-compare mode: Provides PWM signal
  - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare registers.
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if WD feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

programmable timer 1 (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
  - A capture
  - A compare equal
  - A counter overflow
  - An external edge detection
- Sixteen T1 module control registers located in the PF frame beginning at address P040

The T1 module control registers are illustrated in Table 15.

programmable timer 1 (continued)

Table 15. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Capture/Compare								
P040	Bit 15			T1Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 7			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Dual-Compare and Capture/Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

programmable timer 1 (continued)

Figure 6 shows the Timer 1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the PF. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

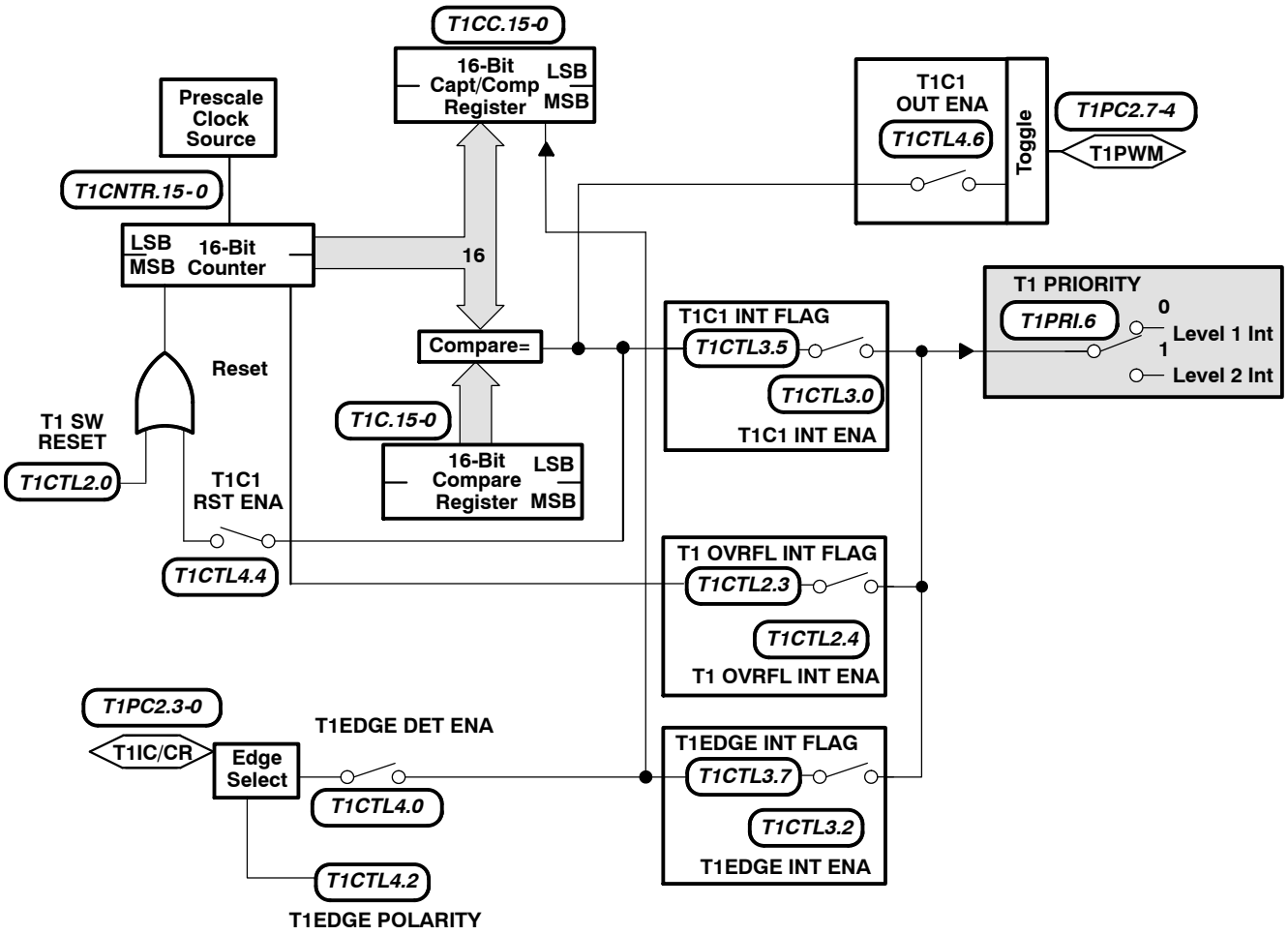


Figure 6. Capture/Compare Mode

programmable timer 1 (continued)

Figure 7 shows the Timer 1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

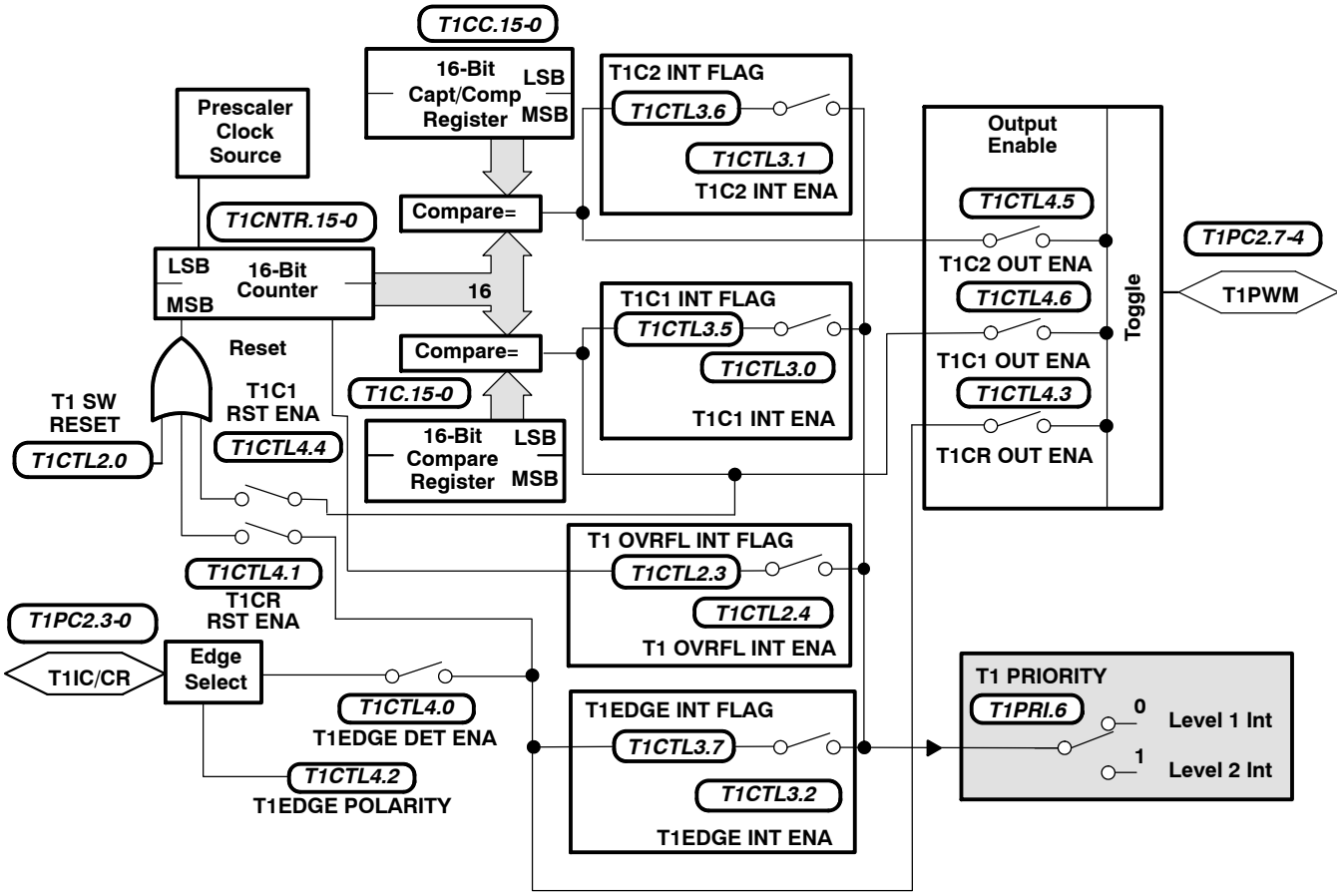


Figure 7. Dual-Compare Mode

programmable timer 1 (continued)

The TMS370Cx1x device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of three mask options as follows: standard watchdog, hard WD, or simple counter.

- Standard watchdog configuration (see Figure 8) for ’C712A EPROM and mask-ROM devices:
  - Watchdog mode
    - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCLK
    - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
    - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
    - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
  - Non-watchdog mode
    - Watchdog timer can be configured as an event counter, pulse accumulator or an interval timer

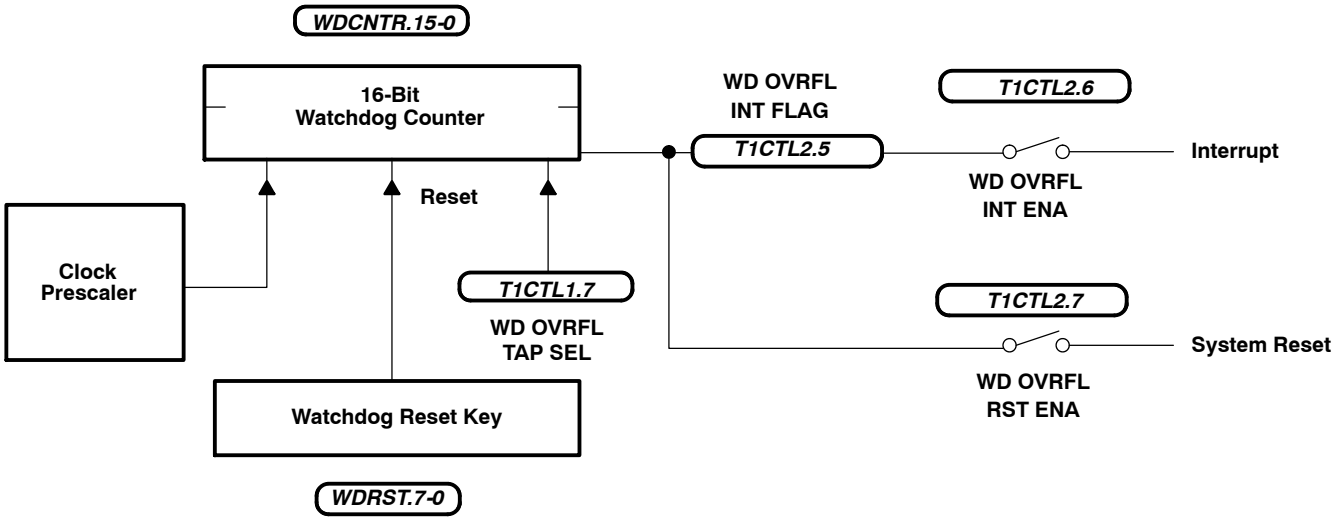


Figure 8. Standard Watchdog

programmable timer 1 (continued)

- Hard watchdog configuration (see Figure 9) for ’C712B EPROM and mask-ROM devices:
  - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
  - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
  - Generates a system reset if an incorrect value is written to the WDRST or if the counter overflows
  - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
  - Automatic activation of the WD timer upon power-up reset
  - INT1 is enabled as a nonmaskable interrupt during low power modes.

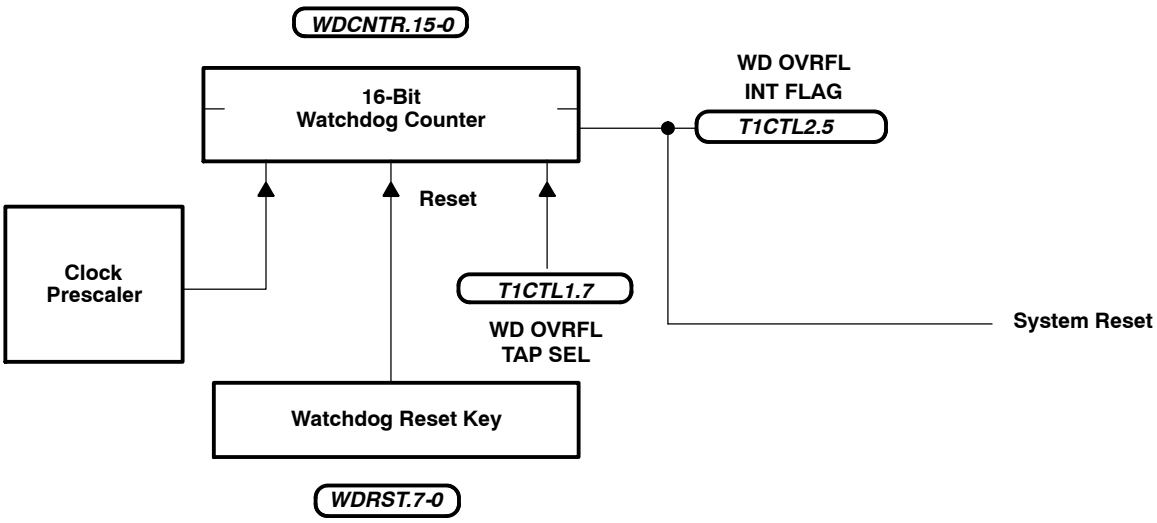


Figure 9. Hard Watchdog

programmable timer 1 (continued)

- Simple counter configuration (see Figure 10) for mask-ROM devices only
  - Simple counter can be configured as an event counter, pulse accumulator, or an internal timer.

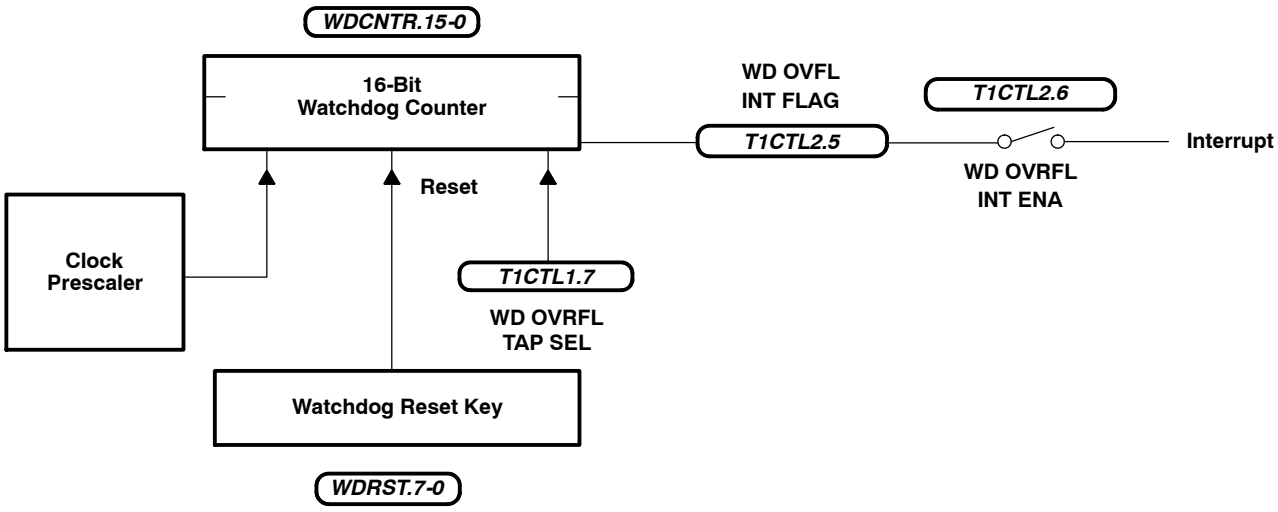


Figure 10. Simple Counter

serial peripheral interface

The SPI is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight bits) to be shifted into and out of the device at a programmable bit transfer rate. The SPI normally is used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion by way of devices such as shift registers, display drivers, and A/D converters. Multi-device communications are supported by the master/slave operation of the SPI. The SPI module features include the following:

- Three external pins
  - SPISOMI: SPI slave output/master input pin or general-purpose bidirectional I/O pin
  - SPISIMO: SPI slave input/master output pin or general-purpose bidirectional I/O pin
  - SPICLK: SPI serial clock pin or general-purpose bidirectional I/O pin
- Two operational modes: Master and slave
- Baud rate: Eight different programmable rates
  - Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^{b}}$$

    where b=bit rate in SPICCR.5-3 (range 0–7)
  - Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK

    for maximum slave SPI BAUD RATE < SYSCLK/8
- Data word format: one to eight data bits
- Simultaneous receiver and transmitter operations (transmit function can be disabled in software)

serial peripheral interface (continued)

- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

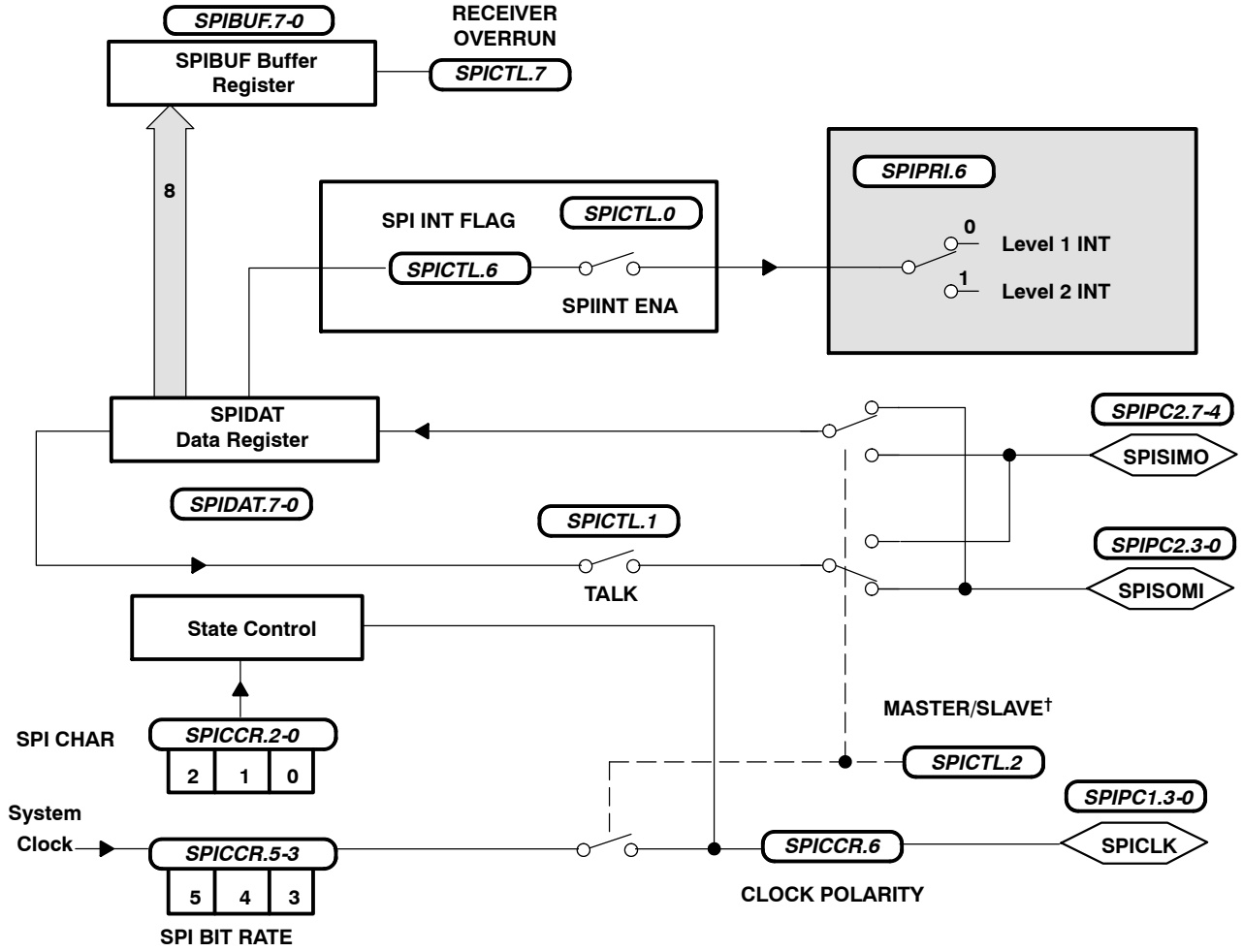
The SPI module-control registers are illustrated in Table 16.

Table 16. SPI Module-Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	**SPI STEST**	**SPI PRIORITY**	**SPI ESPEN**	—	—	—	—	—	SPIPRI

serial peripheral interface (continued)

The SPI block diagram is illustrated in Figure 11.



† The diagram is shown in the slave mode.

Figure 11. SPI Block Diagram

instruction set overview

Table 17 provides an opcode to instruction cross reference of all 73 instructions and 274 opcodes of the ‘370Cx1x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble (LBN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 17. TMS370 Family Opcode/Instruction Map†

LSN \ MSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP ra 2/7							INCW #n,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV *n[SP],A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rn 2/6	TRAP 13 1/14	MOV A,*n[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rn 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rn 2/6	TRAP 11 1/14	extend inst,2 opcodes
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rs 2/7	TRAP 7 1/14	SETC 1/7
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rd 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rs,A 2/9	MOV *lab[B],A 3/12	DJNZ A,ra 2/10	DJNZ B,ra 2/10	DJNZ Rn,ra 3/8	TRAP 5 1/14	RTI 1/12
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rd 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rn 2/6	TRAP 4 1/14	PUSH ST 1/8

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Table 17. TMS370 Family Opcode/Instruction Map †(Continued)

LSN \ MSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rd 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rn 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rs,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rn 2/6	TRAP 2 1/14	LDSP 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rd 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rn 2/6	TRAP 1 1/14	STSP 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rd 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rn 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn.A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

*	=	Indirect addressing operand prefix
&	=	Direct addressing operand prefix
#	=	immediate operand
#16	=	immediate 16-bit number
lab	=	16-label
n	=	immediate 8-bit number
Pd	=	Peripheral register containing destination type
Pn	=	Peripheral register
Ps	=	Peripheral register containing source byte
ra	=	Relative address
Rd	=	Register containing destination type
Rn	=	Register file
Rp	=	Register pair
Rpd	=	Destination register pair
Rps	=	Source Register pair
Rs	=	Register containing source byte

† All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C-compiler, a linker, an in-circuit emulator XDS/22, CDT and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
  - Includes extensive macro capability
  - Provides high-speed operation
  - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
  - Generate assembly code for the TMS370 that can be inspected easily
  - Improves code execution speed and reduces code size with optional optimizer pass
  - Enables direct reference the TMS370's port registers by using a naming convention
  - Provides flexibility in specifying the storage for data objects
  - Interfaces C functions and assembly functions easily
  - Includes assembler and linker
- CDT370 (Compact Development Tool) real-time in-circuit emulation
  - Base (Part Number EDSCDT370 – for PC, requires cable)
    - Cable for 28-pin DIP (Part No. EDSTRG28DIL)
    - Cable for 28-pin PLCC (Part No. EDSTRG28PLCC)
  - EEPROM and EPROM programming support
  - Allows inspection and modification of memory locations
  - Includes compatibility to upload/download program and data memory
  - Execute programs and software routines
  - Includes 1024 samples trace buffer
  - Includes single-step executable instructions
  - Uses software breakpoints to halt program execution at selected address
- XDS/22 in-circuit emulator
  - Base (Part Number TMDS3762210 for PC, requires cable)
    - Cable for 28-pin DIP/PLCC (Part No. TMDS3788828)
  - Contains all the features of the CDT370 described previously but does not have the capability to program the data EEPROM and program EPROM
  - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
  - Allows qualification of breakpoints by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint

HP700 is a trademark of Hewlett-Packard Company.
Sun-3 and Sun-4 are trademarks of Sun Microsystems, Incorporated.

development system support (continued)

- Provides timers for analyzing total and average time in routines
- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and to trace display

- Microcontroller programmer
  - Base (Part No. TMDS3760500A – for PC, requires programmer head)
    - Single unit head for 28-pin PLCC (Part No. TMDS3780510A)
    - Single unit head for 28-pin DIP (Part No. TMDS3780511A)
  - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Design kit (Part No. TMDS3770110 – for PC)
  - Includes TMS370 Application Board and TMS370 Assembler diskette and documentation
  - Supports quick evaluation of TMS370 functionality
  - Capability to upload and download code
  - Capability to execute programs and software routines, and to single-step executable instructions
  - Software breakpoints to halt program execution at selected addresses
  - Wire-wrap prototype area
  - Reverse assembler
- Starter Kit (Part No. TMDS37000 – for PC)
  - Includes TMS370 Assembler diskette and documentation
  - Includes TMS370 Simulator
  - Includes programming adapter board and programming software
  - Does not include (to be supplied by the user)
    - + 5 V power supply
    - ZIF sockets
    - Nine-pin RS232 cable

device numbering conventions

Figure 12 illustrates the numbering and symbol nomenclature for the TMS370Cx1x family.

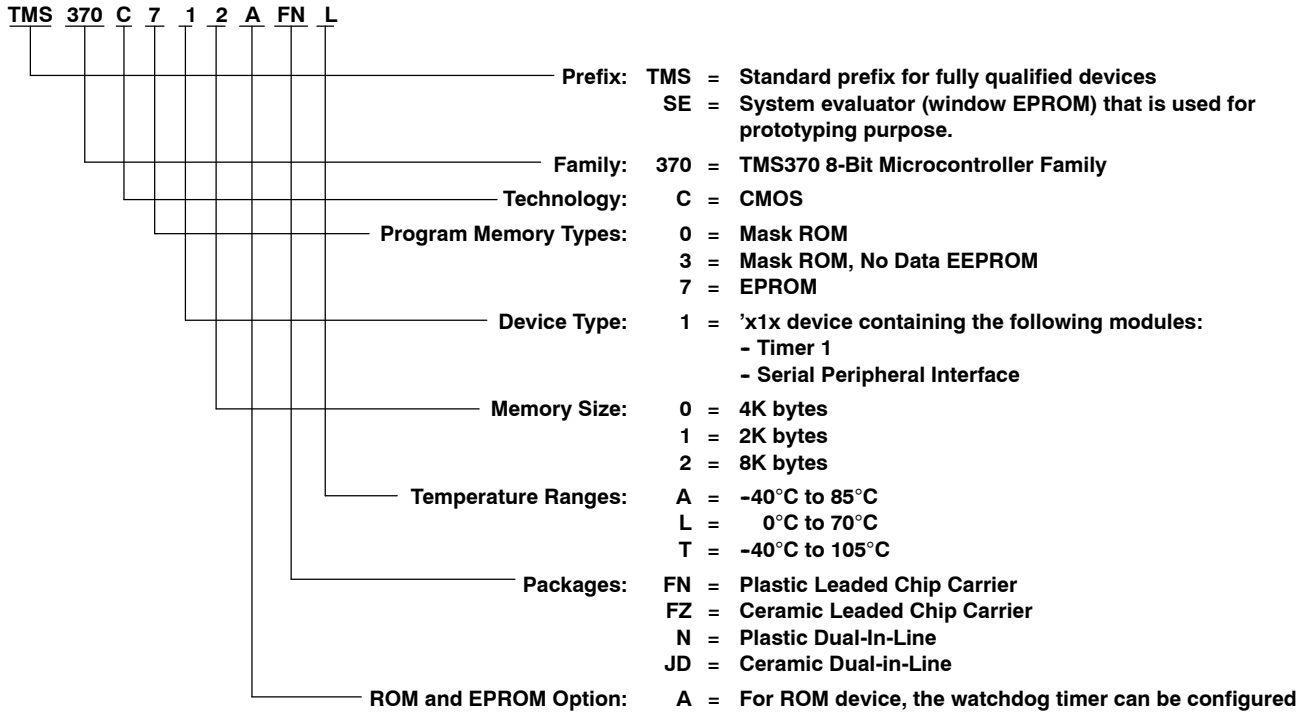


Figure 12. TMS370Cx1x Family Nomenclature

device part numbers

Table 18 provides all of the ’x1x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICES PART NUMBERS FOR 28 PINS (LCC)	DEVICES PART NUMBERS FOR 28 PINS (DIP)
TMS370C010AFNA TMS370C010AFNL TMS370C010AFNT	TMS370C010ANA TMS370C010ANL TMS370C010ANT
TMS370C012AFNA TMS370C012AFNL TMS370C012AFNT	TMS370C012ANA TMS370C012ANL TMS370C012ANT
TMS370C310AFNA TMS370C310AFNL TMS370C310AFNT	TMS370C310ANA TMS370C310ANL TMS370C310ANT
TMS370C311AFNA TMS370C311AFNL TMS370C311AFNT	TMS370C311ANA TMS370C311ANL TMS370C311ANT
TMS370C312AFNA TMS370C312AFNL TMS370C312AFNT	TMS370C312ANA TMS370C312ANL TMS370C312ANT
TMS370C712AFNT TMS370C712BFNT	TMS370C712ANT TMS370C712BNT
SE370C712AFZT† SE370C712BFZT†	SE370C712AJDT† SE370C712BJDT†

† System evaluators are for use in prototype environment and their reliability has not been characterized.

new code release form

Figure 13 shows a sample of the new code release form.

NEW CODE RELEASE FORM
TEXAS INSTRUMENTS
TMS370 MICROCONTROLLER PRODUCTS

DATE: _____

To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:

1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media)
2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.

Company Name: _____
Street Address: _____
Street Address: _____
City: _____ State _____ Zip _____

Customer Part Number: _____
Customer Application: _____

TMS370 Device: _____

TI Customer ROM Number: _____
(provided by Texas Instruments)

OSCILLATOR FREQUENCY

	MIN	TYP	MAX
[] External Drive (CLKIN)			
[] Crystal			
[] Ceramic Resonator			

[] Supply Voltage MIN: _____ MAX: _____
(std range: 4.5V to 5.5V)

TEMPERATURE RANGE
[] 'L': 0° to 70°C (standard)
[] 'A': –40° to 85°C
[] 'T': –40° to 105°C

SYMBOLIZATION
[] TI standard symbolization
[] TI standard w/customer part number
[] Customer symbolization
(per attached spec, subject to approval)

Contact Mr./Ms.: _____
Phone: (_____) _____ Ext.: _____

Customer Purchase Order Number: _____

Customer Print Number *Yes: ____ # _____
No: ____ (Std. spec to be followed)
*If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes	Watchdog counter	Clock Type
[] Enabled	[] Standard	[] Standard (/4)
[] Disabled	[] Hard Enabled	[] PLL (/1)
	[] Simple Counter	

NOTE:
Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE
[] 'N' 28-pin PDIP
[] "FN" 28-pin PLCC
[] "N" 40-pin PDIP
[] "NJ" 40-pin PSDIP (formerly known as N2)
[] "FN" 44-pin PLCC
[] "FN" 68-pin PLCC
[] "NM" 64-pin PSDIP

BUS EXPANSION
[] YES [] NO

NON-STANDARD SPECIFICATIONS:
ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.

RELEASE AUTHORIZATION:
This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.

1. Customer: _____ Date: _____

2. TI: Field Sales: _____
Marketing: _____
Prod. Eng.: _____
Proto. Release: _____

Figure 13. Sample New Code Release Form

Table 19 is a collection of all the peripheral file frames used in the ’Cx1x (provided for a quick reference).

Table 19. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	**AUTO WAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0)†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	SPI Module Control Register Memory Map								
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								

† D3 as SYSCLK, set port D control register 2 = 08h.

Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	**SPI STEST**	**SPI RIORITY**	**SPI ESPEN**	—	—	—	—	—	SPIPRI
	Timer1 Module Register Memory Map								
	Modes: Dual-Compare and Capture/Compare								
P040	Bit 15	T1Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 7	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Dual-Compare and Capture/Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.6 V to 7 V
Input voltage range, All pins except MC . . . . . –0.6 V to 7 V
MC . . . . . –0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current per buffer, I_O (V_O = 0 to V_{CC}) (see Note 2) . . . . . ±10 mA
Maximum I_{CC} current . . . . . 170 mA
Maximum I_{SS} current . . . . . – 170 mA
Continuous power dissipation . . . . . 500 mW
Operating free-air temperature range, T_A: L version . . . . . 0°C to 70°C
A version . . . . . –40°C to 85°C
T version . . . . . –40°C to 105°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS}.
2. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

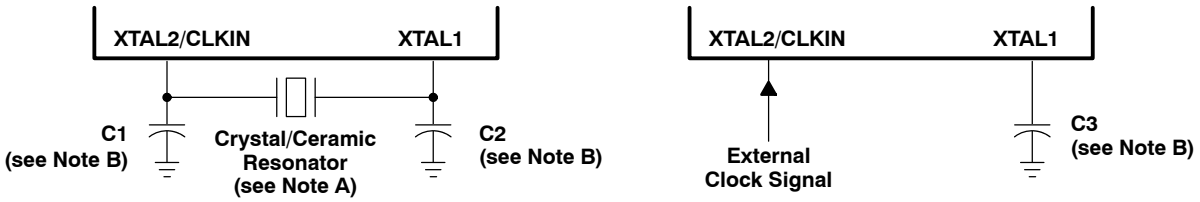
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		$\overline{\text{RESET}}$	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microcomputer	V_{SS}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS}.
3. $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is not within the recommended operating range.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

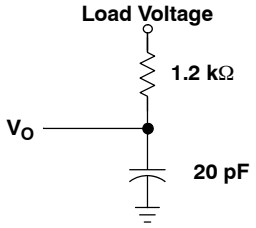
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = –50 μA	0.9 V_{CC}			V
			I_{OH} = –2 mA	2.4			
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	μA
			0.3 V < V_I ≤ 13 V			650	
			See Note 4 12 V ≤ V_I ≤ 13 V			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			± 10	μA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = 0.9 V_{CC}	– 50			μA
			V_{OH} = 2.4 V	– 2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)		See Notes 5 and 6 SYSCLK = 5 MHz		20	36	mA
			See Notes 5 and 6 SYSCLK = 3 MHz		13	25	
			See Notes 5 and 6 SYSCLK = 0.5 MHz		5	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)		See Notes 5 and 6 SYSCLK = 5 MHz		10	17	mA
			See Notes 5 and 6 SYSCLK = 3 MHz		6.5	11	
			See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)		See Notes 5 and 6 SYSCLK = 3 MHz		4.5	8.6	mA
			See Notes 5 and 6 SYSCLK = 0.5 MHz		1.5	3.0	
	Supply current (HALT mode)		See Note 5 XTAL2/CLKIN < 0.2 V		1	30	μA

NOTES: 4. Input current I_{PP} is a maximum of 50 mA only when you are programming EPROM.
5. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2V.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
7. Maximum operating current = 5.6 (SYSCLK) + 8 mA.
8. Maximum standby current = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
9. Maximum standby current = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, only valid up to 3 MHz SYSCLK).



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 14. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4$ V; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4$ V; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 15. Typical Output Load Circuit (See Note A)

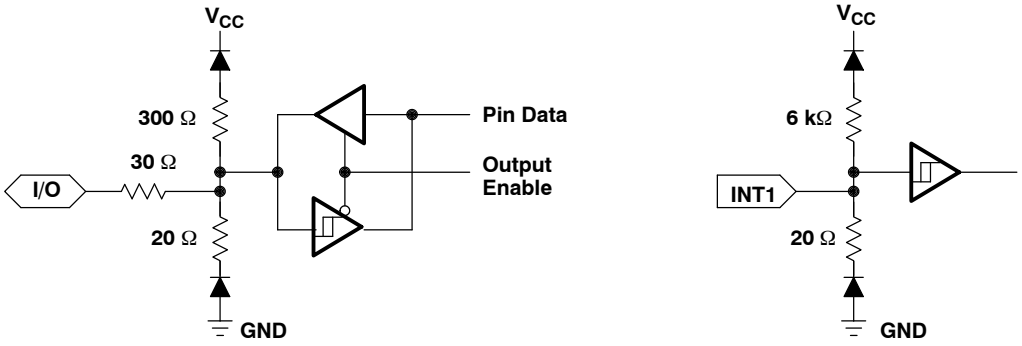


Figure 16. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	SC	SYSCLK
B	Byte	SIMO	SPISIMO
CI	XTAL2/CLKIN	SOMI	SPISOMI
M	Master mode	SPC	SPICLK
S	Slave mode		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 17 and Figure 18.

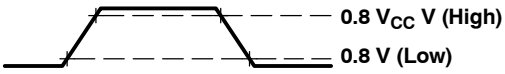


Figure 17. XTAL2/CLKIN Measurement Points

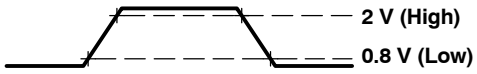


Figure 18. General Measurement Points

external clocking requirements for clock divided by 4 (see Note 10 and Figure 19)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency†	0.5	5	MHz

† SYSCLK = CLKIN/4

NOTES: 10. For V_{IL} and V_{IH}, refer to recommended operating conditions.

11. This pulse may be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

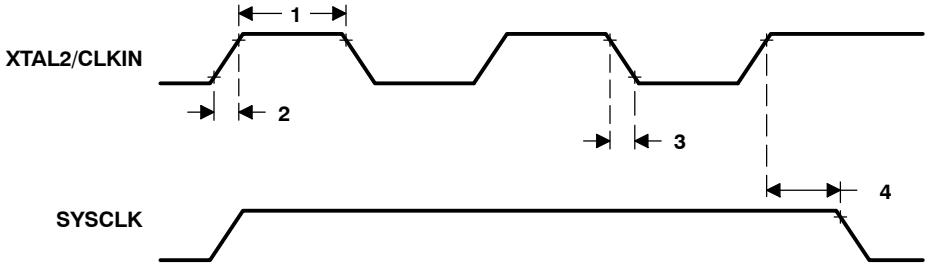


Figure 19. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 10 and Figure 20)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency‡	2	5	MHz

‡ SYSCLK = CLKIN/1

NOTES: 10. For V_{IL} and V_{IH}, refer to recommended operating conditions.

11. This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

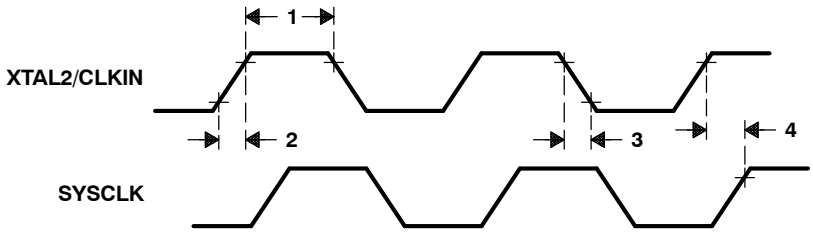


Figure 20. External Clock Timing for Divide-by-1

switching characteristics and timing requirements (see Note 12 and Figure 21)

NO.	PARAMETER			MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK	Divide by 4	200	2000	ns
			Divide by 1	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		0.5 t_c–20	0.5 t_c	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		0.5 t_c	0.5 t_c + 20	ns

NOTE 12: t_c = system-clock cycle time = 1/SYSCLK

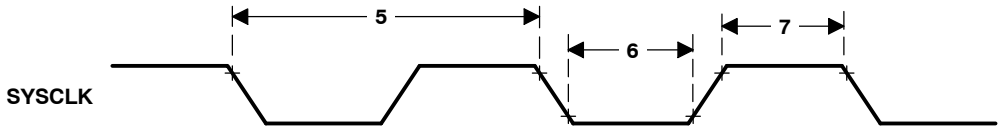


Figure 21. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 22)

		MIN	NOM	MAX	UNIT
t_r	Rise time		30		ns
t_f	Fall time		30		ns

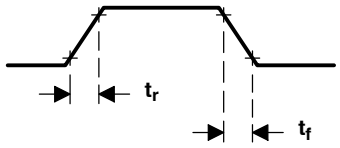


Figure 22. Signal Switching Timing

recommended EEPROM timing requirements for programming

		MIN	MAX	UNIT
$t_{w(PGM)B}$	Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$	Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.5	6	V
V_{PP}	Supply voltage at MC pin		13	13.2	13.5	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)			30	50	mA
SYSCLK	System clock	Divide by 4	0.5		5	MHz
		Divide by 1	2		5	

recommended EPROM timing requirements for programming

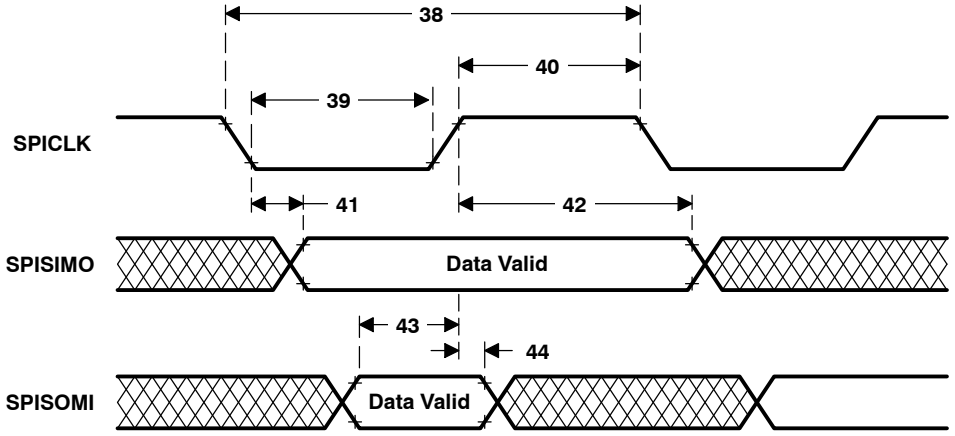
		MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$	Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

SPI master mode external timing characteristics and requirements (see Note 12 and Figure 23)

NO.			MIN	MAX	UNIT
38	$t_{c(SPC)M}$	Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)M}$	Pulse duration, SPICLK low	t_c – 45	$0.5t_{c(SPC)}$+45	ns
40	$t_{w(SPCH)M}$	Pulse duration, SPICLK high	t_c – 55	$0.5t_{c(SPC)}$+45	ns
41	$t_{d(SPCL-SIMOV)M}$	Delay time, SPISIMO valid after SPICLK low (polarity = 1)	– 65	50	ns
42	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (polarity =1)	$t_{w(SPCH)}$ – 50		ns
43	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI to SPICLK high (polarity = 1)	0.25 t_c + 150		ns
44	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 12: t_c = system-clock cycle time = 1/SYSCLK



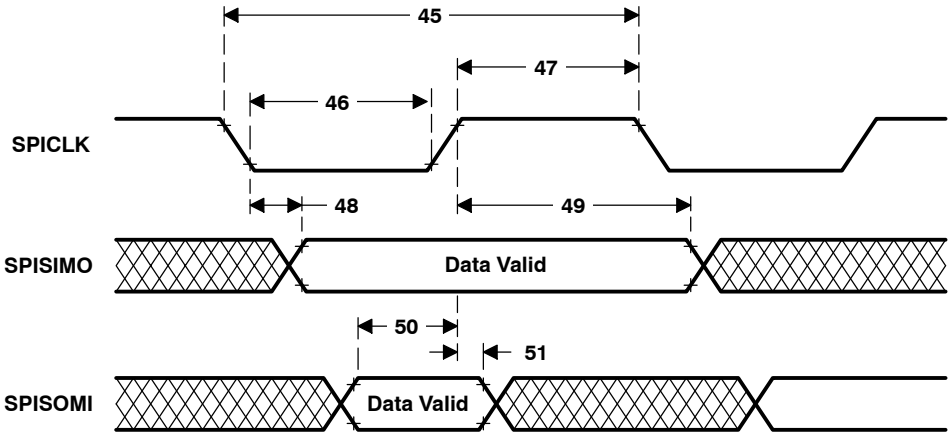
NOTE A: The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 23. SPI Master External Timing

SPI slave mode external timing characteristics and requirements (see Note 12 and Figure 24)

NO.			MIN	MAX	UNIT
45	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)S}$	Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)S}+45$	ns
47	$t_{w(SPCH)S}$	Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)S}+45$	ns
48	$t_{d(SPCL-SOMIV)S}$	Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (polarity =1)	$t_{w(SPCH)S}$		ns
50	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_C + 100$		ns

NOTE 12: t_c = system-clock cycle time = 1/SYSCLK



NOTE A: The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 24. SPI Slave External Timing

Table 20 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

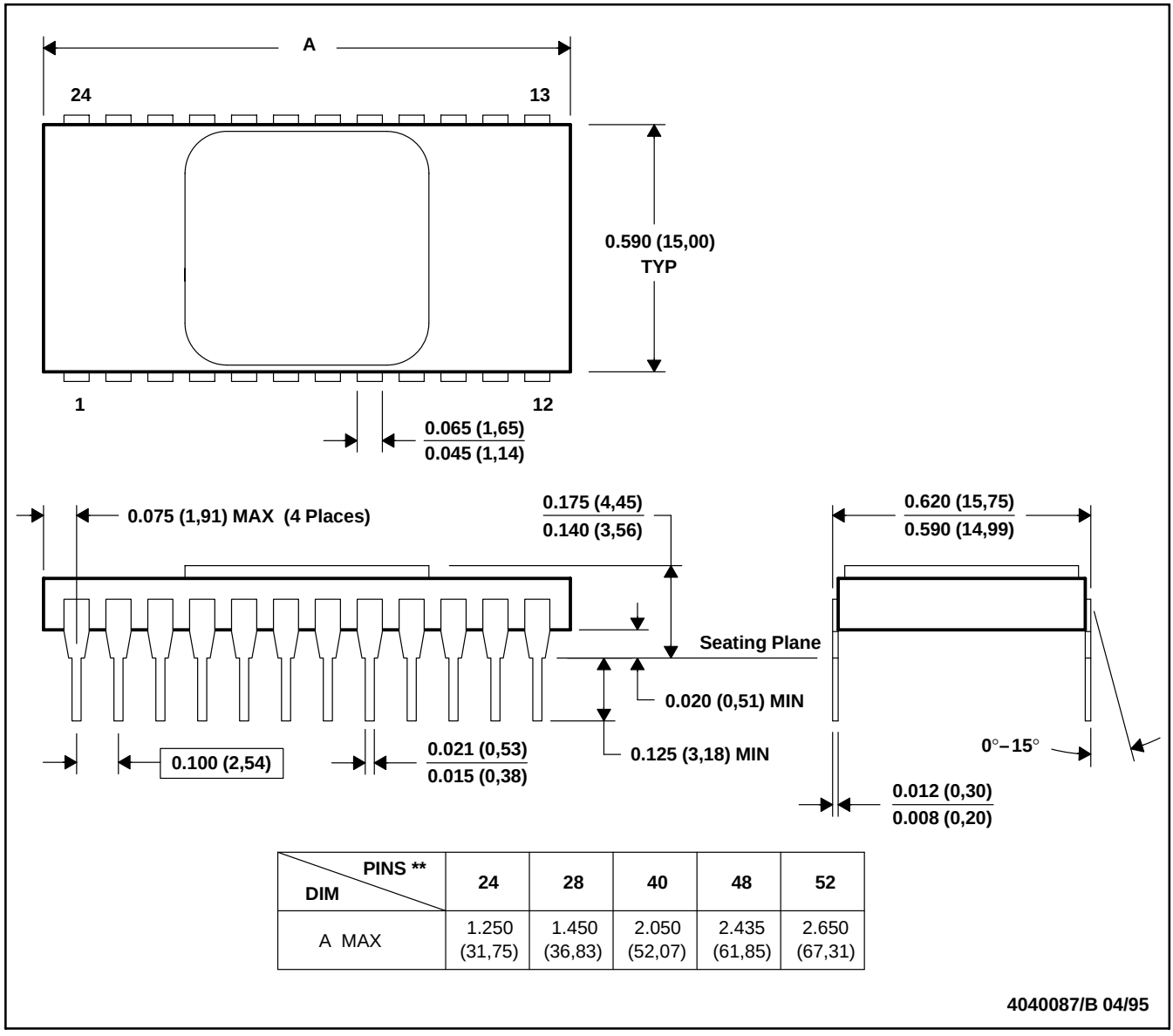
Table 20. TMS370Cx1x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 28 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C010AFNA TMS370C010AFNL TMS370C010AFNT TMS370C012AFNA TMS370C012AFNL TMS370C012AFNT TMS370C310AFNA TMS370C310AFNL TMS370C310AFNT TMS370C311AFNA TMS370C311AFNL TMS370C311AFNT TMS370C312AFNA TMS370C312AFNL TMS370C312AFNT TMS370C712AFNT TMS370C712BFNT
FZ – 28 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C712AFZT SE370C712BFZT
JD – 28 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C712AJDT SE370C712BJDT
N – 28 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C010ANA TMS370C010ANL TMS370C010ANT TMS370C012ANA TMS370C012ANL TMS370C012ANT TMS370C310ANA TMS370C310ANL TMS370C310ANT TMS370C311ANA TMS370C311ANL TMS370C311ANT TMS370C312ANA TMS370C312ANL TMS370C312ANT TMS370C712ANT TMS370C712BNT

MCDI005 – JANUARY 1998

JD (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**

24 PINS SHOWN



DIM \ PINS **	24	28	40	48	52
A MAX	1.250 (31,75)	1.450 (36,83)	2.050 (52,07)	2.435 (61,85)	2.650 (67,31)

4040087/B 04/95

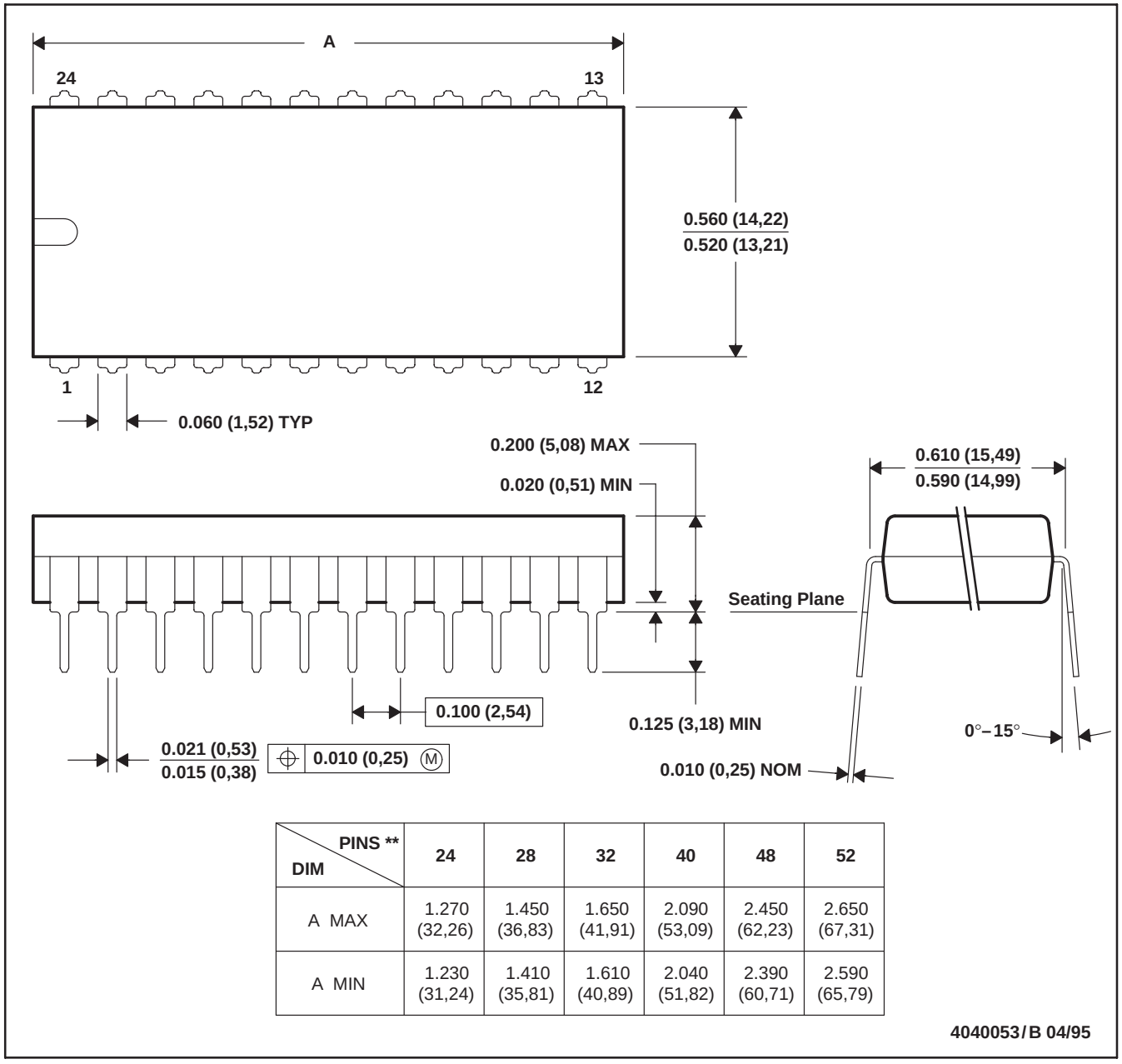
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold-plated.

MPDI008 – OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

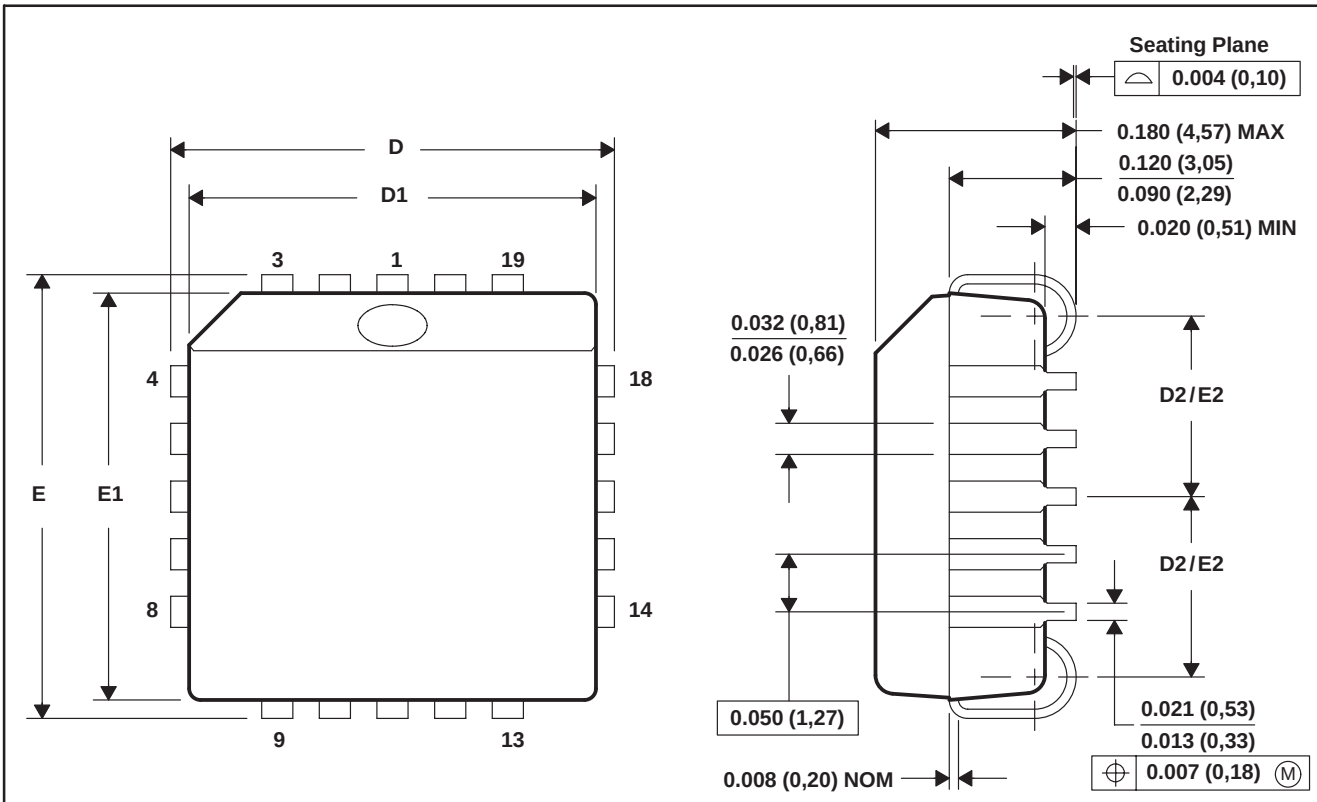
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

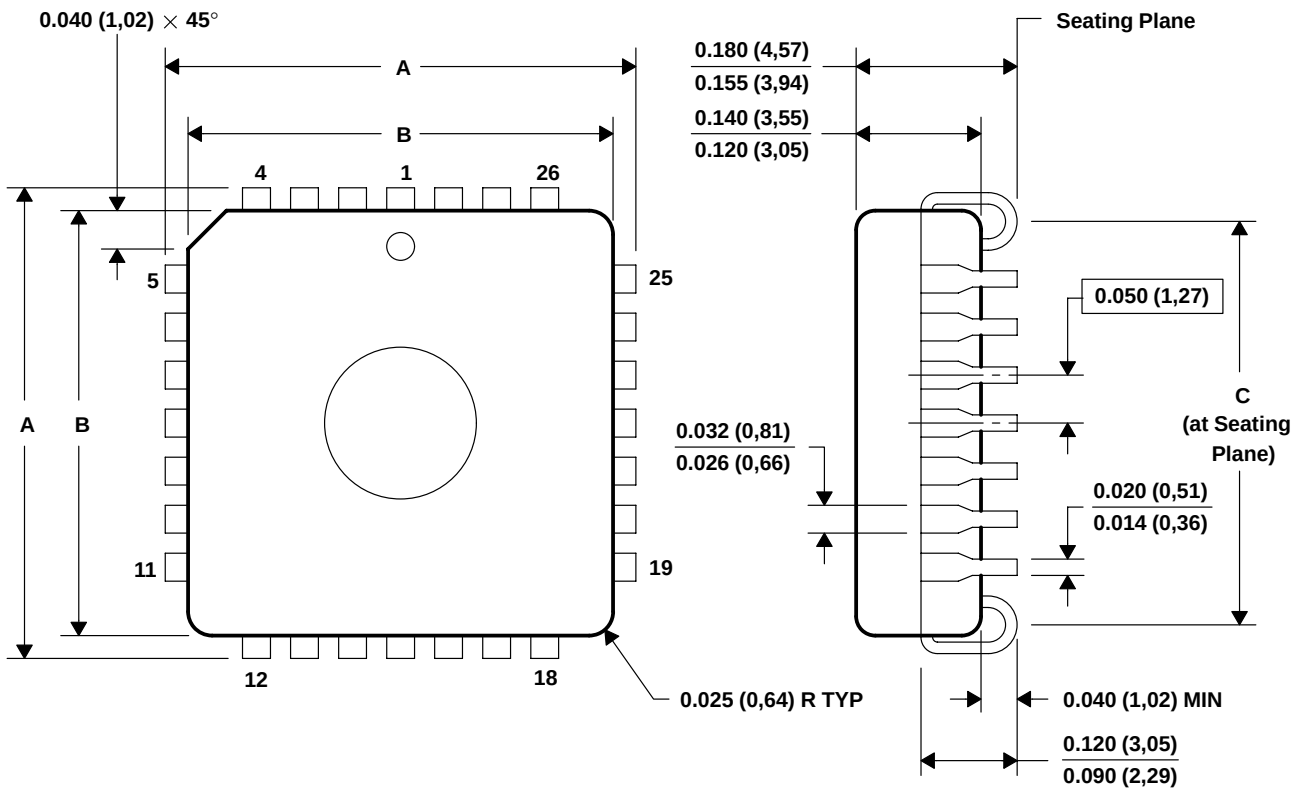
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MJLC003A – FEBRUARY 1995

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



JEDEC OUTLINE	NO. OF PINS**	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	0.485 (12,32)	0.495 (12,57)	0.430 (10,92)	0.455 (11,56)	0.410 (10,41)	0.430 (10,92)
MO-087AB	44	0.685 (17,40)	0.695 (17,65)	0.630 (16,00)	0.655 (16,64)	0.610 (15,49)	0.630 (16,00)
MO-087AC	52	0.785 (19,94)	0.795 (20,19)	0.730 (18,54)	0.765 (19,43)	0.680 (17,28)	0.740 (18,79)
MO-087AD	68	0.985 (25,02)	0.995 (25,27)	0.930 (23,62)	0.955 (24,26)	0.910 (23,11)	0.930 (23,62)

4040219/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SE370C712AFZT	OBSOLETE	JLCC	FZ	28		TBD	Call TI	Call TI			
SE370C712AJDT	OBSOLETE	CDIP SB	JD	28		TBD	Call TI	Call TI			
SE370C712BFZT	OBSOLETE	JLCC	FZ	28		TBD	Call TI	Call TI			
SE370C712BJDT	OBSOLETE	CDIP SB	JD	28		TBD	Call TI	Call TI			
TMS370C012AFNA	NRND	PLCC	FN	28		TBD	Call TI	Call TI			
TMS370C012AFNL	NRND	PLCC	FN	28		TBD	Call TI	Call TI			
TMS370C310AFNA	NRND	PLCC	FN	28		TBD	Call TI	Call TI			
TMS370C310AFNL	NRND	PLCC	FN	28		TBD	Call TI	Call TI			
TMS370C712AFNT	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI		TMS @1986 TI 370C712AFNT	
TMS370C712BFNT	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI			
TMS370C712BNT	OBSOLETE	PDIP	N	28		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265