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National Semiconductor

July 2000

DS96F173M/DS96F175C/DS96F175M EIA-485/EIA-422 Quad Differential Receivers

General Description

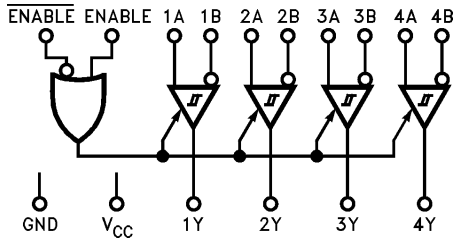
The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Features

- Meets EIA-485, EIA-422A, EIA-423A standards
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Reduced power consumption (I_{CC} = 50 mA max)
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Military temperature range available
- Qualified for MIL STD 883C
- Available to standard military drawings (SMD)
- Available in DIP(J), LCC(E), and FlatPak (W) packages
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

Logic Diagrams



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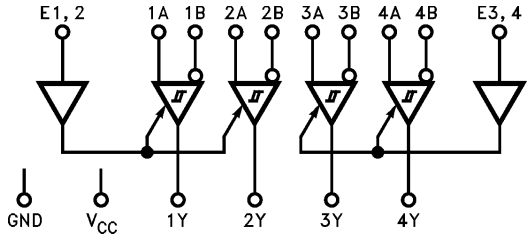
DS96F175



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Function Tables

(Each Receiver) DS96F173

Differential Inputs	Enable		Output
A–B	E	$\overline{E}$	Y
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

(Each Receiver) DS96F175

Differential Inputs	Enable	Output
A–B	E	Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

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Absolute Maximum Ratings COMMERCIAL(Note 2)

Specifications for the 883 version of this product are listed separately.

Storage Temperature Range (T_{STG})	−65˚C to +175˚C
Lead Temperature (Soldering, 60 sec.)	300˚C
Max. Package Power Dissipation (Note 1) at 25˚C	
Ceramic DIP (J)	1500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F175C	4.75	5.0	5.25	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	µA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A)				
DS96F175C	0	25	70	˚C

Note 1: Derate package 10 mW/˚C above 25˚C.

Electrical Characteristics (Notes 3, 4)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	$V_O = V_{OH}$				0.2	V
V_{TL}	Differential-Input (Note 5) Low Threshold Voltage	$V_O = V_{OL}$		−0.2			V
$V_{TH} - V_{TL}$	Hysteresis (Note 6)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV	0˚C to +70˚C	2.8			V
		I_{OH} = −400 µA	−55˚C to +125˚C	2.5			
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 11 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4V to 2.4V				±20	µA
I_I	Line Input Current (Note 7)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	µA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	µA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 8)		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			50	

COMMERCIAL

Switching Characteristics

V_{CC} = 5.0V, T_A = 25˚C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = –2.5V to +2.5V, C_L = 15 pF, *Figure 1*	5.0	15	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	V_{CM} = 0V	5.0	15	22	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*		12	16	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*		13	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2*		14	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*		14	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 1*		1.0	3.0	ns

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0˚C to +70˚C range for the DS96F175C. All typicals are given for V_{CC} = 5V and T_A = 25˚C.

Note 4: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 5: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 6: Hysteresis is the difference between the positive-going input threshold voltage. V_{TH}, and the negative going input threshold voltage, V_{TL}.

Note 7: Refer to EIA-485 Standard for exact conditions.

Note 8: Only one output at a time should be shorted.

Order Number: DS96F175CJ
See NS Package Number J16A

MIL-STD-883C

Absolute Maximum Ratings (Note 2)

For complete Military Specifications, refer to the appropriate SMD or MDS.

Storage Temperature Range (T_{STG})	−65˚C to +175˚C
Lead Temperature (Soldering, 60 sec.)	300˚C
Max. Package Power Dissipation (Note 9) at 25˚C	
Ceramic DIP (J)	1500 mW
Ceramic Flatpak (W)	1034 mW
Ceramic LCC (E)	1500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F173M/DS96F175M	4.50	5.0	5.50	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	µA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A)				
DS96F173M/DS96F175M	−55	25	125	˚C

Note 9: Above T_A = 25˚C derate J package 10 mW/˚C, W package 6.90 mW/˚C, E package 11.11 mW/˚C.

Electrical Characteristics (Notes 3, 4)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V			0.2	V
V_{TL}	Differential-Input (Note 5) Low Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V		−0.2		V
V_{IH}	Enable Input Voltage HIGH			2.0		V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA, V_{CC} = 4.5V			−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV I_{OH} = −400 µA	−55˚C to +125˚C	2.5		V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8.0 mA		0.45	V
I_{OZ}	High-Impedance State Output	V_O = 0.4V, 2.4V, V_{CC} = 5.5V			±20	µA
I_I	Line Input Current (Note 7)	Other Input = 0V	V_I = 12V		1.0	mA
			V_I = −7.0V		−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V, V_{CC} = 5.5V			20	µA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V, V_{CC} = 5.5V			−100	µA
R_I	Input Resistance			10		kΩ
I_{OS}	Short Circuit Output Current	(Note 8)		−15	−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		50	mA
I_{CCX}						

MIL-STD-883C

Switching Characteristics

V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25˚C		T_A = −55˚C	T_A = 125˚C	Units
			Typ	Max	Max	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, *Figure 1*	15	22	30	30	ns
t_{PHL}	Propagation Delay Time,	V_{CM} = 0V	15	22	30	30	ns

MIL-STD-883C (Continued)

Switching Characteristics (Continued)

V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25˚C		T_A = −55˚C	T_A = 125˚C	Units
			Typ	Max	Max	Max	
	High to Low Level Output						
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*	12	16	27	27	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*	13	18	27	27	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2*(Note 15)	14	20	27	27	ns
		C_L = 20 pF, *Figure 2*(Note 15)	14	30	37	37	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*	14	18	30	30	ns
$\|t_{PLH}-t_{PHL}\|$	Pulse Width Distortion (SKEW)	*Figure 1*	1	3	5.0	5.0	ns

SMD Number:

DS96F173MJ	**5962-9076602 MEA**
DS96F173MW	**5962-9076602 MFA**
DS96F173ME	**5962-9076602 M2A**
DS96F175MJ	**5962-9076601 MEA**
DS96F175MW	**5962-9076601 MFA**
DS96F175ME	**5962-9076601 M2A**

Order Number:

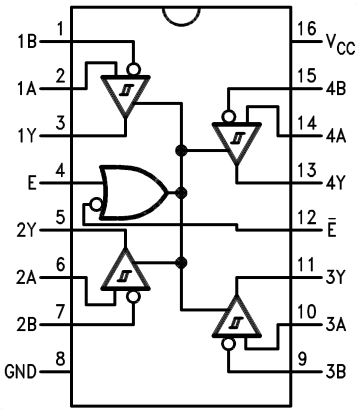
883 Marking	SMD Marking
DS96F173MJ/883	**DS96F173MJ-SMD**
DS96F175MJ/883	**DS96F175MJ-SMD**
See NS Package Number J16A	
DS96F173ME/883	**DS96F173ME-SMD**
DS96F175ME/883	**DS96F175ME-SMD**
See NS Package Number E20A	
DS96F173MW/883	**DS96F173MW-SMD**
DS96F175MW/883	**DS96F175MW-SMD**
See NS Package Number W16A	

For complete Military Product Specifications, refer to the appropriate SMD or MDS.

Connection Diagrams

16-Lead Ceramic Dual-In-Line Package
NS Package Number J16A

DS96F173



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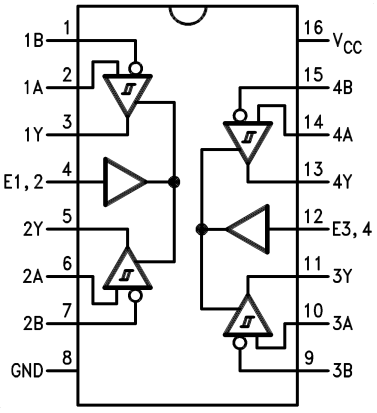
Top View

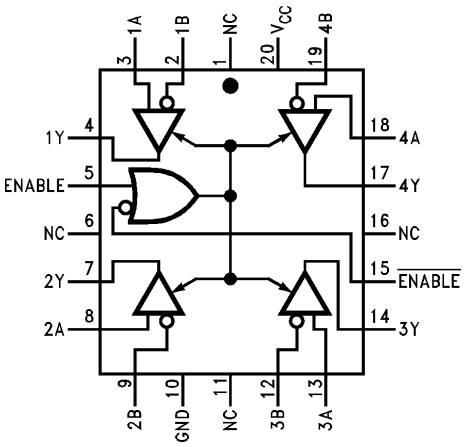
DS96F175



00962702

Top View

20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



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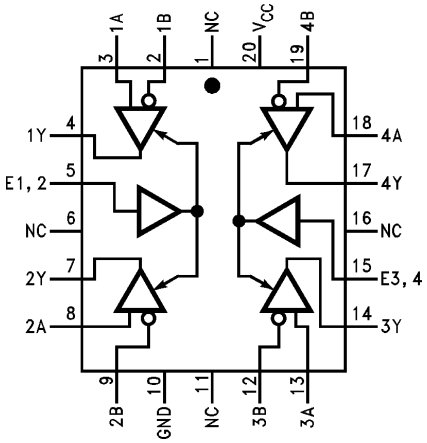
*NC — No Connection

Top View



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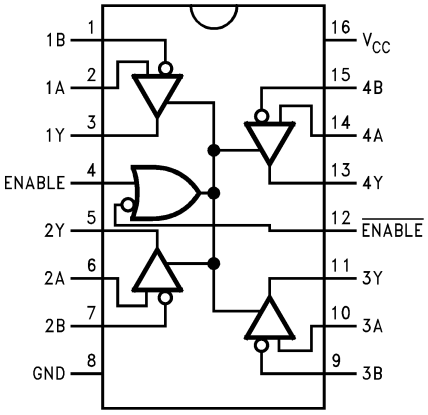
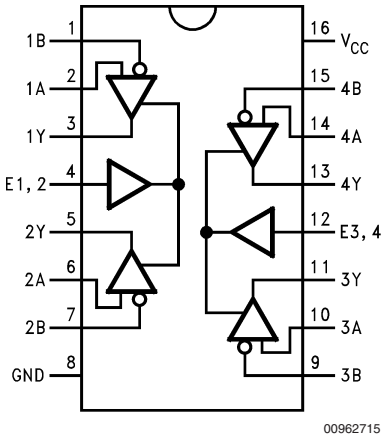
Top View

16-Lead Ceramic Flatpak
NS Package Number W16A

Connection Diagrams (Continued)



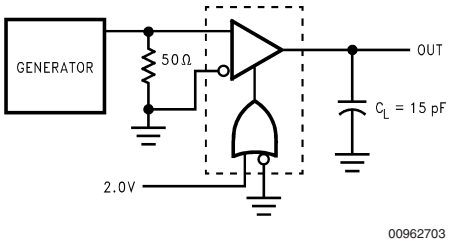
Top View



Top View

Order Numbers are located at the end of the respective Electrical Tables.

Parameter Measurement Information



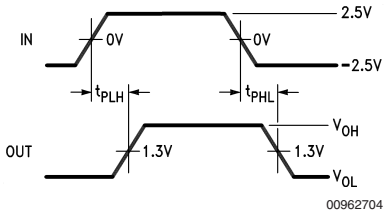
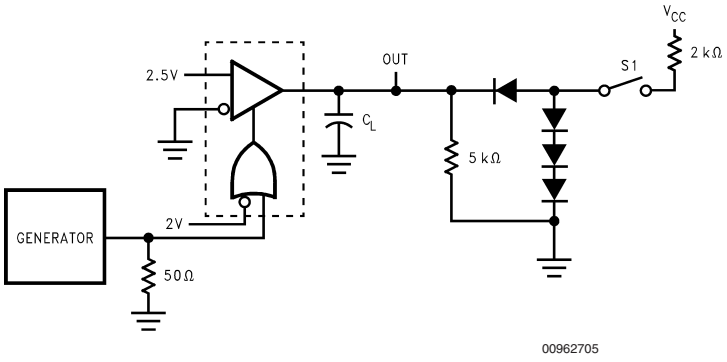


FIGURE 1. t_{PLH}, t_{PHL} (Notes 10, 11)



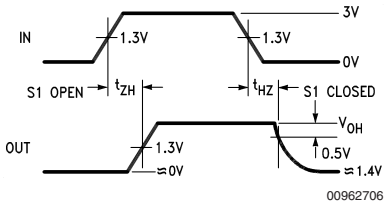


FIGURE 2. t_{HZ}, t_{ZH} (Notes 10, 11, 13, 14)

Parameter Measurement Information (Continued)

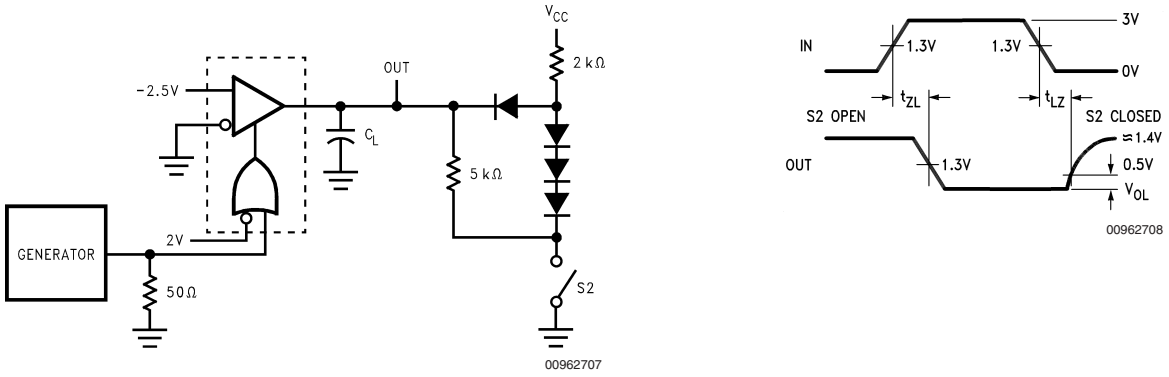


FIGURE 3. t_{ZL}, t_{LZ} (Notes 10, 11, 13, 14)

Note 10: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, $t_r \le 6.0$ ns, $t_f \le 6.0$ ns, $Z_O = 50\Omega$.

Note 11: C_L includes probe and stray capacitance.

Note 12: DS96F173 with active high and active low Enables are shown. DS96F175 has active high Enable only.

Note 13: All diodes are 1N916 or equivalent.

Note 14: To test the active low Enable $\overline{E}$ of DS96F173, ground E and apply an inverted input waveform to $\overline{E}$. DS96F175 has active high enable only.

Note 15: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application

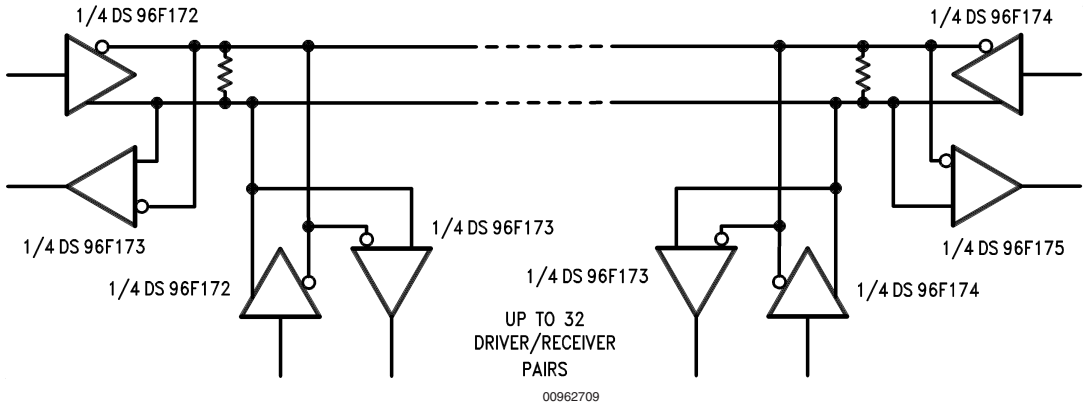
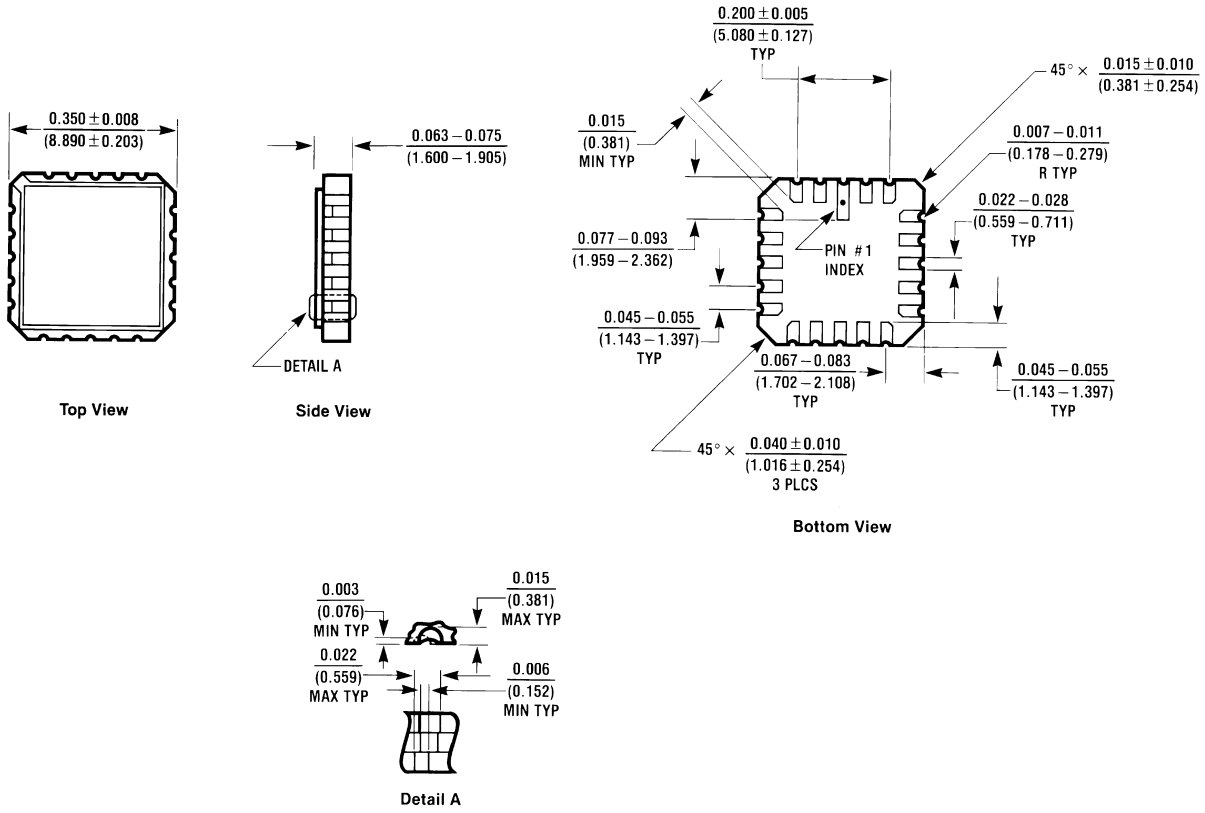


FIGURE 4.

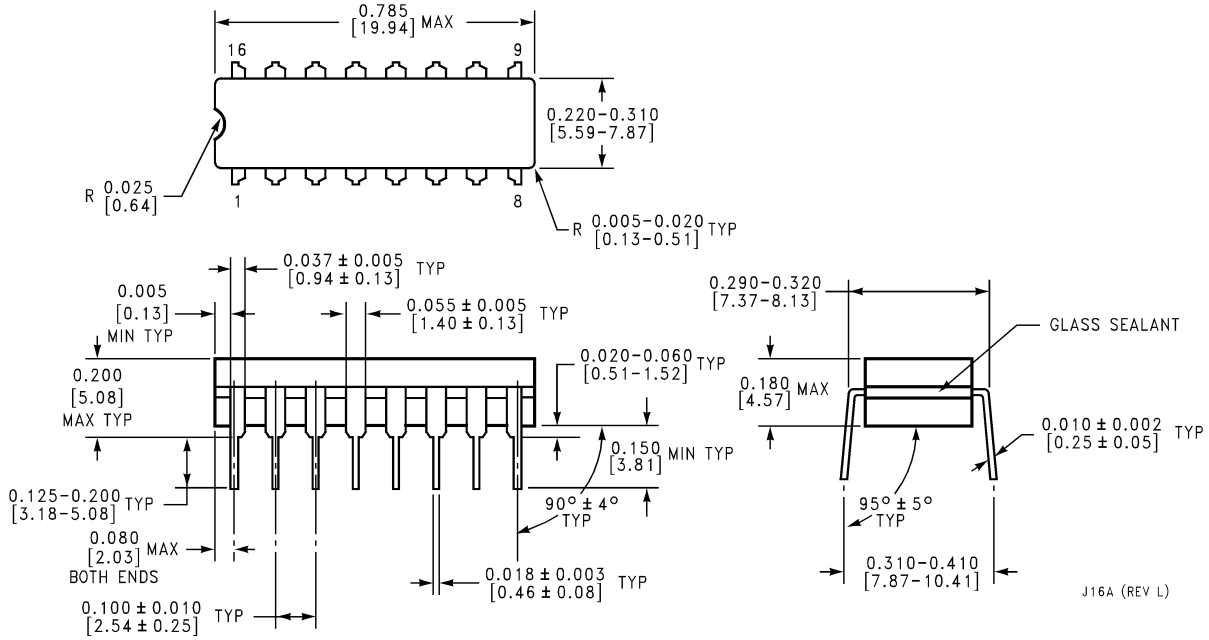
Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Physical Dimensions inches (millimeters)

unless otherwise noted

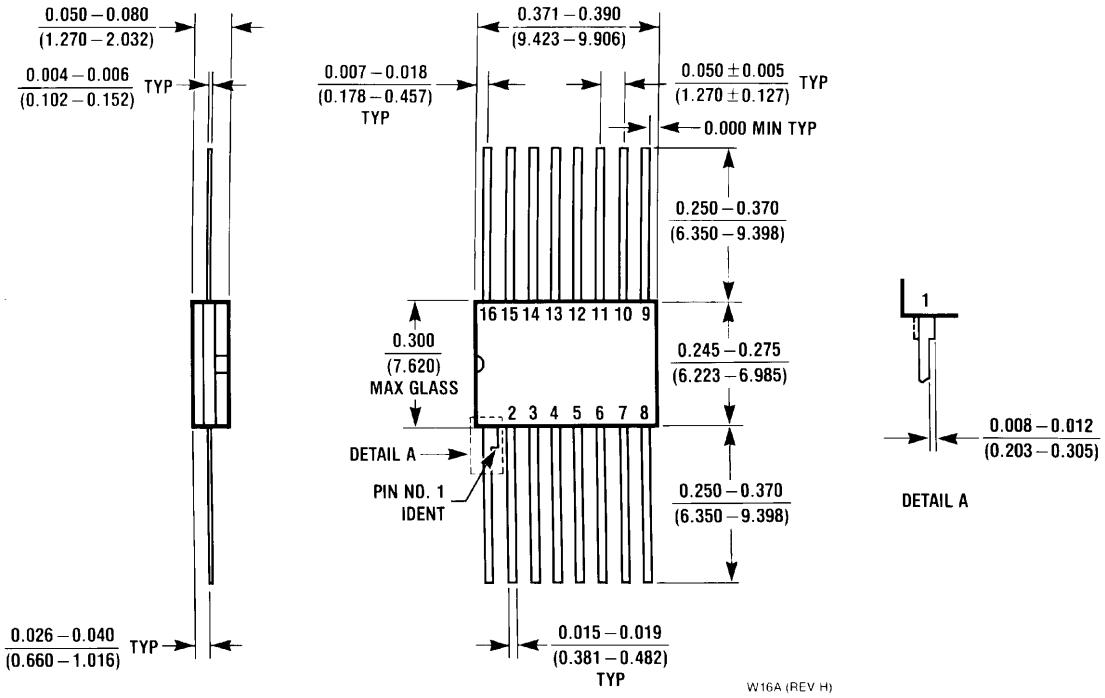


20-Lead Ceramic Leadless Chip Carrier (E)
Order Number DS96F173ME/883 or DS96F175ME/883
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
Order Number DS96F175CJ, DS96F173MJ/883 or DS96F175MJ/883
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic FlatPak (W)
Order Number DS96F173MW/883 or DS96F175MW/883
NS Package Number W16A

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