National Semiconductor

February 1993

74BCT573
Octal D Latch with TRI-STATE® Outputs

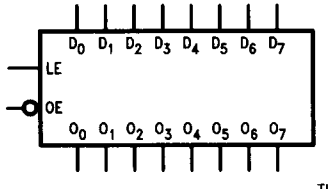
General Description

The 'BCT573 consists of eight latches with TRI-STATE outputs for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. This device is functionally identical to the "BCT373 but has a broadside pinout.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to the 'BCT373
- TRI-STATE outputs for bus interfacing
- Guaranteed 2000V minimum ESD protection
- Guaranteed multiple output switching specifications
- Guaranteed 500 mA minimum latchup protection
- Low I_{CCZ} through BiCMOS techniques
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Logic Symbol



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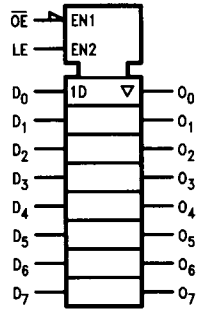
IEEE/IEC



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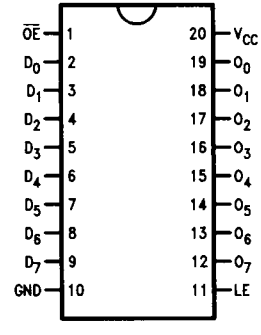
Connection Diagram

Pin Assignment for DIP and SOIC



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Functional Description

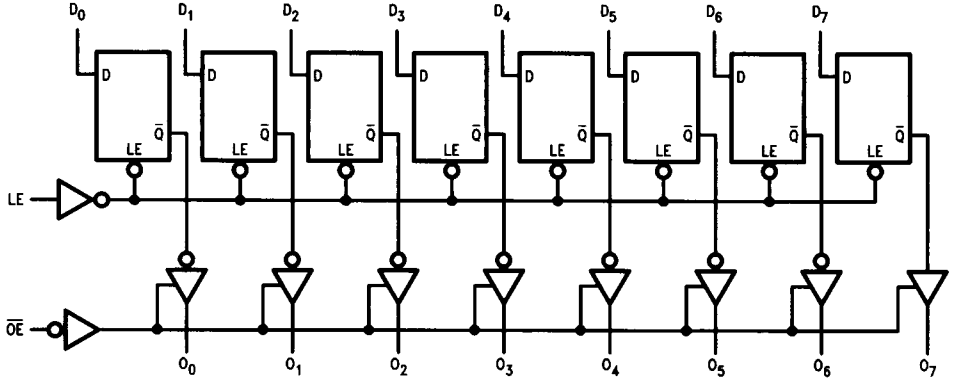
The 'BCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfer with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
O_0 = Value stored from previous clock cycle

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	0V–5.5V	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	0V–5.5V	V_{OUT} = 0.5V
I_{OZ}	Output Leakage Current			±20	μA	0V–2.0V 1.8V–0V	$\overline{OE}$ = 2.0V, V_{OUT} = 0.5V or 2.7V (Power Up) $\overline{OE}$ = 2.0V, V_{OUT} = 0.5V or 2.7V (Power Down)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		8	12	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		29	48	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	8	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$		Units
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.5	4.0 7.4	8.4 10.5	2.0 3.5	8.4 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	3.0 3.0	6.8 5.7	8.9 8.3	3.0 3.0	8.9 8.3	ns
t_{PZH} t_{PZL}	Output Enable Time	3.7 3.7	6.1 6.5	10.0 10.0	3.7 3.7	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.2 2.2	4.8 4.8	7.0 7.0	2.2 2.2	7.0 7.0	ns

AC Operating Requirements

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE	1.0 1.0		1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	4.0 4.0		4.0 4.0		ns
$t_w(H)$	LE Pulse Width, HIGH	4.0		4.0		ns

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50\ pF$ 8 Outputs Switching (Note 1)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 1 Output Switching (Note 2)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250\ pF$ 8 Outputs Switching (Notes 1, 2)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.5	10.0 13.0	3.0 4.0	9.5 13.0	4.0 6.0	12.0 16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	4.0 4.0	10.0 9.5	4.0 4.0	12.0 10.0	6.0 6.0	14.5 13.0	ns

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc).

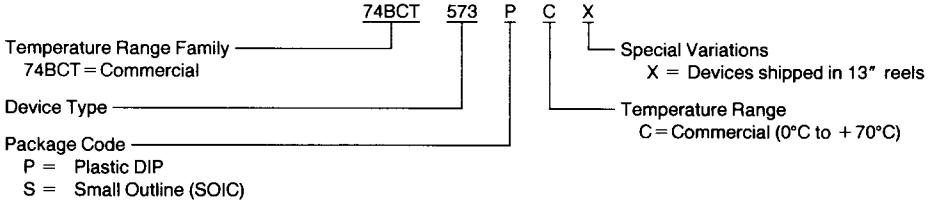
Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

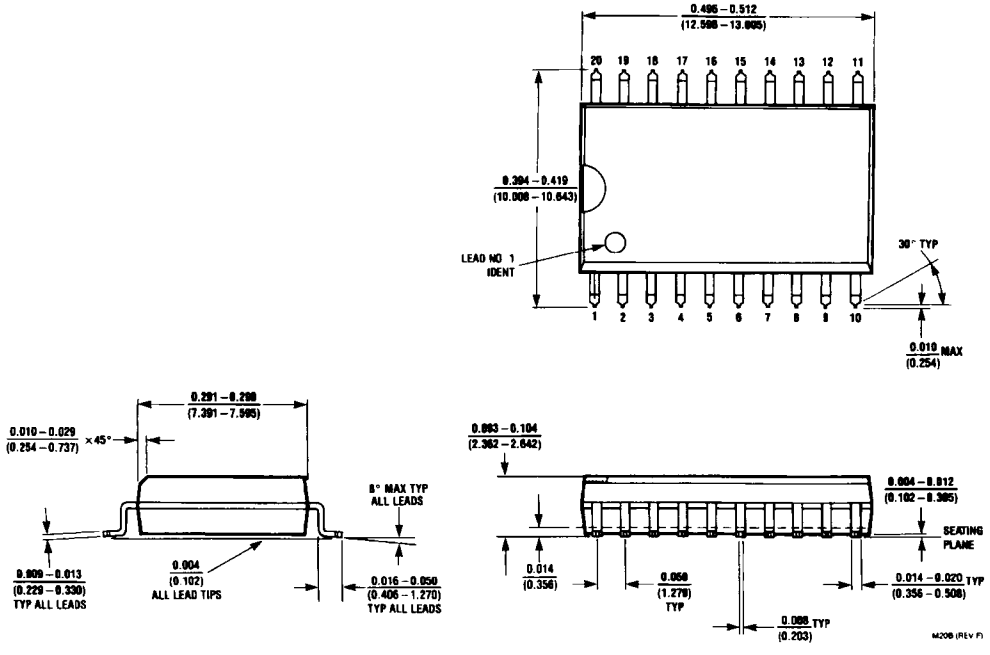
Symbol	Parameteer	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	10.0	pF	V_{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

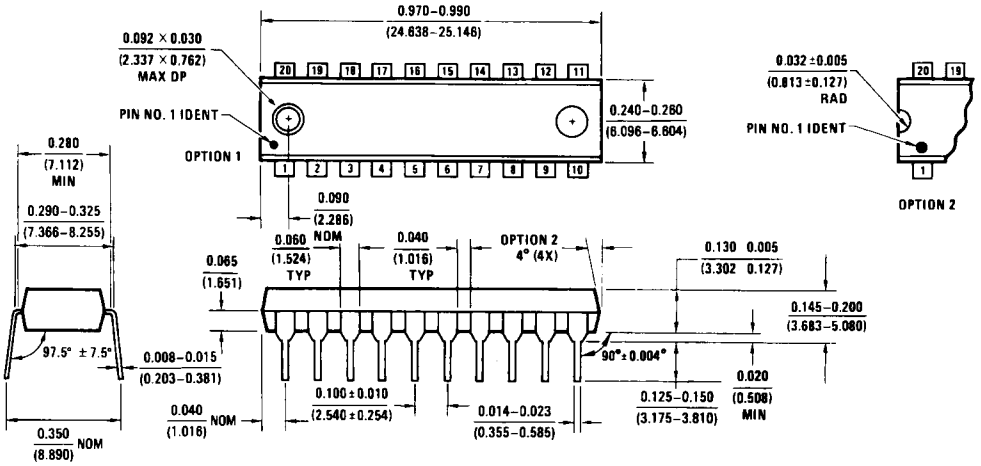


Physical Dimensions inches (millimeters)



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Fürstenfeldbruck
Germany
Tel: (0-81-41) 103-0
Telex: 527649
Fax: (0-81-41) 10-35-06

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15-3 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-3299-7001
FAX: 3-3299-7000

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 737-1600
Telex: 51292 NSHKL
Fax: (852) 736-9960

National Semicondutores Do Brazil Ltda.
Av. Brig. Faria Lima, 1409
6 Andar
Cep-01
Sao F
Tel: (
Telex
Fax: (

National Semiconductor (Australia) Pty, Ltd.
16 Business Park Dr.
Notting Hill, VIC 3168

035492