National Semiconductor

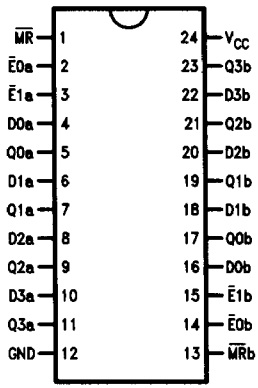
93L08
Dual 4-Bit Latch

General Description

The 93L08 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input and active LOW Enable inputs.

Connection Diagram

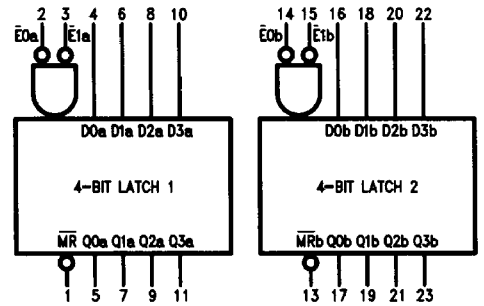
Dual-In-Line Package



TL/F/9594-1

Order Number 93L08DMQB or 93L08FMQB
See NS Package Number J24A or W24C

Logic Symbol



TL/F/9594-2

V_{CC} = Pin 24
GND = Pin 12

Pin Names	Description
D0a–D3a, D0b–D3b	Parallel Latch Inputs
$\overline{E}$0a, $\overline{E}$1a, $\overline{E}$0b, $\overline{E}$1b,	AND Enable Inputs (Active LOW)
$\overline{MR}$a, $\overline{MR}$b	Master Reset Inputs (Active LOW)
Q0a–Q3a, Q0b–Q3b	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	8			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	1			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	18			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	4			ns
t_w (L)	$\overline{E}_n$ Pulse Width LOW	32			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	30			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			D_n			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			D_n			−640	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				29	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 3 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}n$ to Qn		45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to Qn		27 29	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		30	ns

Functional Description

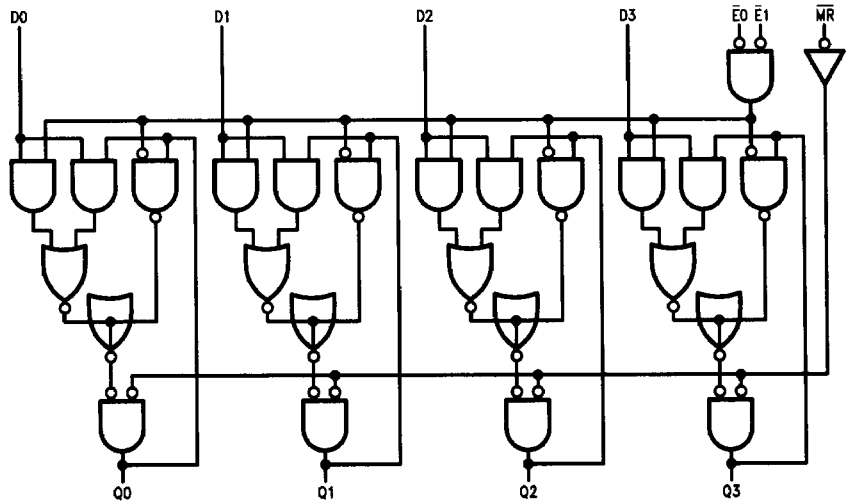
Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Truth Table

$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D	Qn	Operation
H	L	L	L	L	Data Entry
H	L	L	H	L	Data Entry
H	L	H	X	Qn−1	Hold
H	H	L	X	Qn−1	Hold
H	H	H	X	Qn−1	Hold
L	X	X	X	L	Reset

Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9594-3