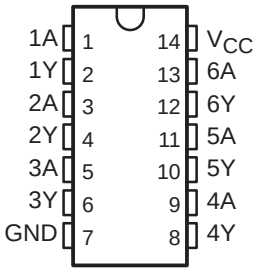
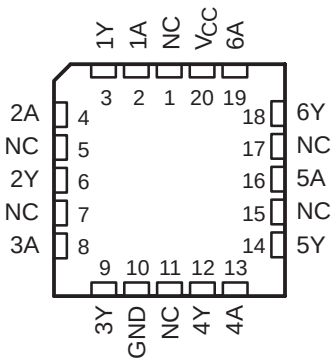
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **2-V to 5.5-V V_{CC} Operation**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Outputs Are Disabled During Power Up and Power Down With Inputs Tied to GND**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

SN54LV06A . . . J OR W PACKAGE
SN74LV06A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV06A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These hex inverter buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The ’LV06A devices perform the Boolean function $Y = \overline{A}$ in positive logic.

The open-drain outputs require pullup resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

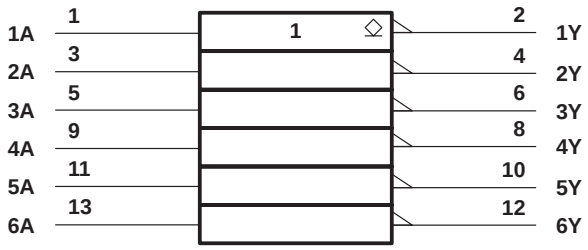
These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

The SN54LV06A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV06A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

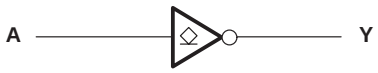
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the power-off state, V_O (see Note 1) . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . –50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . –35 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
DGV package . . . . . 127°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV06A		SN74LV06A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	5.5	0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LV06A			SN74LV06A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	I_{OL} = 50 μA		2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA		2.3 V			0.4			0.4	
	I_{OL} = 8 mA		3 V			0.44			0.44	
	I_{OL} = 16 mA		4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND		0 V to 5.5 V			±1			±1	μA
I_{OH}	$V_I = V_{IL}$,	$V_{OH} = V_{CC}$	5.5 V			±2.5			±2.5	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V		0 V			5			5	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		1.6			1.6		pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV06A		SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5.4*	10.4*	1*	13*	1	13	ns
t_{PHL}	A	Y			7.2*	10.4*	1*	13*	1	13	
t_{PLH}	A	Y	C_L = 50 pF		9.7	15.2	1	18	1	18	ns
t_{PHL}	A	Y			9.3	15.2	1	18	1	18	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV06A		SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		4.1*	7.1*	1*	8.5*	1	8.5	ns
t_{PHL}	A	Y			4.9*	7.1*	1*	8.5*	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.1	10.6	1	12	1	12	ns
t_{PHL}	A	Y			6.4	10.6	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV06A		SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3*	5.5*	1*	6.5*	1	6.5	ns
t_{PHL}	A	Y			3.3*	5.5*	1*	6.5*	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		4.8	7.5	1	8.5	1	8.5	ns
t_{PHL}	A	Y			4.4	7.5	1	8.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

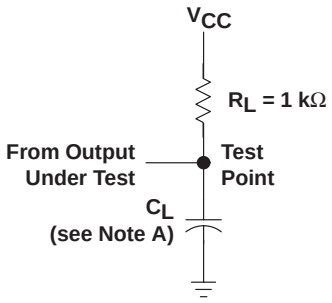
PARAMETER		SN74LV06A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

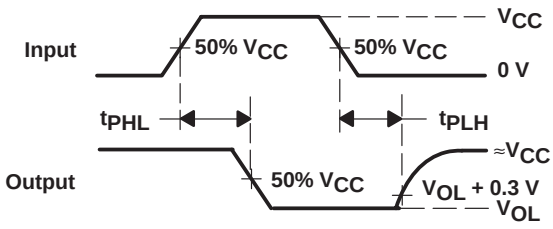
operating characteristics, T_A = 25°C

C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	2.6	pF
			5 V	4.7	

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
OPEN-DRAIN OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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