National Semiconductor

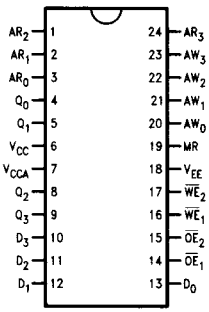
100145 16 x 4-Bit Register File Random Access Memory

General Description

The 100145 is a 64-bit register file organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the Write mode and the latches are in a Hold mode. When either $\overline{WE}$ input is HIGH, the circuit is in the Read mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active-LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches, and forces the outputs LOW.

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



TL/D/9638–1

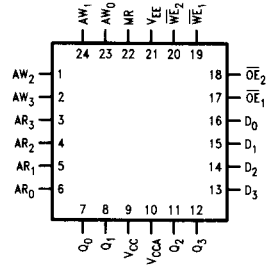
Top View

Order Number 100145DC
See NS Package Number J24E*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

24-Pin Ceramic Flatpak



TL/D/9638–2

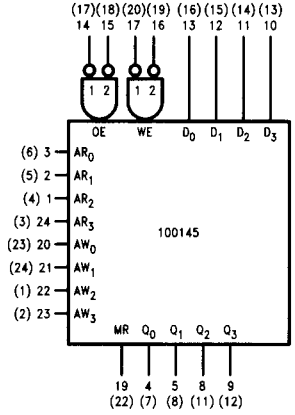
Top View

Order Number 100145FC
See NS Package Number W24B*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

Logic Symbol



TL/D/9638–3

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

AR_0–AR_3	Read Address Inputs
AW_0–AW_3	Write Address Inputs
$\overline{WE}_1$, $\overline{WE}_2$	Read Enable Inputs (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)
D_0–D_3	Data Inputs
MR	Master Reset Input
Q_0–Q_3	Data Outputs