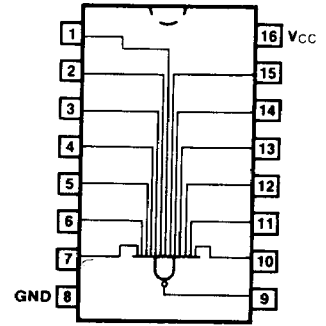


✓ **54S/74S133** 010125
 ✓ **54LS/74LS133** 010124
13-INPUT NAND GATE

CONNECTION DIAGRAM
 PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74S133PC, 74LS133PC		9B
Ceramic DIP (D)	A	74S133DC, 74LS133DC	54S133DM, 54LS133DM	6B
Flatpak (F)	A	74S133FC, 74LS133FC	54S133FM, 54LS133FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.)	54/74LS (U.L.)
	HIGH/LOW	HIGH/LOW
Inputs	1.25/1.25	0.5/0.25
Outputs	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max		V _{IN} = Gnd	V _{CC} = Max
I _{CC} H	Power Supply Current	5.0		0.5		mA		
I _{CC} L		10		1.1			V _{IN} = Open	
t _{PLH}	Propagation Delay	6.0		15		ns	Figs. 3-1, 3-4	
t _{PHL}		7.0		38				

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.