4703B/4703BX

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

FAIRCHILD CMOS MACROLOGIC™

DESCRIPTION — The 4703B/4703BX is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 4703B/4703BX has 3-state outputs which provide added versatility and is fully compatible with all CMOS families.

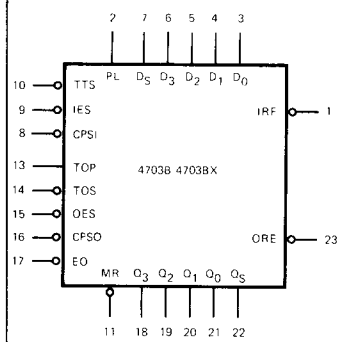
The 4703B is specified to operate over a power supply voltage range of 4.5 V to 12.5 V and the 4703BX is specified to operate over a power supply voltage range of 3 V to 15 V.

- **5.3 MHz SERIAL OR PARALLEL DATA RATE, TYPICALLY AT V_{DD} = 10 V**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL CMOS FAMILIES**
- **SLIM 24-PIN PACKAGE**

PIN NAMES

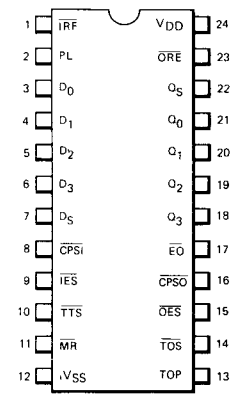
D_0–D_3	Parallel Data Inputs
D_S	Serial Data Input
$\overline{PL}$	Parallel Load Input
$\overline{CPSI}$	Serial Input Clock Input (HIGH-to-LOW Triggered)
$\overline{CPSO}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{IES}$	Serial Input Enable (Active LOW)
$\overline{TTS}$	Transfer to Stack Input (Active LOW)
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)
$\overline{TOP}$	Transfer Out Parallel Input
$\overline{OES}$	Serial Output Enable Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{IRF}$	Input Register Full Output (Active LOW)
$\overline{ORE}$	Output Register Empty Output (Active LOW)
Q_0–Q_3	Parallel Data Outputs
Q_S	Serial Data Output

LOGIC SYMBOL



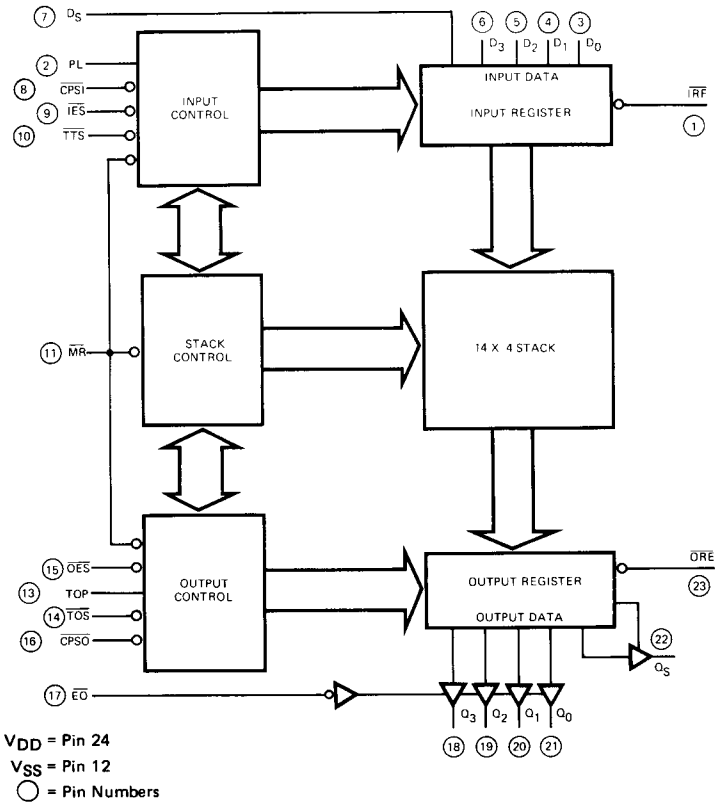
V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the block diagram the 4703B/4703BX consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section, as described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the D_0–D_3 inputs into the F_0–F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section). The D_0–D_3 inputs are "ones catching" and must remain stable while PL is HIGH.

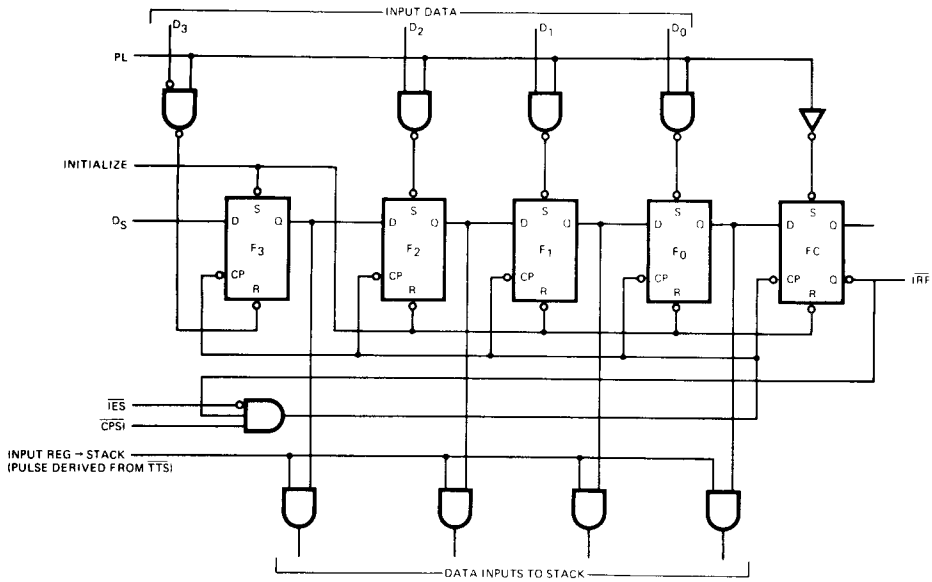


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry – Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the $\overline{CPSI}$ clock input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0–F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. *Figure 2* illustrates the final positions in a 4703B/4703BX resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack – The outputs of Flip-Flops F_0–F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 4703B/4703BX, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

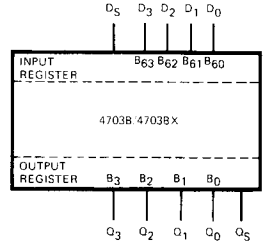


Fig. 2
FINAL POSITIONS IN A 4703B/4703BX RESULTING
FROM A 64-BIT SERIAL TRAIN

Output Register (Data Extraction) – The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

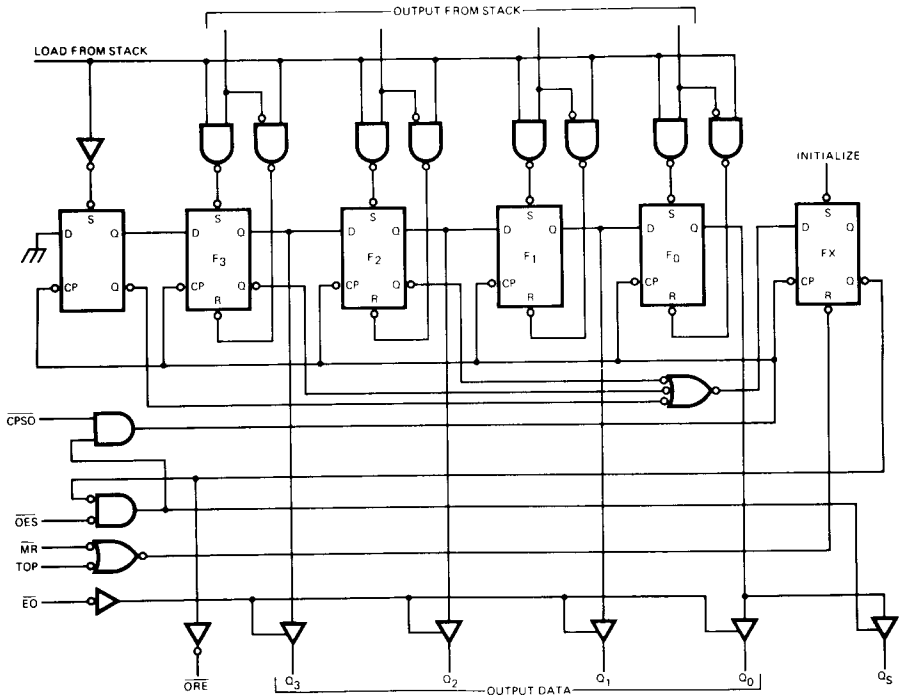


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{CPSO}$ should be LOW. $\overline{TOS}$ should be grounded for single slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{ORE}$ remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{TOS}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{ORE}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

EXPANSION

Vertical Expansion – The 4703B/4703BX may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in *Figure 4*. Using the same technique, any FIFO of (15n + 1) words by four bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 4703B/4703BX's flexibility for serial/parallel input and output. For other expansion schemes, refer to the Applications section of this book.

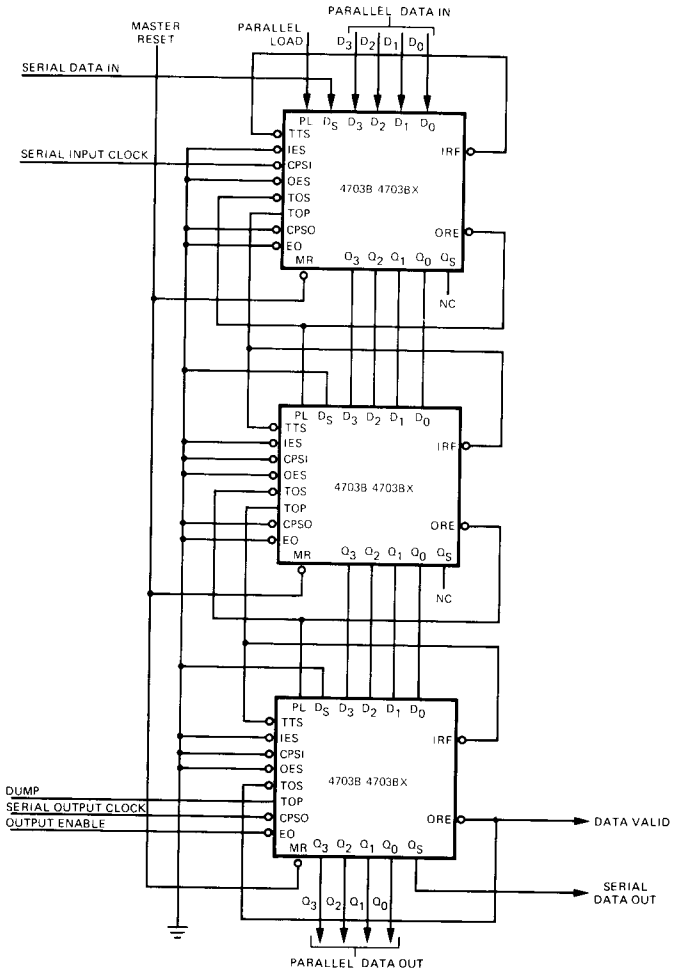


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 4703B/4703BX can also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in *Figure 5*. Using the same technique, any FIFO of 16 words by 4n bits can be constructed, where n is the number of devices. The $\overline{IRF}$ output of the right most device (most significant device) is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 4703B/4703BX's flexibility for serial/parallel input and output.

It should be noted that this form of horizontal expansion extracts a penalty in speed. A single FIFO is guaranteed to operate at 3.4 MHz; an array of four FIFOs connected in the above manner is guaranteed at 1.5 MHz. An expansion scheme that provides higher speed but requires additional components is shown in the Applications section of this book.

Horizontal and Vertical Expansion – The 4703B/4703BX can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 6*. Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

Figures 7 and *8* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 6*. The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 6* is shown in *Figure 9*.

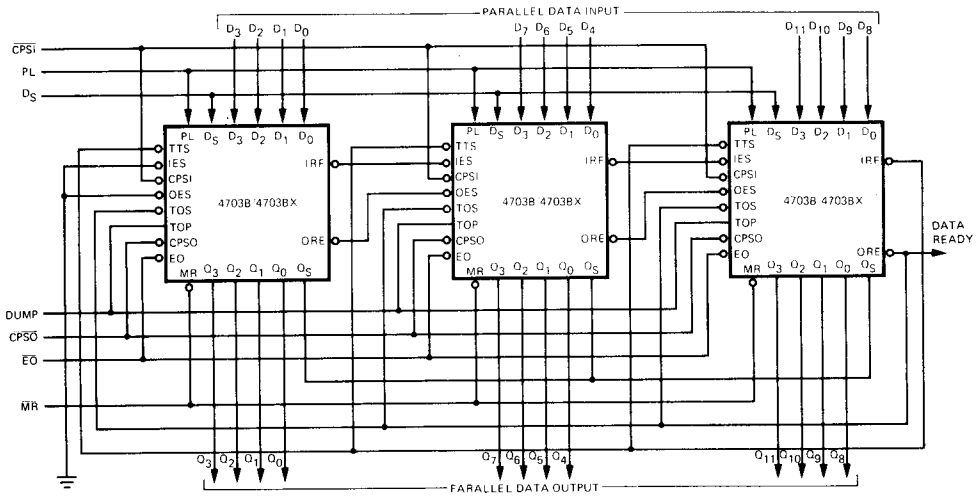


Fig. 5
A HORIZONTAL EXPANSION SCHEME

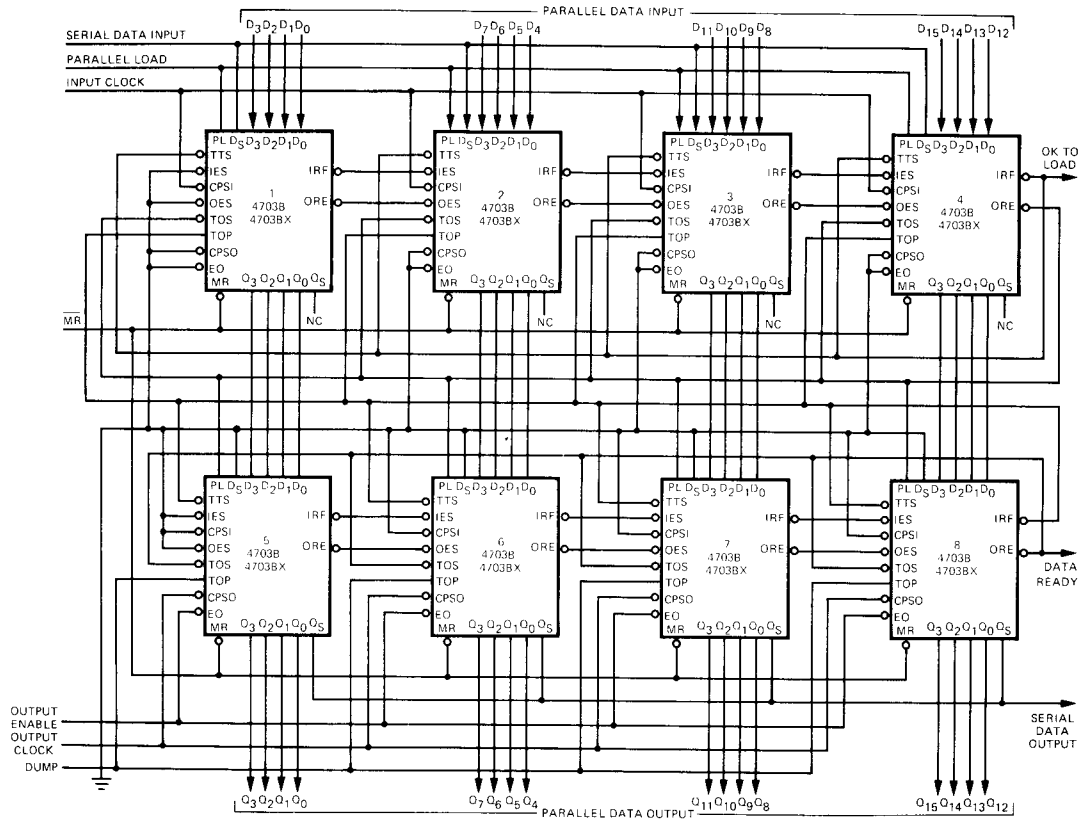


Fig. 6
A 31 X 16 FIFO ARRAY

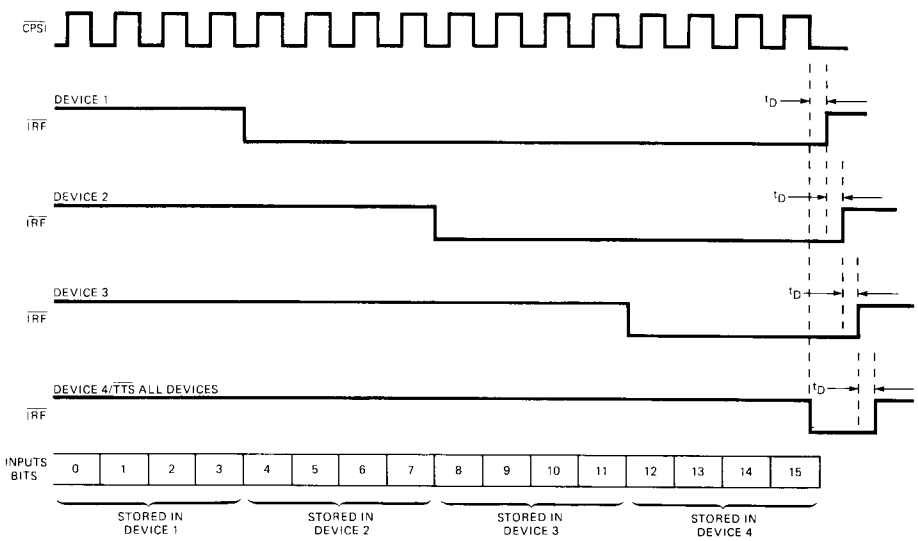


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

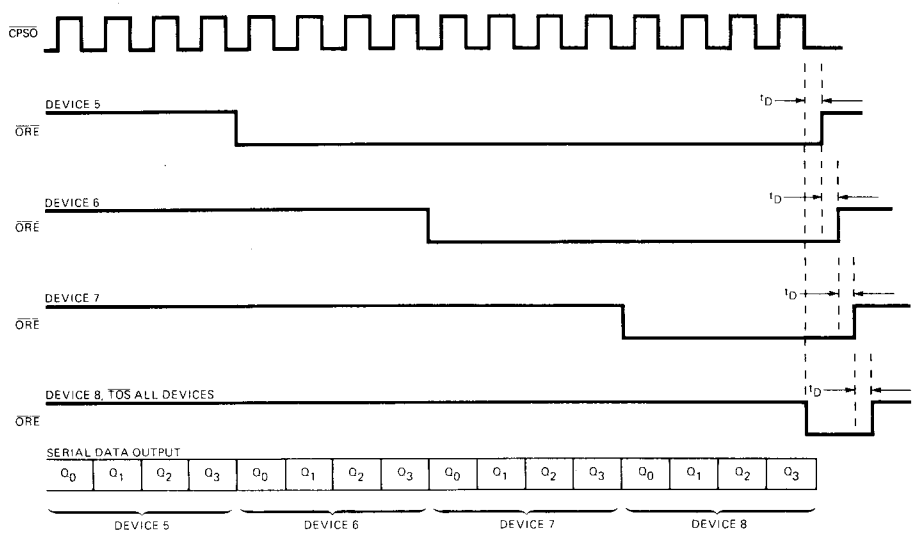


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

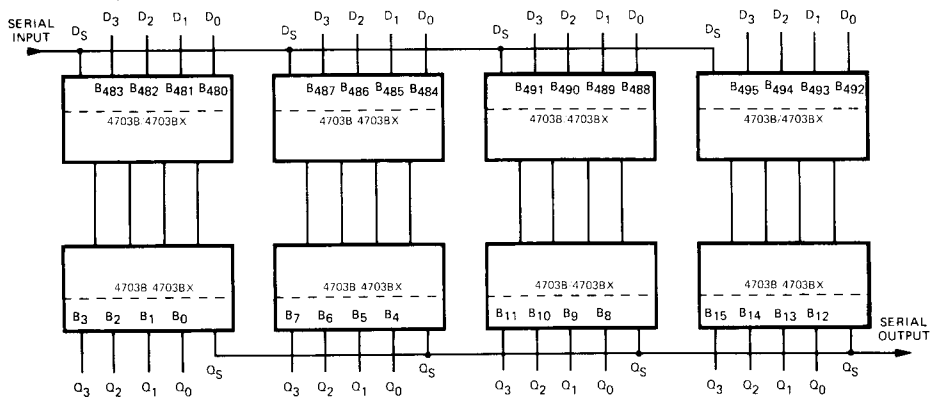


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry – Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 4703B/4703BX incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 4703B/4703BX array of *Figure 6* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row, master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 4703B/4703BX FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 10* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

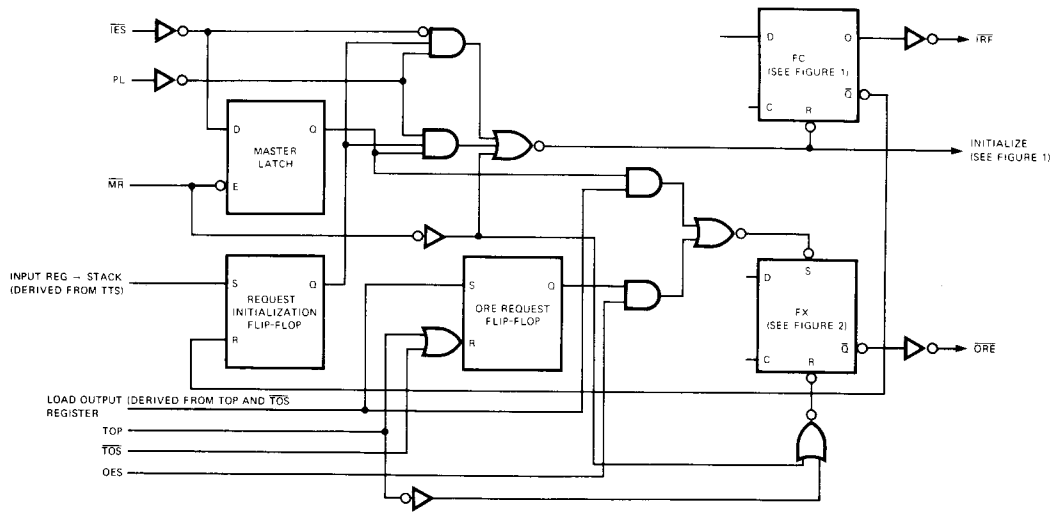


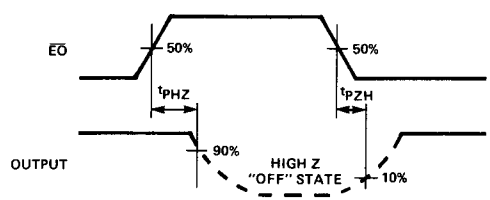
Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

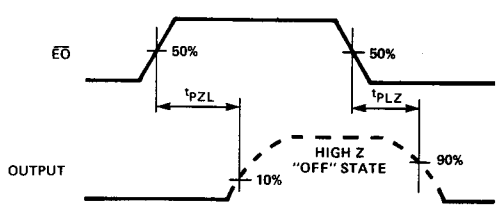
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay, $\overline{CPSO}$ to $\overline{ORE}$		159	318		74	148		52	104	ns	
t_{PLH}	Propagation Delay, $\overline{TOS}$ to $\overline{ORE}$		320	640		114	228		80	160	ns	
t_{PLH}	Propagation Delay,		401	802		134	268		94	188	ns	C_L = 50 pF,
t_{PHL}	TOP to $\overline{ORE}$		256	512		109	218		77	154		R_L = 200 kΩ
t_{PHL}	Propagation Delay, PL to $\overline{IRF}$		119	238		44	88		31	62	ns	Input Transition
t_{FT}	Fall Through Time		2020	4040		820	1640		574	1148	ns	Times ≤ 20 ns
t_{PZH}	Output Enable Time		51	102		24	48		17	34	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			85	170		33	66		24	48		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		64	128		34	68		24	48	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			80	160		39	78		28	56		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		46	92		25	50		18	36	ns	
t_{THL}			34	68		18	36		13	26		
$t_W\overline{CP}(H)$	Min $\overline{CPSI}$ Pulse Width (HIGH)	118	59		44	22		31	16		ns	
$t_W\overline{CP}(L)$	Min $\overline{CPSI}$ Pulse Width (LOW)	220	110		108	54		76	38		ns	
$t_W\overline{CP}(L)$	Min $\overline{CPSO}$ Pulse Width (LOW)	120	60		60	30		42	21		ns	
$t_W\overline{CP}(H)$	Min $\overline{CPSO}$ Pulse Width (HIGH)	110	55		72	36		51	26		ns	
t_WPL(H)	Min PL Pulse Width (HIGH)	122	61		44	22		31	16		ns	
$t_W\overline{TTS}(L)$	Min $\overline{TTS}$ Pulse Width (LOW)	160	80		124	62		87	44		ns	
$t_W\overline{TOS}(L)$	Min $\overline{TOS}$ Pulse Width (LOW)	182	91		60	30		42	21		ns	
t_WTOP(L)	Min TOP Pulse Width (LOW)	142	71		52	26		37	19		ns	
$t_W\overline{MR}(L)$	Min $\overline{MR}$ Pulse Width (LOW)	192	96		108	54		76	38		ns	
t_{rec}	$\overline{MR}$ Recovery Time	44	22		36	18		26	13		ns	
t_s	Set-Up and Hold Times,	104	52		40	20		28	14		ns	
t_h	D_S to $\overline{CPSI}$	−8	−15		24	12		18	9			
t_s	Set-Up and Hold Times, $\overline{TTS}$ to	186	93		98	49		70	35		ns	
t_h	$\overline{IRF}$, Serial or Parallel Mode	76	38		52	26		38	19			
t_s	Set-Up Time, $\overline{ORE}$ to $\overline{TOS}$	−151	−302		−21	−42		−15	−30		ns	
f_{MAX}	Input CLOCK Frequency (Note 2)	1.1	2.3		2.6	5.3		3.4	6.9		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



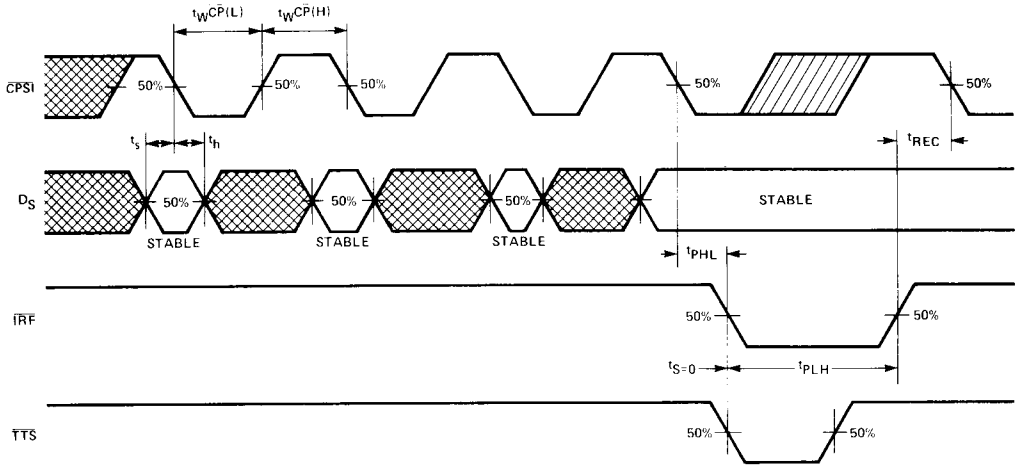
OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

SWITCHING WAVEFORMS (Cont'd)

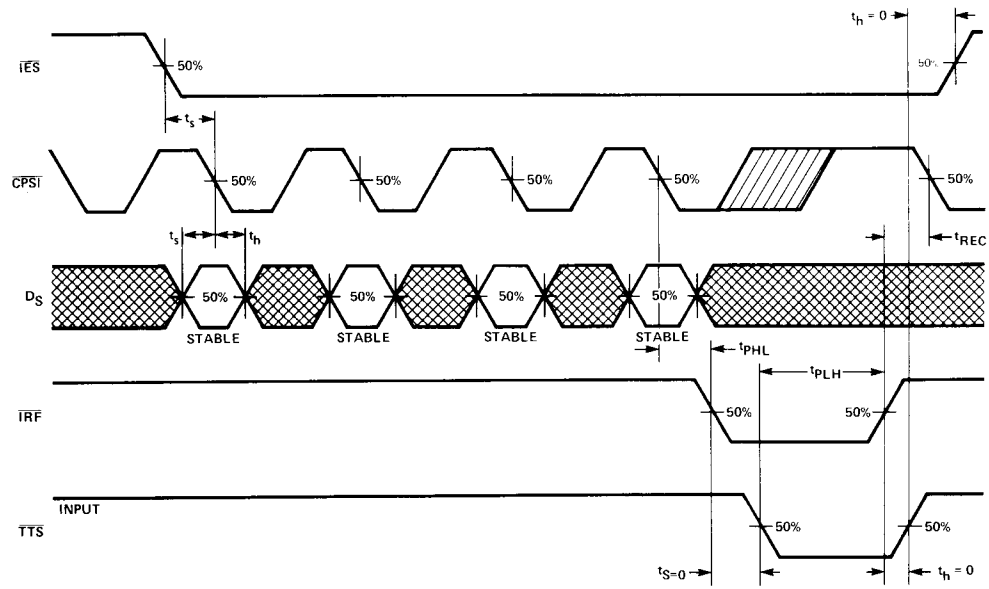
SERIAL INPUT UNEXPANDED OR MASTER OPERATION



MINIMUM $\overline{CPSI}$ PULSE WIDTH, PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$, AND SET-UP AND HOLD TIMES, D_S TO $\overline{CPSI}$, AND $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$, = PL = LOW

SERIAL INPUT EXPANDED SLAVE OPERATION



PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$ AND SET-UP AND HOLD TIMES, $\overline{IES}$ TO $\overline{CPSI}$, D_S TO $\overline{CPSI}$ AND $\overline{TTS}$ TO $\overline{IRF}$.

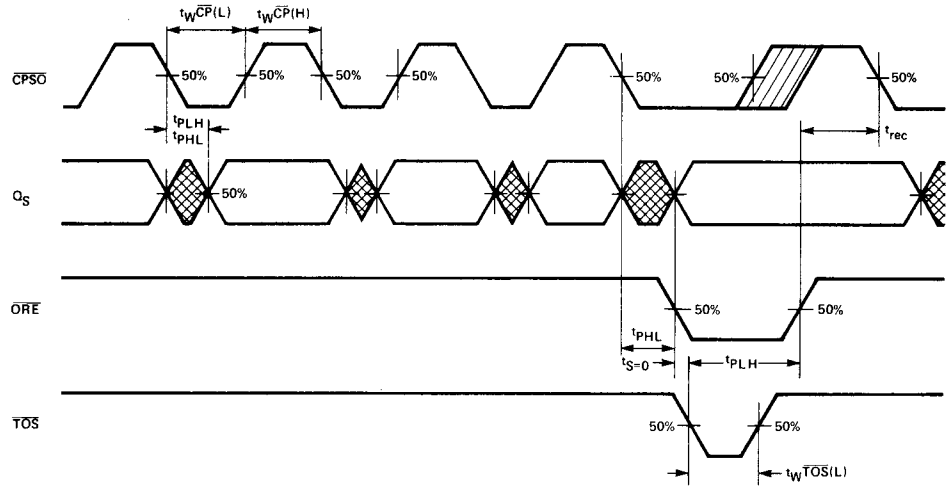
CONDITIONS: STACK NOT FULL $\overline{IES}$ = HIGH
WHEN INITIALIZED, PL = LOW

NOTE:
Set-up and hold times are shown as positive values but may be specified as negative values.

7

SWITCHING WAVEFORMS (Cont'd)

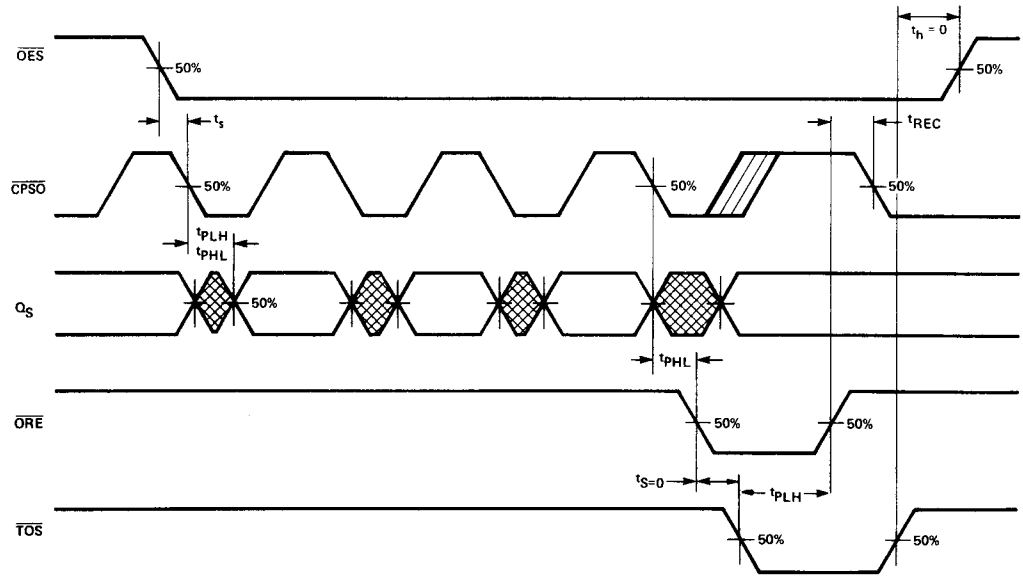
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION



$\overline{ORE}$ RECOVERY TIME, PROPAGATION DELAY $\overline{CPSO}$ TO QS, $\overline{CPSO}$ TO $\overline{ORE}$, $\overline{TOS}$ TO $\overline{ORE}$, MINIMUM $\overline{CPSO}$ PULSE WIDTH, MINIMUM $\overline{TOS}$ PULSE WIDTH AND SET-UP TIME $\overline{ORE}$ TO $\overline{TOS}$.

CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{IES}$ = LOW
WHEN INITIALIZED, $\overline{OES}$ = LOW

SERIAL OUTPUT, SLAVE OPERATION



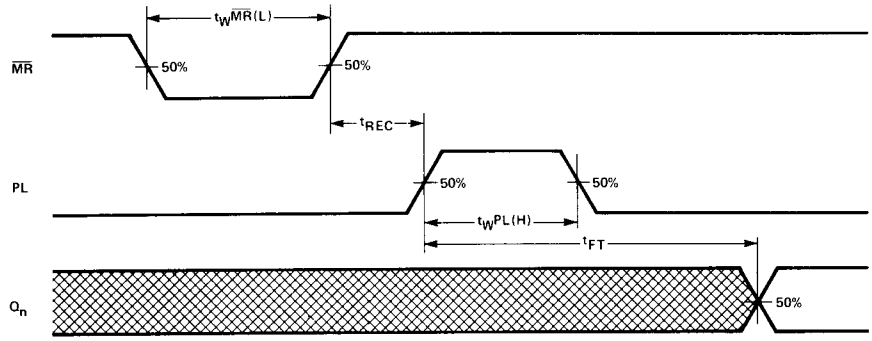
$\overline{ORE}$ RECOVERY TIME, PROPAGATION DELAY $\overline{CPSO}$ TO Q_S, $\overline{CPSO}$ TO $\overline{ORE}$, $\overline{TOS}$ TO $\overline{ORE}$, AND SET-UP AND HOLD TIMES, $\overline{OES}$ TO $\overline{CPSO}$, $\overline{ORE}$ TO $\overline{TOS}$, $\overline{TOS}$ TO $\overline{OES}$

CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{IES}$ = HIGH
WHEN INITIALIZED

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS (Cont'd)

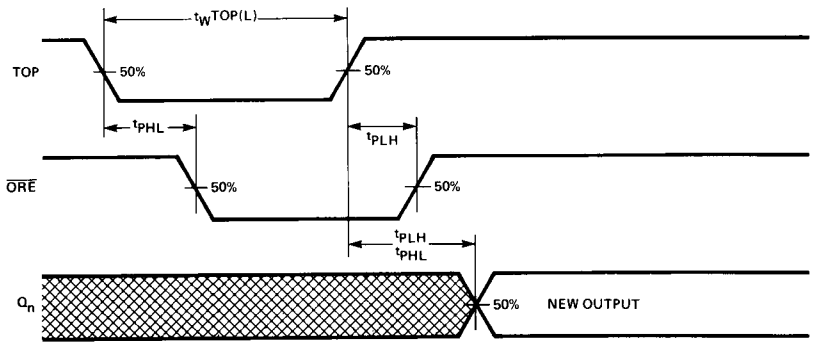
FALL THROUGH TIME



MINIMUM $\overline{MR}$ AND PL PULSE WIDTHS, RECOVERY TIME FOR $\overline{MR}$ AND FALL THROUGH TIME

CONDITIONS: $\overline{TTS}$ CONNECTED TO $\overline{IRF}$, $\overline{TOS}$ CONNECTED TO $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ = LOW. TOP = HIGH

PARALLEL OUTPUT, FOUR BIT WORD OR MASTER IN PARALLEL EXPANSION



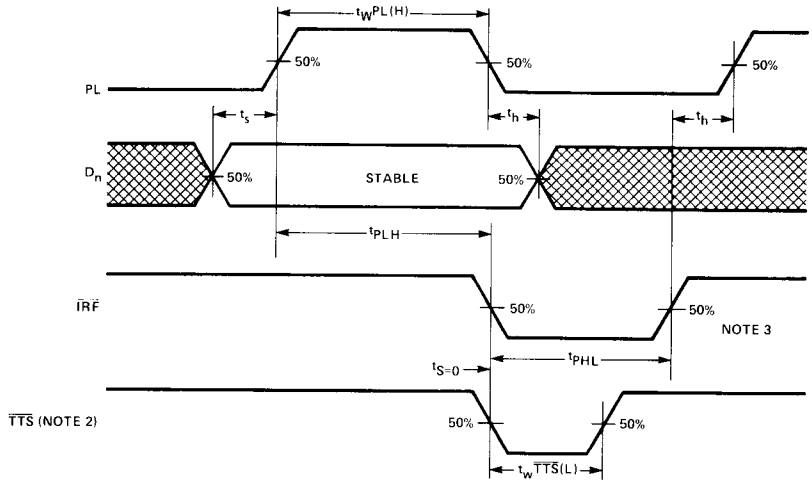
PROPAGATION DELAY, TOP TO $\overline{ORE}$, TOP TO Q_n, AND MINIMUM TOP PULSE WIDTH

CONDITIONS: $\overline{IES}$ = LOW WHEN INITIALIZED, $\overline{EO}$ = $\overline{CPSO}$ = LOW. DATA AVAILABLE IN STACK

7

SWITCHING WAVEFORMS (Cont'd)

PARALLEL LOAD MODE, FOUR BIT WORD (UNEXPANDED)
OR MASTER IN PARALLEL EXPANSION

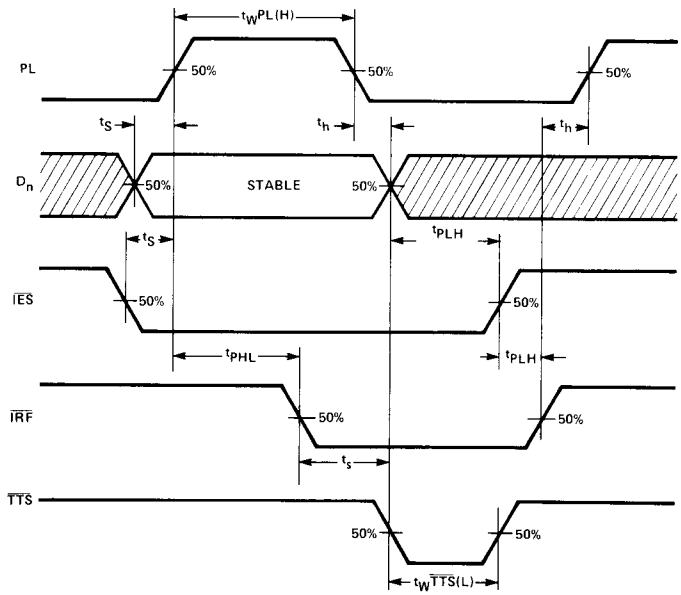


PROPAGATION DELAY PL TO $\overline{IRF}$, $\overline{TTS}$ TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES D_n TO PL, $\overline{IRF}$ TO PL, $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$ = LOW
WHEN INITIALIZED

NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, $\overline{IRF}$ will stay LOW.

PARALLEL LOAD, SLAVE MODE



PROPAGATION DELAY, $\overline{TTS}$ TO $\overline{IES}$, $\overline{IES}$ TO $\overline{IRF}$, PL TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES, D_n TO PL, $\overline{IRF}$ TO $\overline{TTS}$, $\overline{IRF}$ TO PL

CONDITIONS: STACK NOT FULL, DEVICE INITIALIZED
WITH $\overline{IES}$ HIGH

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF HIGH Current	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF LOW Current	XC									−1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
											−12		MAX	
		XM									−0.4		MIN, 25°C	
											−12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35	μA	MIN, 25°C	
					250			500			1000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PHL}	Propagation Delay, $\overline{CPSI}$ to $\overline{IRF}$		215	430		81	162		57	114	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times < 20 ns
t_{PLH}	Propagation Delay, $\overline{TTS}$ to $\overline{IRF}$		439	878		131	262		92	184	ns	
t_{PLH}	Propagation Delay, $\overline{CPSO}$ to Q_S		306	612		68	136		48	96	ns	
t_{PHL}			299	598		79	158		56	112		
t_{PLH}	Propagation Delay, TOP to Q_n		325	650		128	256		90	180	ns	
t_{PHL}			293	586		114	228		80	160		

Notes on following page.

7