BURR-BROWN®

AD515

FET-Input Electrometer OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 0.075pA max
- LOW POWER: 1.5mA max
- LOW OFFSET: 1mV max
- LOW DRIFT: 15μV/°C max
- LOW COST
- REPLACES ANALOG DEVICES AD515

APPLICATIONS

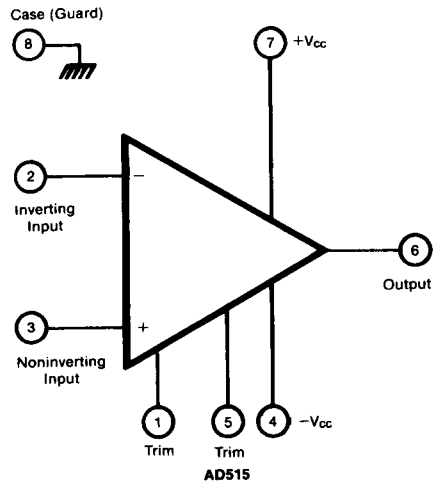
- pH SENSORS
- INTEGRATORS
- TEST EQUIPMENT
- ELECTRO-OPTICS
- CHARGE AMPLIFIERS
- GAS DETECTORS

DESCRIPTION

The Burr-Brown AD515 is a monolithic pin-for-pin replacement for the hybrid Analog Devices AD515 ultra-low bias current operational amplifier.

Laser-trimmed offset voltage and very-low bias current are important features of this popular amplifier. Monolithic construction allows lower cost and higher reliability than hybrid designs.

The AD515 is available in three electrical grades; all are specified over 0°C to +70°C and supplied in a TO-99 hermetic package.



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PDS-654A

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	AD515J			AD515K			AD515L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain[1]	$R_L \geq 2k\Omega$	20k			40k			25k			V/V
	$R_L \geq 10k\Omega$	40k			100k			50k			V/V
	T_{MIN} to T_{MAX}, R_L = 2k	15k			40k			25k			V/V
RATED OUTPUT											
Voltage Output: R_L = 2kΩ	T_{MIN} to T_{MAX}	±10	±12		*	*		*	*		V
R_L = 10kΩ	T_{MIN} to T_{MAX}	±12	±13		*	*		*	*		V
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		10	25	50	*	*	*	*	*	*	mA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			350			*			*		kHz
Full Power Response	20V p-p, R_L = 2k	5	16		*	*		*	*		kHz
Slew Rate	V_O = ±10V, R_L = 2k, Gain = −1	0.3	1.0		*	*		*	*		V/μs
Overload Recovery	Gain = −1		16	100		*	*		*	*	μs
INPUT											
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		0.4	3.0		*	1.0		*	1.0	mV
Average Drift	T_{MIN} to T_{MAX}			50			15			25	μV/°C
Supply Rejection	T_{MIN} to T_{MAX}	68	86		80			74			dB
			50	400			100			200	μV/V
BIAS CURRENT[2]											
Input Bias Current Either Input	V_{CM} = 0VDC			300			150			75	fA
IMPEDANCE											
Differential			10^{13} ‖ 1.6			*			*		Ω ‖ pF
Common-Mode			10^{15} ‖ 0.8			*			*		Ω ‖ pF
VOLTAGE RANGE[3]											
Differential Input Range		±20			*			*			V
Common-Mode Input Range		±10	±11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	66	94		80			70			dB
NOISE											
Voltage: 0.1Hz to 10Hz			4.0			*			*		μV p-p
f_O = 10Hz			75			*			*		$nV/\sqrt{Hz}$
f_O = 100Hz			55			*			*		$nV/\sqrt{Hz}$
f_O = 1kHz			50			*			*		$nV/\sqrt{Hz}$
Current: 0.1Hz to 10Hz			0.003			*			*		pA p-p
f_O = 10Hz to 10kHz			0.01			*			*		pA rms
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		0.8	1.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification Range	Ambient temp.	0		+70	*		*	*		*	°C
Storage	Ambient temp.	−65		+150	*		*	*		*	°C

* Specification same as AD515J.

NOTES: (1) With or without nulling of V_{OS}. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 200°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

AD515 X H

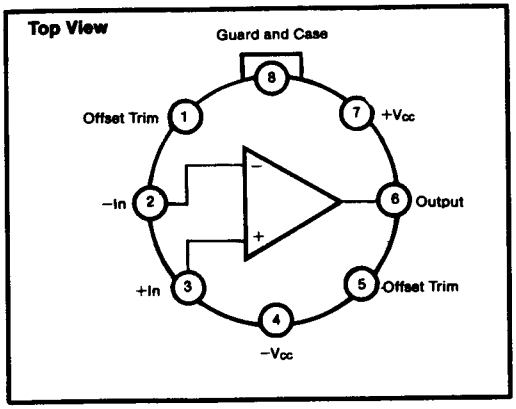
Basic model number

Performance grade
J, K, L = 0°C to +70°C

Package code
H = TO-99 metal can

CONNECTION DIAGRAM

Top View

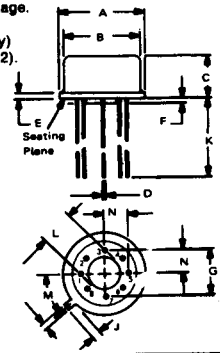


MECHANICAL

"H" PACKAGE TO-99 (Hermetic)

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

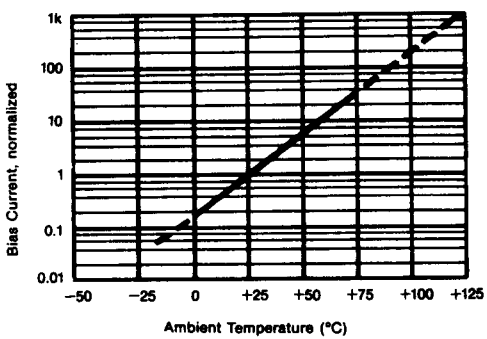
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



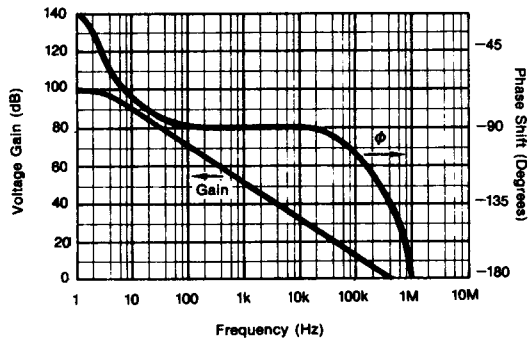
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

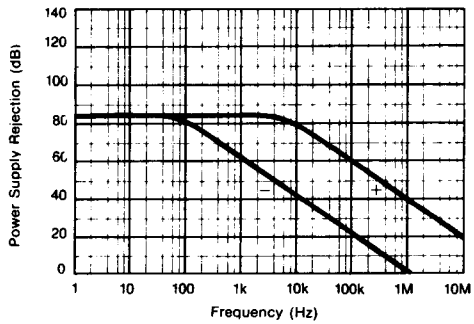
NORMALIZED BIAS CURRENT vs TEMPERATURE



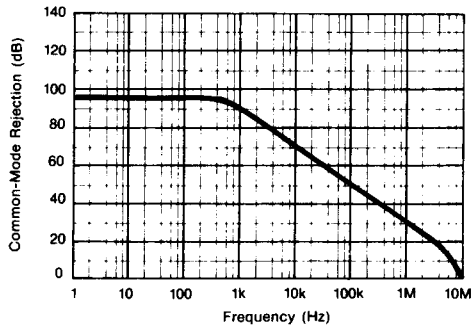
OPEN-LOOP FREQUENCY RESPONSE



POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

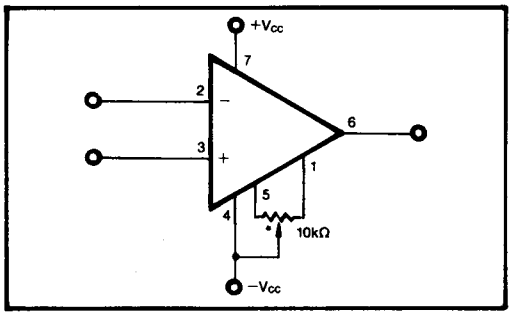


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

The AD515 requires input protection only if the source is not current limited. Limiting input current to 0.5mA with a series resistor is recommended when input voltage exceeds supply voltage.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the AD515. To avoid leakage problems, it is recommended that the signal input lead of the AD515 be wired to a Teflon standoff. If the lead is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential. The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

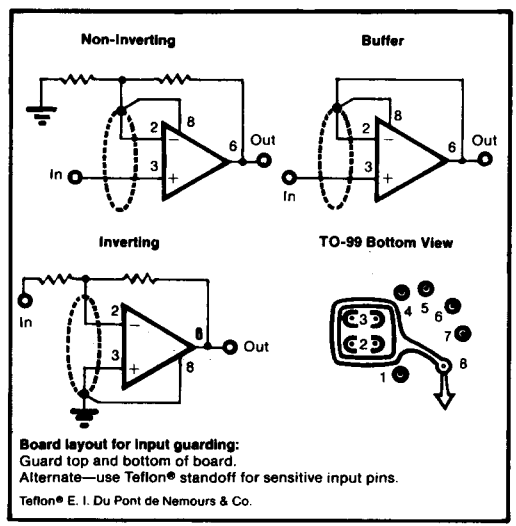


FIGURE 2. Connection of Input Guard.