National Semiconductor

CLC440
High-Speed, Low-Power, Voltage Feedback Op Amp

General Description

The CLC440 is a wideband, low-power, voltage feedback op amp that offers 750MHz unity-gain bandwidth, 1500V/µs slew rate, and 90mA output current. For video applications, the CLC440 sets new standards for voltage feedback monolithics by offering the impressive combination of 0.015% differential gain and 0.025° differential phase errors while dissipating a mere 70mW.

The CLC440 incorporates the proven properties of Comlinear's current feedback amplifiers (high bandwidth, fast slewing, etc.) into a "classical" voltage feedback architecture. This amplifier possesses truly differential and fully symmetrical inputs both having a high 900kΩ impedance with matched low input bias currents. Furthermore, since the CLC440 incorporates voltage feedback, a specific R_f is not required for stability. This flexibility in choosing R_f allows for numerous applications in wideband filtering and integration.

Unlike several other high-speed voltage feedback op amps, the CLC440 operates with a wide range of dual or single supplies allowing for use in a multitude of applications with limited supply availability. The CLC440's low 3.5nV/√Hz(e_n) and 2.5pA/√Hz(i_n) noise sets a very low noise floor.

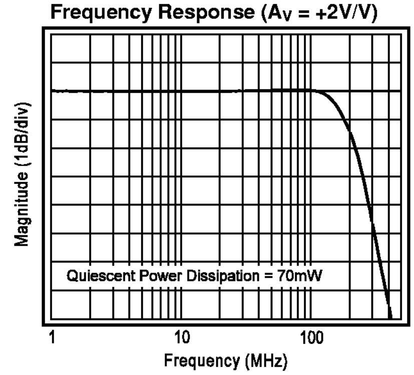
Features

- Unity-gain stable
- High unity-gain bandwidth: 750MHz
- Ultra-low differential gain: 0.015%
- Very low differential phase: 0.025°
- Low power: 70mW
- Extremely fast slew rate: 1500V/µs
- High output current: 90mA
- Low noise: 3.5nV/√Hz
- Dual ±2.5V to ±6V or single 5V to 12V supplies

Applications

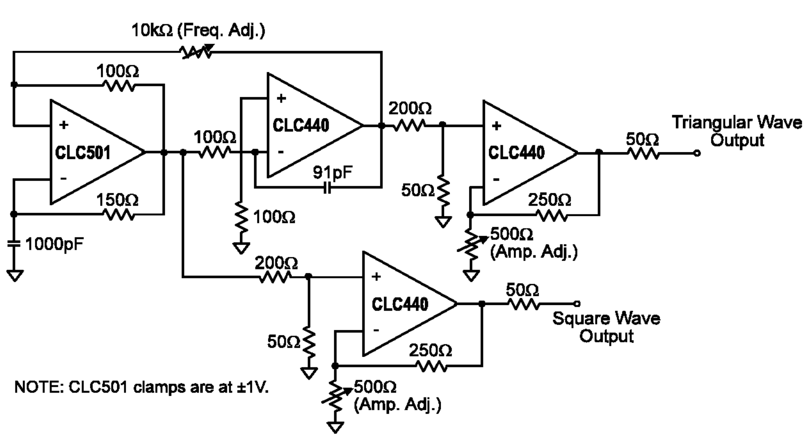
- Professional video
- Graphics workstations
- Test equipment
- Video switching & routing
- Communications
- Medical imaging
- A/D drivers
- Photo diode transimpedance amplifiers
- Improved replacement for CLC420 or OPA620

Frequency Response (A_V = +2V/V)

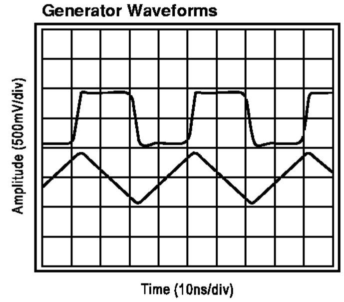


Typical Application

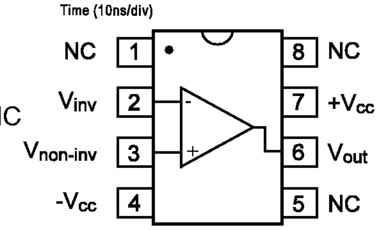
10MHz to 40MHz Square and Triangular Wave Generator



Generator Waveforms



Pinout
DIP & SOIC



CLC440 Electrical Characteristics (A_V = +2, R_f = R_g = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC440	+25˚C	+25˚C	0 to 70˚C	-40 to 85˚C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth A_V =+2	V_{out} < 0.2V_{pp}	260	165	165	135	MHz	
	V_{out} < 4.0V_{pp}	190	150	135	130	MHz	
-3dB bandwidth A_V =+1	V_{out} < 0.2V_{pp}	750				MHz	
gain bandwidth product	V_{out} < 0.2V_{pp}	230				MHz	
gain flatness	V_{out} < 2.0V_{pp} DC to 75MHz	0.05	0.15	0.20	0.20	dB	
linear phase deviation	V_{out} < 2.0V_{pp} DC to 75MHz	0.8	1.2	1.5	1.5	deg	
differential gain	4.43MHz, R_L=150Ω	0.015	0.03	0.04	0.04	%	
differential phase	4.43MHz, R_L=150Ω	0.025	0.05	0.06	0.06	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	1.5	2.0	2.2	2.5	ns	
	4V step	3.2	4.2	4.5	5.0	ns	
settling time to 0.05%	2V step	10	14	16	16	ns	
overshoot	4V step	7	13	13	13	%	
slew rate	4V step, ±0.5V crossing	1500	900	750	600	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 5MHz	-64	-59	-59	-59	dBc	
	2V_{pp}, 20MHz	-52	-46	-46	-46	dBc	
3rd harmonic distortion	2V_{pp}, 5MHz	-70	-65	-64	-64	dBc	
	2V_{pp}, 20MHz	-51	-45	-43	-43	dBc	
equivalent input noise							
voltage	>1MHz	3.5	4.5	5.0	5.0	nV/√Hz	
current	>1MHz	2.5	3.5	4.0	4.0	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1.0	3.0	3.5	4.0	mV	A
average drift		5.0		10	10	µV/°C	
input bias current		10	30	35	40	µA	A
average drift		30		50	60	nA/°C	
input offset current		0.5	2.0	2.0	3.0	µA	A
average drift		3.0		10	10	nA/°C	
power supply rejection ratio	DC	65	58	58	58	dB	
common-mode rejection ratio	DC	80	65	60	60	dB	
supply current	R_L= ∞	7.0	7.5	8.0	8.0	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	900	500	400	300	kΩ	
input capacitance	common-mode	1.2	2.0	2.0	2.0	pF	
	differential-mode	0.5	1.0	1.0	1.0	pF	
input voltage range	common-mode	±3.0	±2.8	±2.7	±2.7	V	
output voltage range	R_L= 100Ω	±2.5	±2.3	±2.2	±2.2	V	
output voltage range	R_L= ∞	±3.0	±2.8	±2.7	±2.7	V	
output current		±90	±80	±65	±45	mA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

voltage supply	±6V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175˚C
storage temperature range	-65˚C to +150˚C
lead temperature (soldering 10 sec)	+300˚C
ESD rating (human bodey model)	<1000V

Package Thermal Resistance

Package	θ_{jc}	θ_{ja}
Plastic (AJP)	70˚/W	125˚/W
Surface Mount (AJE)	60˚/W	140˚/W
CerDip	40˚/W	130˚/W

Ordering Information

Model	Temperature Range	Description
CLC440AJP	-40°C to +85°C	8-pin PDIP
CLC440AJE	-40°C to +85°C	8-pin SOIC
CLC440A8B	-55°C to +125°C	8-pin hermetic CerDIP, MIL-STD-883

Contact factory for SMD number.

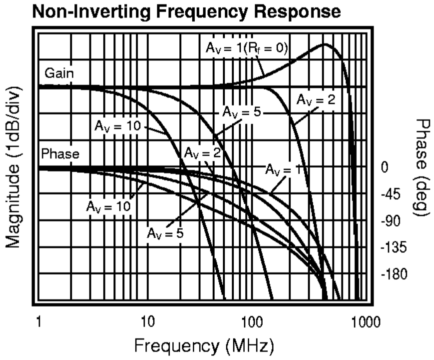
Notes

A) J-level: spec is 100% tested at +25˚C.

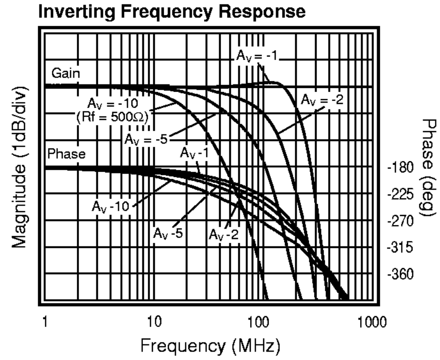
Transitor Count 46

CLC440 Typical Performance Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

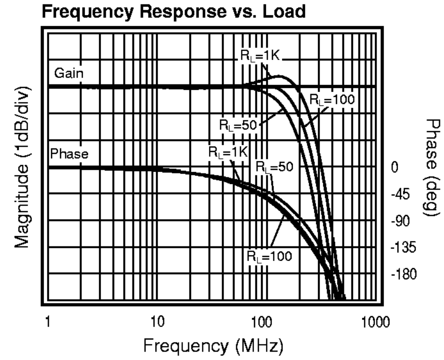
Non-Inverting Frequency Response



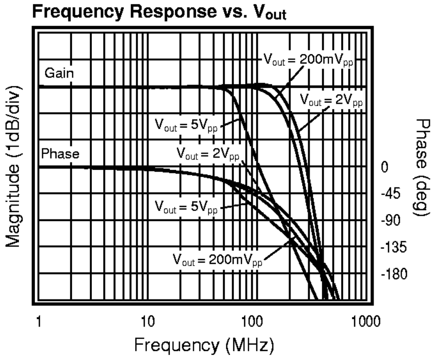
Inverting Frequency Response



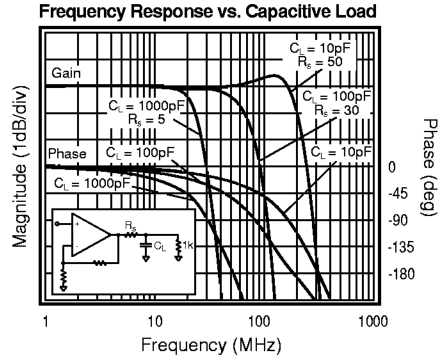
Frequency Response vs. Load



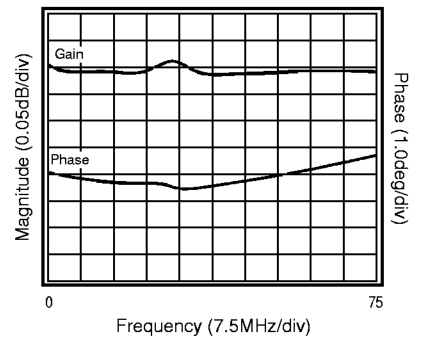
Frequency Response vs. V_{out}



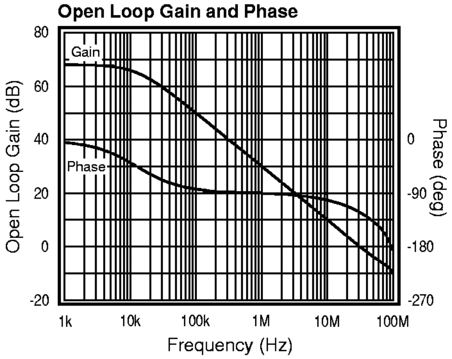
Frequency Response vs. Capacitive Load



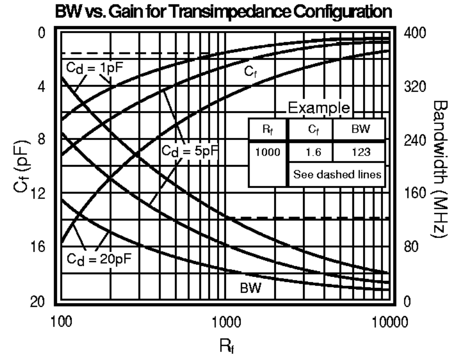
Gain Flatness and Linear Phase



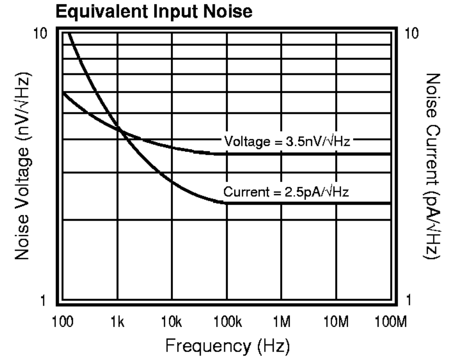
Open Loop Gain and Phase



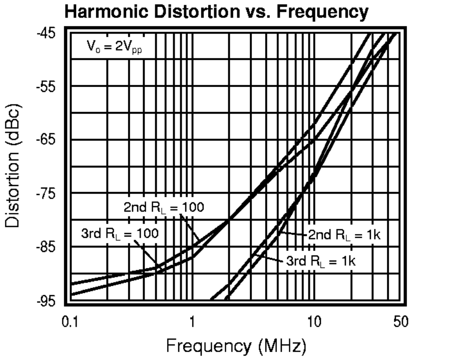
BW vs. Gain for Transimpedance Configuration



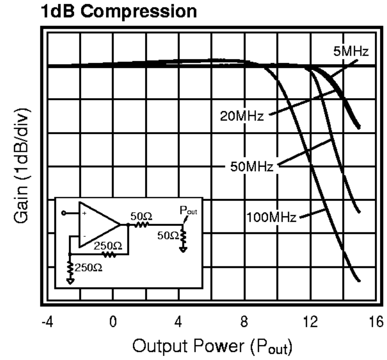
Equivalent Input Noise



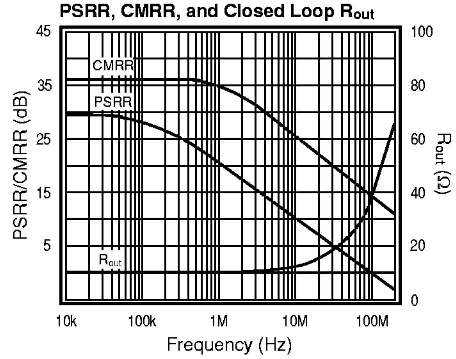
Harmonic Distortion vs. Frequency



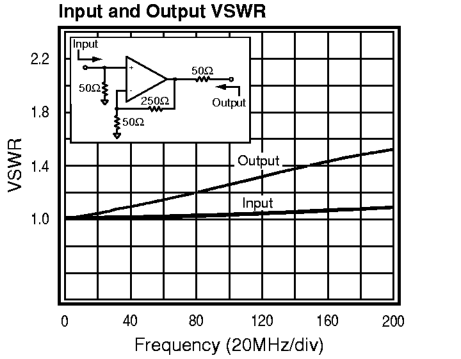
1dB Compression



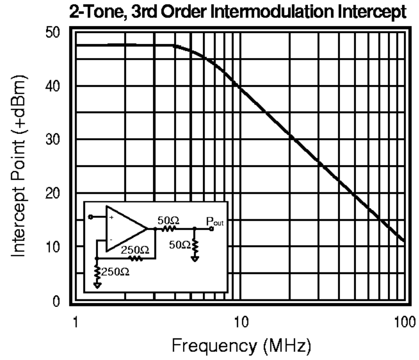
PSRR, CMRR, and Closed Loop R_{out}



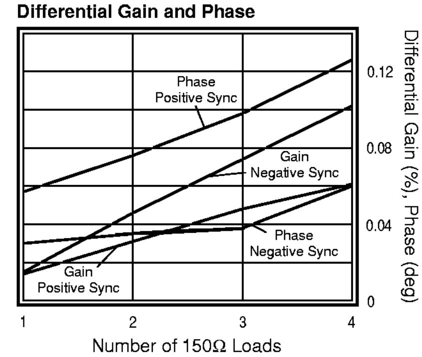
Input and Output VSWR



2-Tone, 3rd Order Intermodulation Intercept

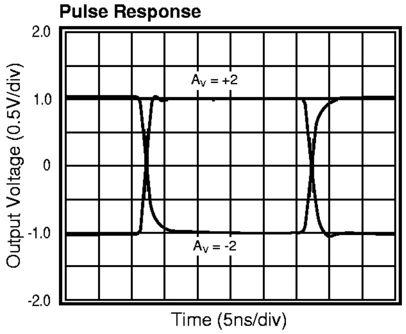


Differential Gain and Phase

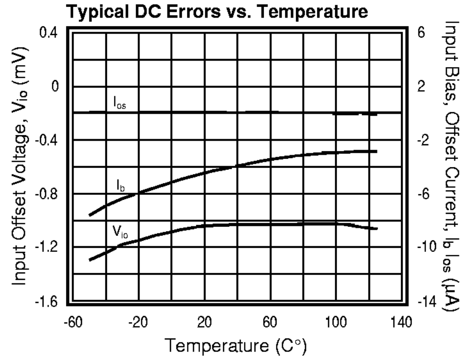


CLC440 Typical Performance Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

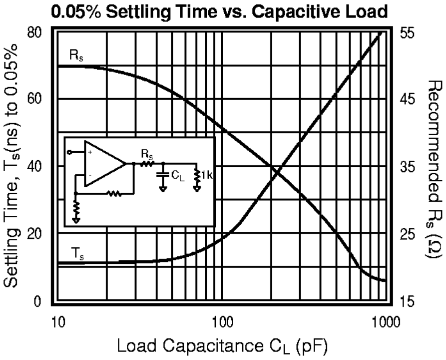
Pulse Response



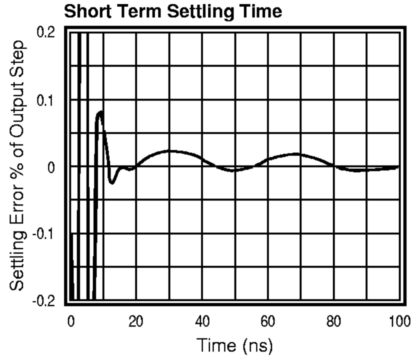
Typical DC Errors vs. Temperature



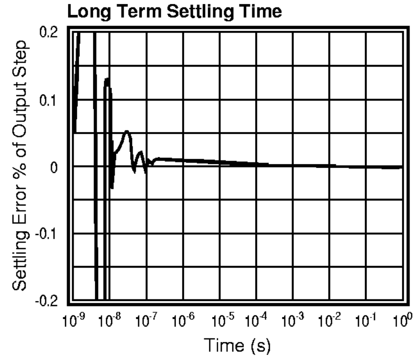
0.05% Settling Time vs. Capacitive Load



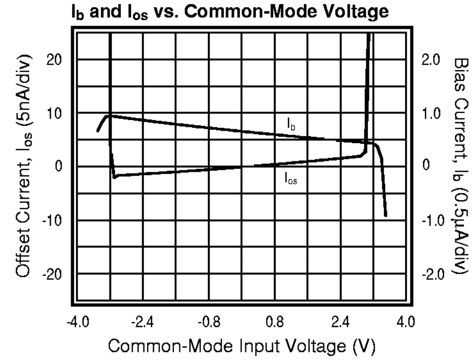
Short Term Settling Time



Long Term Settling Time



I_b and I_{os} vs. Common-Mode Voltage



APPLICATION INFORMATION

General Design Equations

The CLC440 is a unity gain stable voltage feedback amplifier. The matched input bias currents track well over temperature. This allows the DC offset to be minimized by matching the impedance seen by both inputs.

Gain

The non-inverting and inverting gain equations for the CLC440 are as follows:

$$\text{Non-inverting Gain: } 1+\frac{R_f}{R_g}$$

$$\text{Inverting Gain: } -\frac{R_f}{R_g}$$

Gain Bandwidth Product

The CLC440 is a voltage feedback amplifier, whose closed-loop bandwidth is approximately equal to the gain-bandwidth product (GBP) divided by the gain (Av). For gains greater than 5, Av sets the closed-loop bandwidth of the CLC440.

$$\text{Closed Loop Bandwidth} = \frac{GBP}{A_v}$$

$$A_v = \frac{(R_f + R_g)}{R_g}$$

GBP = 230MHz

For gains less than 5, refer to the frequency response plots to determine maximum bandwidth.

Output Drive and Settling Time Performance

The CLC440 has large output current capability. The 90mA of output current makes the CLC440 an excellent choice for applications such as:

- Video Line Drivers
- Distribution Amplifiers

When driving a capacitive load or coaxial cable, include a series resistance R_S to back match or improve settling time. Refer to the “Settling Time vs. Capacitive Load” plot in the typical performance section to determine the recommended resistance for various capacitive loads.

When driving resistive loads of under 500Ω, settling time performance diminishes. This degradation occurs because a small change in voltage on the output causes a large change of current in the power supplies. This current creates ringing on the power supplies. A small resistor will dampen this effect if placed in series with the 6.8μF bypass capacitor.

Noise Figure

Noise Figure (NF) is a measure of noise degradation caused by an amplifier.

$$NF = 10LOG\left(\frac{S_i/N_i}{S_o/N_o}\right) = 10LOG\left(\frac{e_{ni}^2}{e_t^2}\right)$$

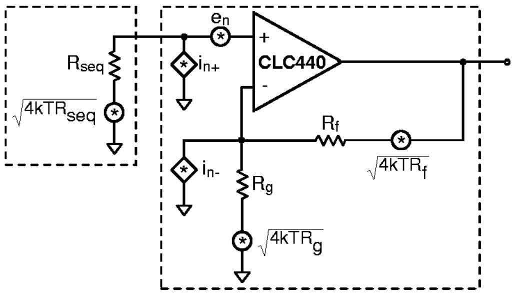
where,

e_{ni} = Total Equivalent Input Noise Density Due to the Amplifier

e_t = Thermal Voltage Noise ($\sqrt{4kTR_{seq}}$)

Figure 1 shows the noise model for the non-inverting amplifier configuration. The model includes all of the following noise sources:

- Input voltage noise (e_n)
- Input current noise ($i_n = i_{n+} = i_{n-}$)
- Thermal Voltage Noise (e_t) associated with each external resistor



$R_{seq} = R_s$ for Unterminated Systems
$R_{seq} = R_s \parallel R_T$ for Terminated Systems

Figure 1: Non-inverting Amplifier Noise Model

The total equivalent input noise density is calculated by using the noise model shown. Equations 1 and 2 represent the noise equation and the resulting equation for noise figure.

$$e_{ni} = \sqrt{e_n^2 + i_n^2\left(R_{seq}^2 + \left(R_f \parallel R_g\right)^2\right) + 4kTR_{seq} + 4kT\left(R_f \parallel R_g\right)}$$

Equation 1: Noise Equation

$$NF = 10LOG\left(\frac{e_n^2 + i_n^2\left(R_{seq}^2 + \left(R_f \parallel R_g\right)^2\right) + 4kTR_{seq} + 4kT\left(R_f \parallel R_g\right)}{4kTR_{seq}}\right)$$

Equation 2: Noise Figure Equation

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

- Minimize $R_f \parallel R_g$
- Choose the optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \cong \frac{e_n}{i_n}$$

Figure 2 is a plot of NF vs R_s with $R_f = 0$, $R_g = \infty$ ($A_v = +1$). The NF curves for both Unterminated and Terminated systems are shown. The Terminated curve assumes $R_s = R_T$. The table indicates the NF for various source resistances including $R_s = R_{OPT}$.

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC440 (CLC730055-DIP, CLC730060-SOIC) and suggests their use as a guide for high frequency layout and as an aid in device testing and characterization.

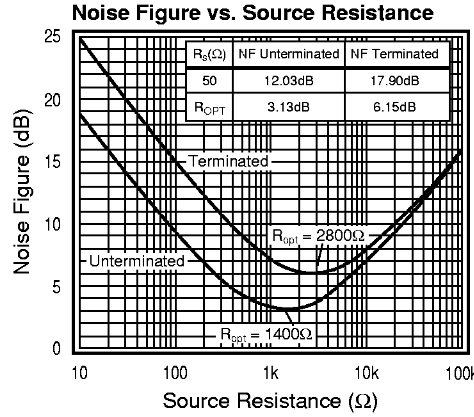


Figure 2: Noise Figure vs. Source Resistance

These boards were laid out for optimum, high-speed performance. The ground plane was removed near the input and output pins to reduce parasitic capacitance. And all trace lengths were minimized to reduce series inductances.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. 6.8µF tantalum, 0.01µF ceramic, and 500pF ceramic capacitors are recommended on both supplies. Place the 6.8µF capacitors within 0.75 inches of the power pins, and the 0.01µF and 500pF capacitors less than 0.1 inches from the power pins.

Dip sockets add parasitic capacitance and inductance which can cause peaking in the frequency response and overshoot in the time domain response. If sockets are necessary, flush-mount socket pins are recommended. The device holes in the 730055 evaluation board are sized for Cambion P/N 450-2598 socket pins, or their functional equivalent.

Applications Circuits

Transimpedance Amplifier

The low 2.5pA/√Hz input current noise and unity gain stability make the CLC440 an excellent choice for transimpedance applications. Figure 3 illustrates a low noise transimpedance amplifier that is commonly implemented with photo diodes. R_f sets the transimpedance gain. The photo diode current multiplied by R_f determines the output voltage.

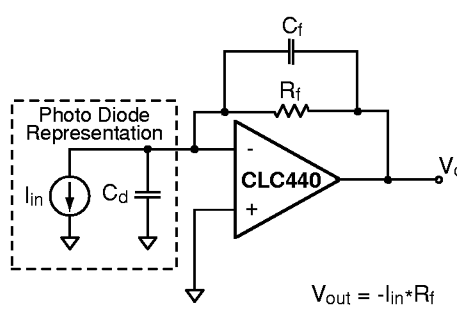


Figure 3: Transimpedance Amplifier Configuration

The capacitances are defined as:

- C_{in} = Internal Input Capacitance of the CLC440 (typ 1.2pF)
- C_d = Equivalent Diode Capacitance
- C_f = Feedback Capacitance

The transimpedance plot in the typical performance section provides the recommended C_f and expected bandwidth for different gains and diode capacitances. The feedback capacitances indicated on the plot give optimum gain flatness and stability. If a smaller capacitance is used, then peaking will occur. The frequency response shown in Figure 4 illustrates the influence of the feedback capacitance on gain flatness.

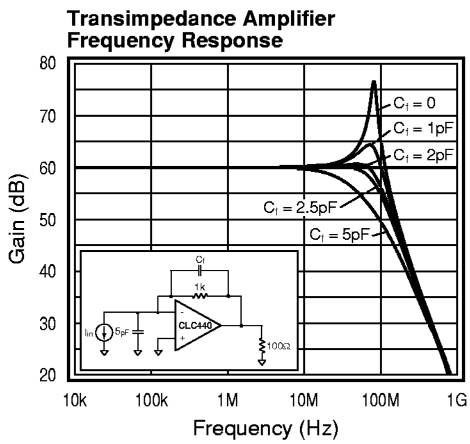


Figure 4

The total input current noise density (i_{ni}) for the basic transimpedance configuration is shown in Equation 3. The plot of current noise density versus feedback resistance is shown in Figure 5.

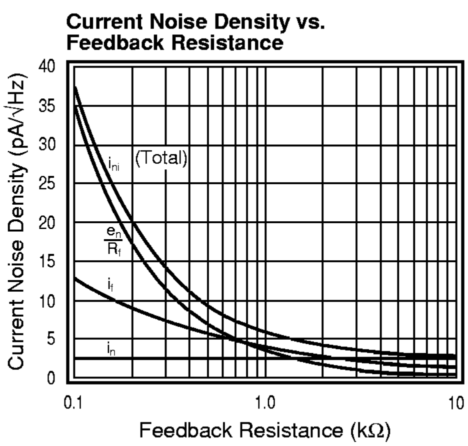


Figure 5

$$i_{ni} = \sqrt{i_n + \left(\frac{e_n 2}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 3: Total Equivalent Input Referred Current Noise Density

Rectifier

The large bandwidth of the CLC440 allows for high speed rectification. A common rectifier topology is shown in Figure 6. R_1 and R_2 set the gain of the rectifier. V_{out} for a 5MHz, $2V_{pp}$ sinusoidal input is shown in Figure 7.

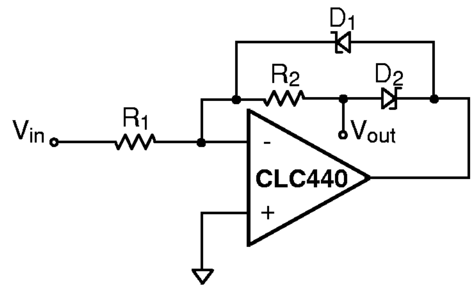


Figure 6: Rectifier Topology

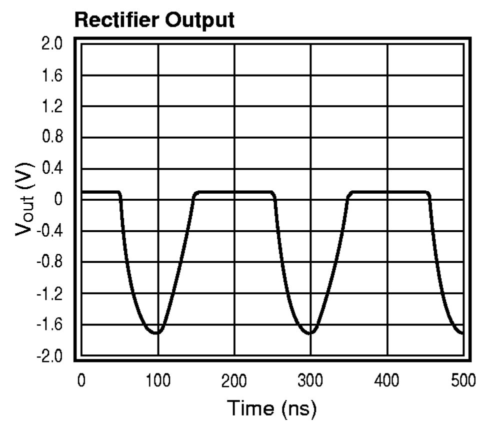
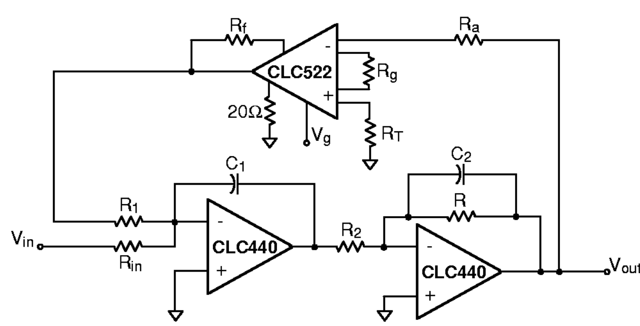


Figure 7: Rectifier Output

Tunable Low Pass Filter

The center frequency of the low pass filter (LPF) can be adjusted by varying the CLC522 gain control voltage, V_g.



$$\omega_o = \sqrt{\frac{k}{R_1R_2C_1C_2}} \quad Q = \sqrt{k}\left(\frac{RC_2}{\sqrt{R_1R_2C_1C_2}}\right) \quad R_g = \frac{V_{in\,(max)}}{1.8mA} \quad A_{v\,(max)} = k = 1.85\frac{R_f}{R_g}$$

Figure 8: Tunable Low Pass Filter

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1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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