

54LS161A/DM54LS161A/DM74LS161A, 54LS163A/DM54LS163A/DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional

gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

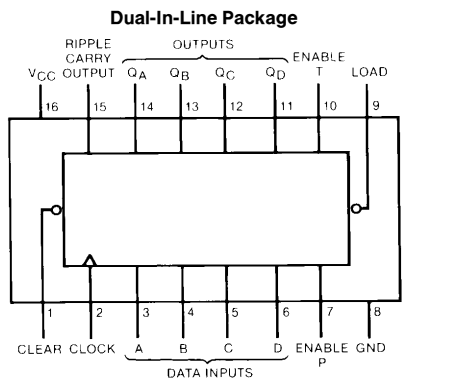
These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW
- Alternate Military/Aerospace device (54LS161, 54LS163) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



**Order Numbers 54LS161ADMQB, 54LS161AFMQB,
54LS161ALMQB, 54LS163ADMQB, 54LS163AFMQB,
54LS163ALMQB, DM54LS161AJ, DM54LS161AW,
DM54LS163AJ, DM54LS163AW, DM74LS161AM,
DM74LS161AN, DM74LS163AM or DM74LS163AN**
See NS Package Number E20A, J16A,
M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| DM54LS and 54LS | −55°C to +125°C |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | | DM54LS161A | | | DM74LS161A | | | Units |
|------------------|--------------------------------|----------|------------|-----|------|------------|-----|------|-------|
| | | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High Level Input Voltage | | 2 | | | 2 | | | V |
| V _{IL} | Low Level Input Voltage | | | | 0.7 | | | 0.8 | V |
| I _{OH} | High Level Output Current | | | | −0.4 | | | −0.4 | mA |
| I _{OL} | Low Level Output Current | | | | 4 | | | 8 | mA |
| f _{CLK} | Clock Frequency (Note 1) | | 0 | | 25 | 0 | | 25 | MHz |
| | Clock Frequency (Note 2) | | 0 | | 20 | 0 | | 20 | MHz |
| t _w | Pulse Width (Note 1) | Clock | 20 | 6 | | 20 | 6 | | ns |
| | | Clear | 20 | 9 | | 20 | 9 | | |
| | Pulse Width (Note 2) | Clock | 25 | | | 25 | | | ns |
| | | Clear | 25 | | | 25 | | | |
| t _{SU} | Setup Time (Note 1) | Data | 20 | 8 | | 20 | 8 | | ns |
| | | Enable P | 25 | 17 | | 25 | 17 | | |
| | | Load | 25 | 15 | | 25 | 15 | | |
| | Setup Time (Note 2) | Data | 20 | | | 20 | | | ns |
| | | Enable P | 30 | | | 30 | | | |
| | | Load | 30 | | | 30 | | | |
| t _H | Hold Time (Note 1) | Data | 0 | −3 | | 0 | −3 | | ns |
| | | Others | 0 | −3 | | 0 | −3 | | |
| | Hold Time (Note 2) | Data | 5 | | | 5 | | | ns |
| | | Others | 5 | | | 5 | | | |
| t _{REL} | Clear Release Time (Note 1) | | 20 | | | 20 | | | ns |
| | Clear Release Time (Note 2) | | 25 | | | 25 | | | ns |
| T _A | Free Air Operating Temperature | | −55 | | 125 | 0 | | 70 | °C |

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

'LS161 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units | |
|------------------|-----------------------------------|--|-------------------------------------|--------------|--------------|------------------------------|----|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | -1.5 | V | |
| V _{OH} | High Level Output Voltage | V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min | DM54 DM74 | 2.5 2.7 | 3.4 3.4 | V | |
| V _{OL} | Low Level Output Voltage | V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min | DM54 DM74 | | 0.25 0.35 | 0.4 0.5 | V |
| | | I _{OL} = 4 mA, V _{CC} = Min | DM74 | | 0.25 | 0.4 | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max V _I = 7V | Enable T Clock Load Others | | | 0.2 0.2 0.2 0.1 | mA |
| I _{IH} | High Level Input Current | V _{CC} = Max V _I = 2.7V | Enable T Clock Load Others | | | 40 40 40 20 | μA |
| I _{IL} | Low Level Input Current | V _{CC} = Max V _I = 0.4V | Enable T Clock Load Others | | | -0.8 -0.8 -0.8 -0.4 | mA |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 2) | DM54 DM74 | -20 -20 | | -100 -100 | mA |
| I _{CCH} | Supply Current with Outputs High | V _{CC} = Max (Note 3) | | | 18 | 31 | mA |
| I _{CCL} | Supply Current with Outputs Low | V _{CC} = Max (Note 4) | | | 19 | 32 | mA |

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | R _L = 2 kΩ | | | | Units |
|------------------|--|-------------------------------|------------------------|-----|------------------------|-----|-------|
| | | | C _L = 15 pF | | C _L = 50 pF | | |
| | | | Min | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | | 25 | | 20 | | MHz |
| t _{PLH} | Propagation Delay Time Low to High Level Output | Clock to Ripple Carry | | 25 | | 30 | ns |
| t _{PHL} | Propagation Delay Time High to Low Level Output | Clock to Ripple Carry | | 30 | | 38 | ns |
| t _{PLH} | Propagation Delay Time Low to High Level Output | Clock to Any Q (Load High) | | 22 | | 27 | ns |
| t _{PHL} | Propagation Delay Time High to Low Level Output | Clock to Any Q (Load High) | | 27 | | 38 | ns |

'LS161 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load) (Continued)

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2\text{ k}\Omega$ | | | | Units |
|-----------|--|------------------------------|--------------------------|-----|----------------------|-----|-------|
| | | | $C_L = 15\text{ pF}$ | | $C_L = 50\text{ pF}$ | | |
| | | | Min | Max | Min | Max | |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Any Q (Load Low) | | 24 | | 30 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Any Q (Load Low) | | 27 | | 38 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Enable T to Ripple Carry | | 14 | | 27 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Enable T to Ripple Carry | | 15 | | 27 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clear to Any Q | | 28 | | 45 | ns |

Recommended Operating Conditions

| Symbol | Parameter | | DM54LS163A | | | DM74LS163A | | | Units |
|-----------|--------------------------------|----------|------------|-----|------|------------|-----|------|------------|
| | | | Min | Nom | Max | Min | Nom | Max | |
| V_{CC} | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High Level Input Voltage | | 2 | | | 2 | | | V |
| V_{IL} | Low Level Input Voltage | | | | 0.7 | | | 0.8 | V |
| I_{OH} | High Level Output Current | | | | -0.4 | | | -0.4 | mA |
| I_{OL} | Low Level Output Current | | | | 4 | | | 8 | mA |
| f_{CLK} | Clock Frequency (Note 1) | | 0 | | 25 | 0 | | 25 | MHz |
| | Clock Frequency (Note 2) | | 0 | | 20 | 0 | | 20 | MHz |
| t_W | Pulse Width (Note 1) | Clock | 20 | 6 | | 20 | 6 | | ns |
| | | Clear | 20 | 9 | | 20 | 9 | | |
| | Pulse Width (Note 2) | Clock | 25 | | | 25 | | | ns |
| | | Clear | 25 | | | 25 | | | |
| t_{SU} | Setup Time (Note 1) | Data | 20 | 8 | | 20 | 8 | | ns |
| | | Enable P | 25 | 17 | | 25 | 17 | | |
| | | Load | 25 | 15 | | 25 | 15 | | |
| | Setup Time (Note 2) | Data | 20 | | | 20 | | | ns |
| | | Enable P | 30 | | | 30 | | | |
| | | Load | 30 | | | 30 | | | |
| t_H | Hold Time (Note 1) | Data | 0 | -3 | | 0 | -3 | | ns |
| | | Others | 0 | -3 | | 0 | -3 | | |
| | Hold Time (Note 2) | Data | 5 | | | 5 | | | ns |
| | | Others | 5 | | | 5 | | | |
| t_{REL} | Clear Release Time (Note 1) | | 20 | | | 20 | | | ns |
| | Clear Release Time (Note 2) | | 25 | | | 25 | | | ns |
| T_A | Free Air Operating Temperature | | -55 | | 125 | 0 | | 70 | $^\circ C$ |

Note 1: $C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, $T_A = 25^\circ C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50\text{ pF}$, $R_L = 2\text{ k}\Omega$, $T_A = 25^\circ C$ and $V_{CC} = 5V$.

'LS163 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
|-----------|-----------------------------------|--|--|--------------|------|---------------|
| V_I | Input Clamp Voltage | $V_{CC} = \text{Min}, I_I = -18 \text{ mA}$ | | | -1.5 | V |
| V_{OH} | High Level Output Voltage | $V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$ | DM54 | 2.5 | 3.4 | V |
| | | | DM74 | 2.7 | 3.4 | |
| V_{OL} | Low Level Output Voltage | $V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$ | DM54 | | 0.25 | V |
| | | | DM74 | | 0.35 | |
| | | | $I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$ | DM74 | | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}$ $V_I = 7V$ | Enable T | | 0.2 | mA |
| | | | Clock, Clear | | 0.2 | |
| | | | Load | | 0.2 | |
| | | | Others | | 0.1 | |
| I_{IH} | High Level Input Current | $V_{CC} = \text{Max}$ $V_I = 2.7V$ | Enable T | | 40 | μA |
| | | | Load | | 40 | |
| | | | Clock, Clear | | 40 | |
| | | | Others | | 20 | |
| I_{IL} | Low Level Input Current | $V_{CC} = \text{Max}$ $V_I = 0.4V$ | Enable T | | -0.8 | mA |
| | | | Clock, Clear | | -0.8 | |
| | | | Load | | -0.8 | |
| | | | Others | | -0.4 | |
| I_{OS} | Short Circuit Output Current | $V_{CC} = \text{Max}$ (Note 2) | DM54 | -20 | -100 | mA |
| | | | DM74 | -20 | -100 | |
| I_{CCH} | Supply Current with Outputs High | $V_{CC} = \text{Max}$ (Note 3) | | 18 | 31 | mA |
| I_{CCL} | Supply Current with Outputs Low | $V_{CC} = \text{Max}$ (Note 4) | | 18 | 32 | mA |

Note 1: All typicals are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS163 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2 \text{ k}\Omega$ | | | | Units |
|-----------|--|-------------------------------|---------------------------|-----|-----------------------|-----|-------|
| | | | $C_L = 15 \text{ pF}$ | | $C_L = 50 \text{ pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum Clock Frequency | | 25 | | 20 | | MHz |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Ripple Carry | | 25 | | 30 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Ripple Carry | | 30 | | 38 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Any Q (Load High) | | 22 | | 27 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Any Q (Load High) | | 27 | | 38 | ns |

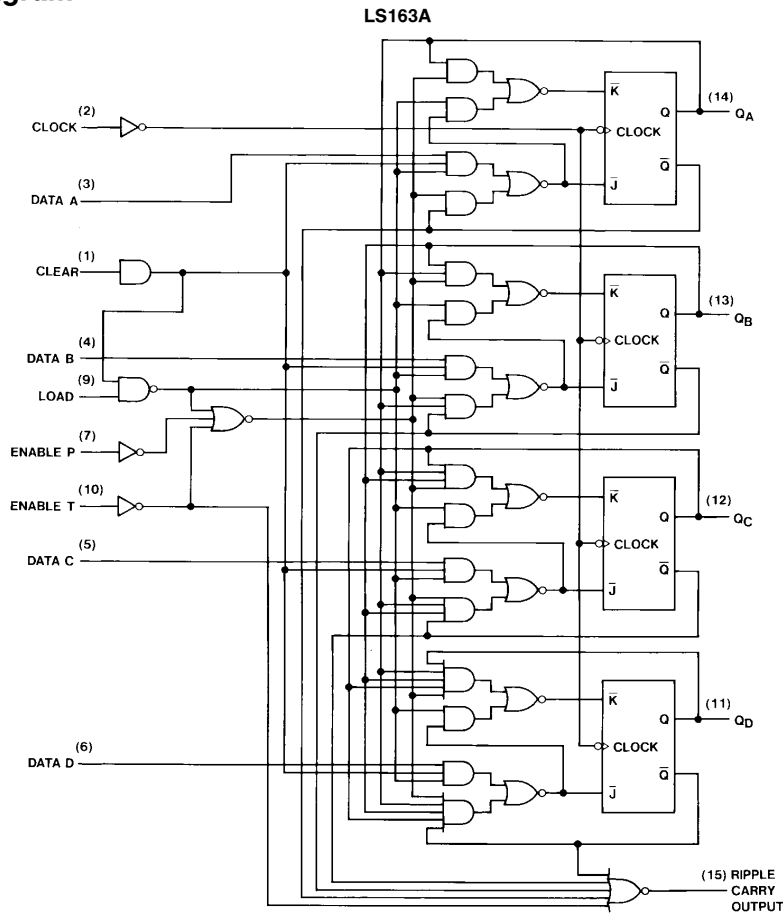
'LS163 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load) (Continued)

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2\text{ k}\Omega$ | | | | Units |
|-----------|--|------------------------------|--------------------------|-----|----------------------|-----|-------|
| | | | $C_L = 15\text{ pF}$ | | $C_L = 50\text{ pF}$ | | |
| | | | Min | Max | Min | Max | |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Any Q (Load Low) | | 24 | | 30 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Any Q (Load Low) | | 27 | | 38 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Enable T to Ripple Carry | | 14 | | 27 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Enable T to Ripple Carry | | 15 | | 27 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clear to Any Q (Note 1) | | 28 | | 45 | ns |

Note 1: The propagation delay clear to output is measured from the clock input transition.

Logic Diagram

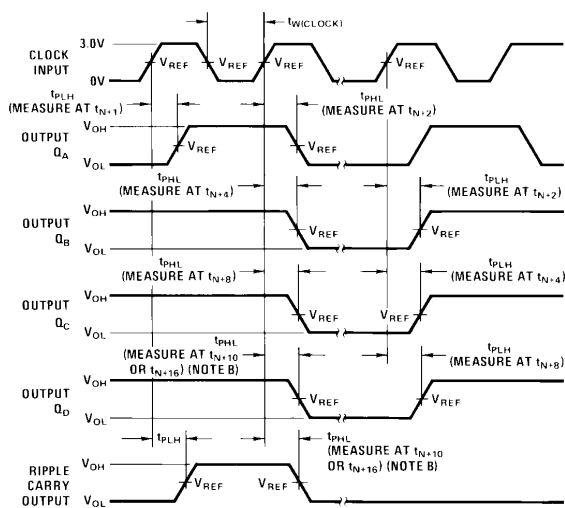


TL/F/6397-2

The LS161A is similar, however, the clear buffer is connected directly to the flip flops.

Parameter Measurement Information

Switching Time Waveforms



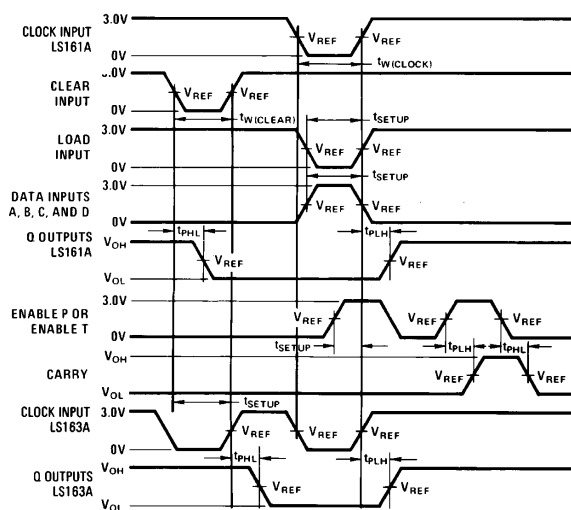
TL/F/6397-3

Note A: The input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX} .

Note B: Outputs QD and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms



TL/F/6397-4

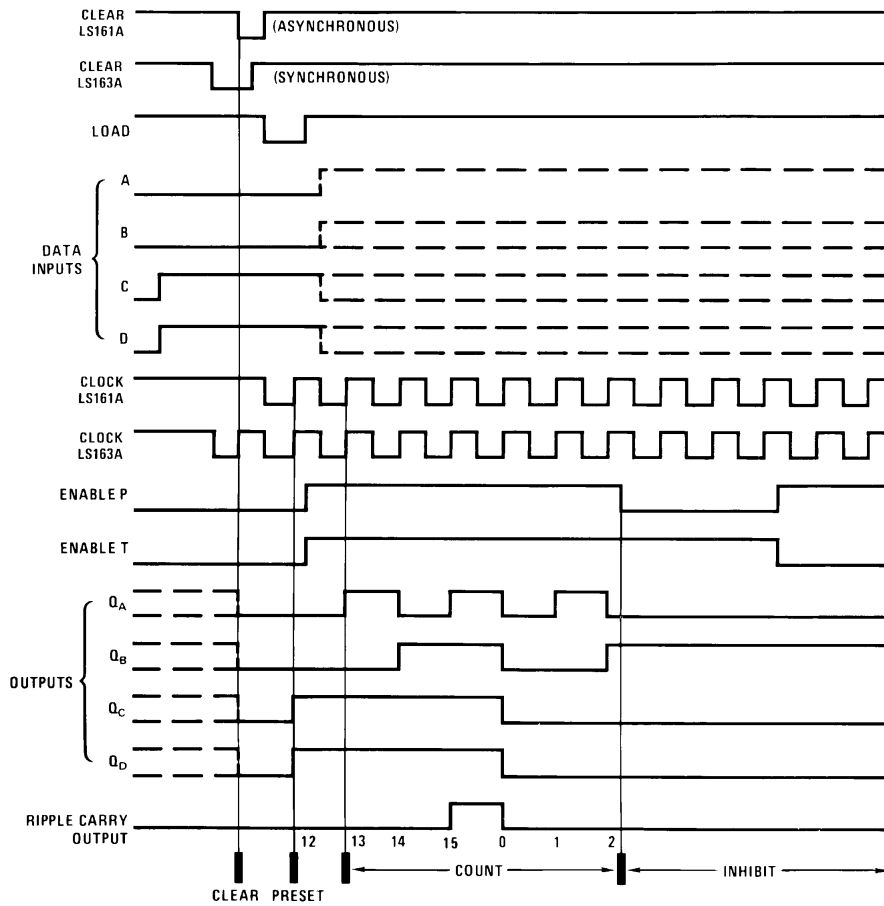
Note A: The input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX} .

Note B: Enable P and enable T setup times are measured at t_{n+0} .

Note C: $V_{REF} = 1.3V$.

Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences

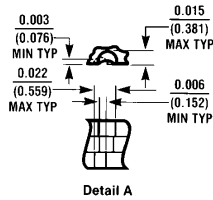
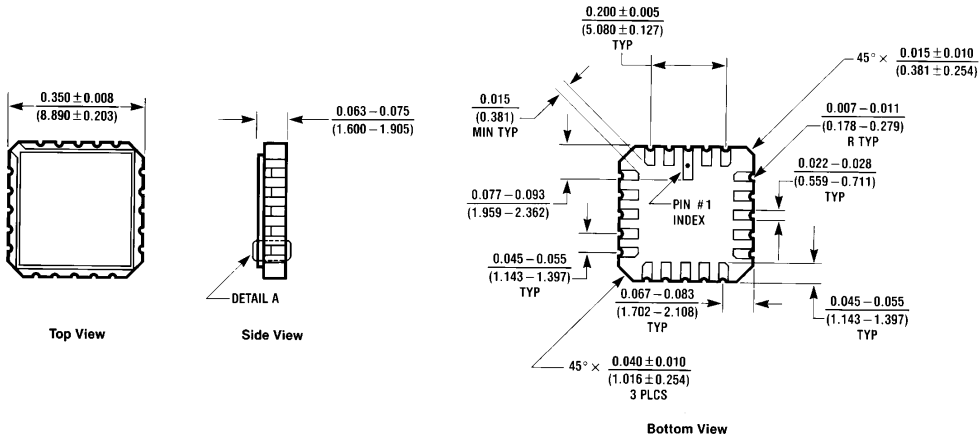


TL/F/6397-5

Sequence:

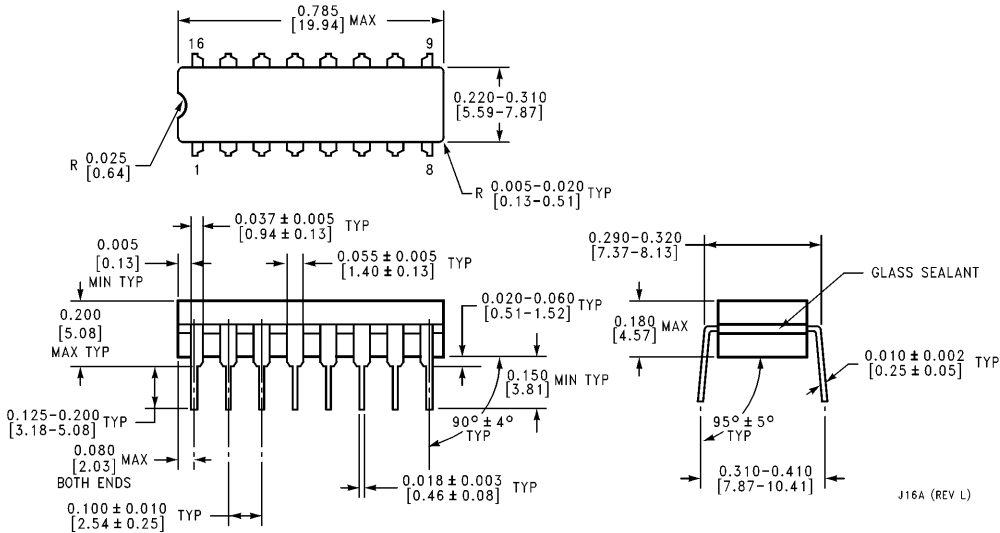
- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one, and two
- (4) Inhibit

Physical Dimensions inches (millimeters)



E20A (REV D)

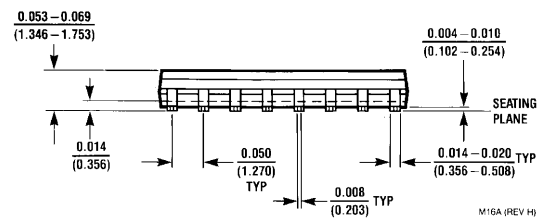
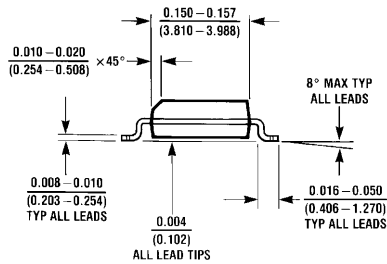
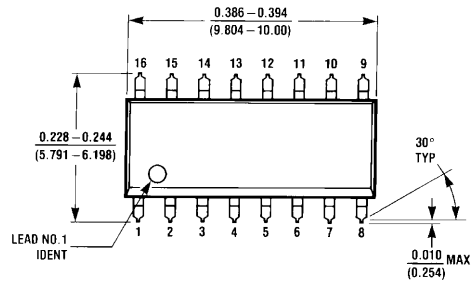
Ceramic Leadless Chip Carrier Package (E)
Order Numbers 54LS161ALMQB or 54LS163ALMQB
NS Package Number E20A



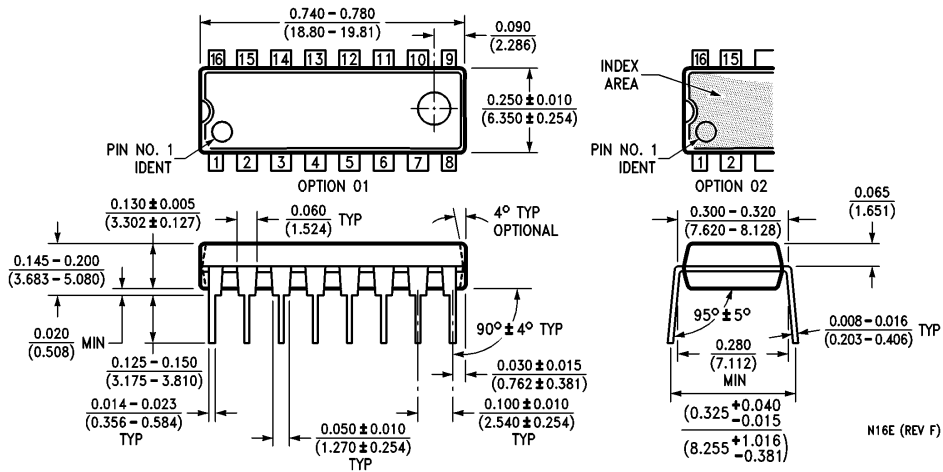
J16A (REV L)

16-Lead Ceramic Dual-In-Line Package (J)
Order Numbers 54LS161ADMQB, 54LS163ADMQB, DM54LS161AJ or DM54LS163AJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

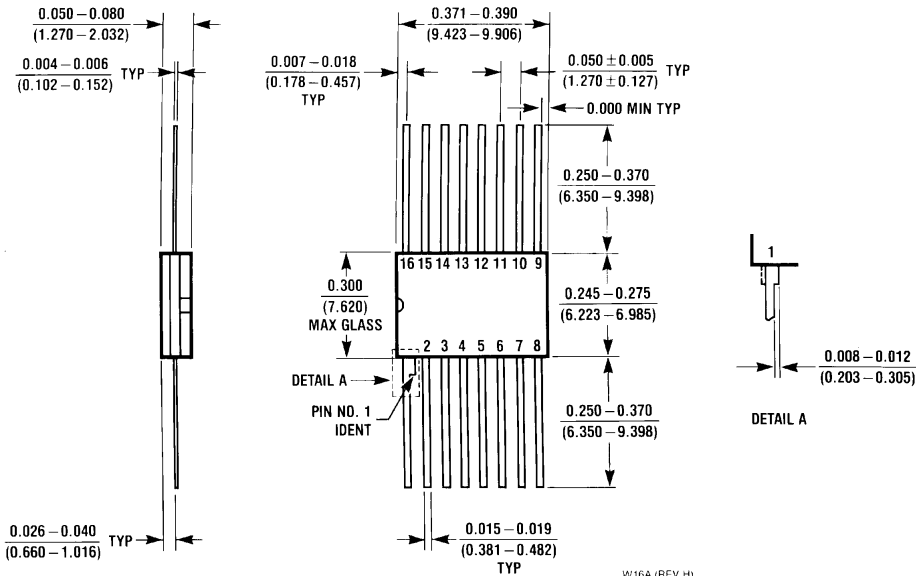


16-Lead Small Outline Molded Package (M)
Order Number DM74LS161AM or DM74LS163AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Numbers DM74LS161AN, DM74LS163AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Numbers 54LS161AFMQB, 54LS163AFMQB,
DM54LS161AN or DM54LS163AW
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: onjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.