T-46-07-11

National Semiconductor

74ACQ377 • 54ACTQ/74ACTQ377
Quiet Series Octal D Flip-Flop with Clock Enable

General Description

The 'ACQ/'ACTQ377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is low. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

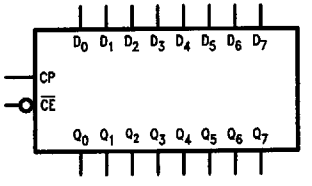
The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT377
- 4 kV minimum ESD immunity
- 'ACTQ has TTL-compatible inputs
- Standard Military Drawing (SMD)
  54ACTQ377: 5962-9219001

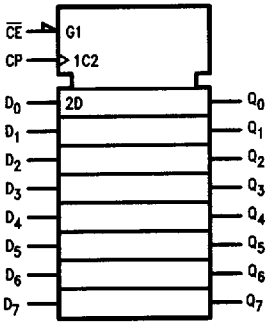
Ordering Code: See Section 8

Logic Symbols



TL/F/10151–1

IEEE/IEC

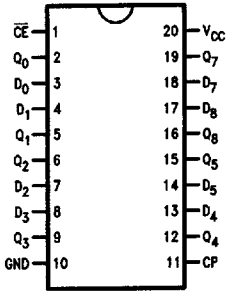


TL/F/10151–2

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

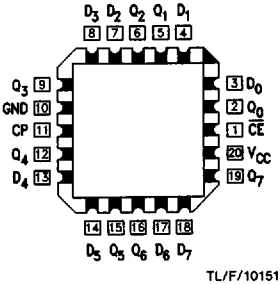
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10151–3

Pin Assignment for LCC



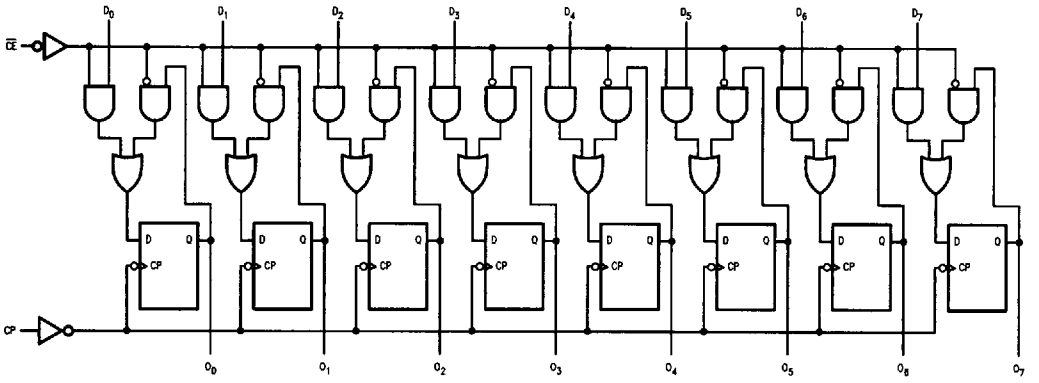
TL/F/10151–4

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	⌐‾	L	H	H
Load '0'	⌐‾	L	L	L
Hold (Do Nothing)	⌐‾	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐‾ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/10151–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables National does not recommend operation of FACT™ circuits outside databook specifications

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C	74ACQ T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.44		I_{OL} 24 mA
		5.5		0.36	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*All outputs loaded, thresholds on input associated with output under test

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data inputs (n) switching. (n−1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching. 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

5

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V_{IN} = V_{CC} or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). (n − 1) Data Inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	71 95			67 91		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.0 5.5	10.0 7.5	3.0 1.5	11.0 8.0	ns	2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to Q_n	3.3 5.0		1.0 0.5	1.5 1.0		1.5 1.0	ns	

*Voltage Range 5 0 is 5.0V ±0.5V
Voltage Range 3.3 is 3 3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same package device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design Not tested.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0		4.0 3.5	4.0 3.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0		0.0 1.5	0.0 1.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0		5.5 4.5	5.5 4.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0		0.0 1.5	0.0 1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	3.3 5.0		5.5 4.0	6.0 4.0	ns	2-4

*Voltage Range 5 0 is 5.0V ±0 5V
Voltage Range 3 3 is 3 3V ±0 3V

5

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	87			85		83		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to Q_n	5.0	2.0	6.0	8.0	1.5	10.0	1.5	8.5	ns	2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to Q_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0		3.5	4.0	3.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0		1.5	1.5	1.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	5.0		4.5	5.0	4.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	5.0		1.5	1.5	1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0		4.0	5.0	4.0	ns	2-4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V