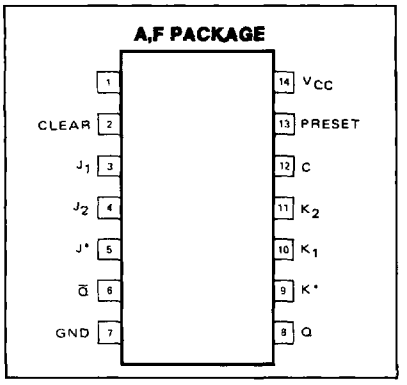
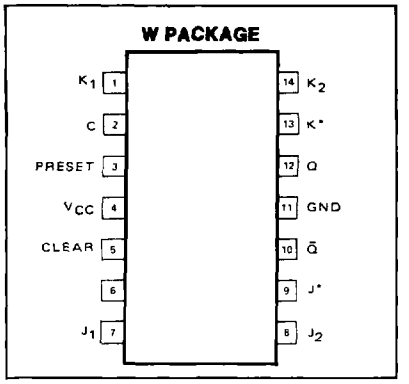
J-K FLIP-FLOP 54/7470

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

PIN CONFIGURATION





TRUTH TABLE

LOGIC

J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	0

$J = J_1J_2J^*$ $K = K_1K_2K^*$
n is time prior to clock
n+1 is time following clock
† both outputs in 0 state

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	35		MHz
t_{Setup}	Input setup time				10	20	ns
t_{Hold}	Input hold time				0	5	ns
	Propagation delay time						
t_{PLH}	Low-to-high	Clear, Preset				50	ns
t_{PHL}	High-to-low					50	
t_{PLH}	Low-to-high	Clock		10	27	50	ns
t_{PHL}	High-to-low			10	18	50	

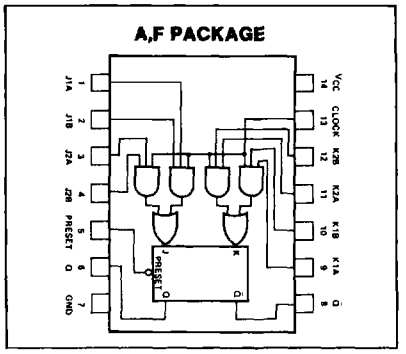
Load circuit and typical waveforms are shown at the front of section.

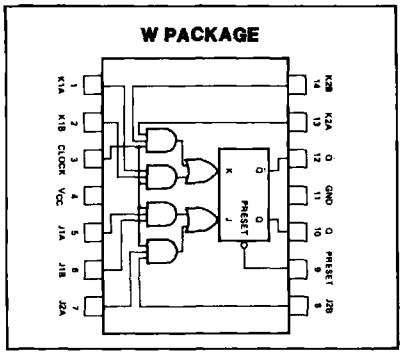
J-K MASTER-SLAVE FLIP-FLOP 54/7471

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

PIN CONFIGURATION





TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. J = (J1A•J1B)+ (J2A•J2B)
2. K = (K1A•K1B) + (K2A•K2B)
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	30		MHz
Propagation delay time							
t_{PLH}	Low-to-high	Preset			6	13	ns
t_{PHL}	High-to-low				12	24	
t_{PLH}	Low-to-high	Clock		6	14	21	ns
t_{PHL}	High-to-low			10	22	27	

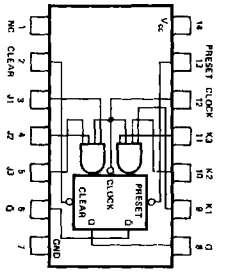
Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

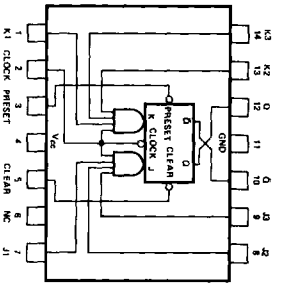
54	F,W	74	A,F
54H	F,W	74H	A,F

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.
5. NC = no internal connection.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	20		25	30		MHz
$t_{w(Clock)}$	Width of clock input pulse									
	Clock high			20			12			ns
	Clock low			47			28			
$t_{w(Clear)}$	Width of clear input pulse			25			16			ns
t_{Setup}	Input setup time			0↑			0↑			ns
t_{Hold}	Input hold time			0↓			0↓			ns
Propagation delay time										
t_{PLH}	Low-to-high	Clear			16	25		6	13	ns
t_{PHL}	High-to-low				25	40		12	24	
t_{PLH}	Low-to-high	Clock		10	16	25		16	21	ns
t_{PHL}	High-to-low			10	25	40		22	27	

Load circuit and typical waveforms are shown at the front of section.