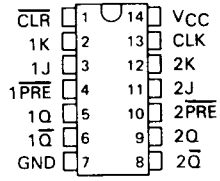
TYPES SN54ALS114A, SN54AS114, SN74ALS114A, SN74AS114
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2661, APRIL 1982—REVISED DECEMBER 1983

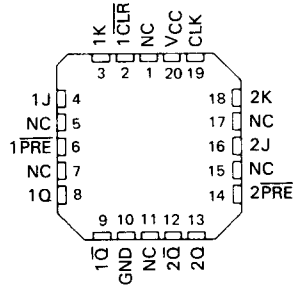
- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS114A	40 MHz (C_L = 15 pF)	6 mW
'AS114	175 MHz (C_L = 50 pF)	95 mW

SN54ALS114A, SN54AS114 . . . J PACKAGE
SN74ALS114A, SN74AS114 . . . N PACKAGE
(TOP VIEW)



SN54ALS114A, SN54AS114 . . . FH PACKAGE
SN74ALS114A, SN74AS114 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

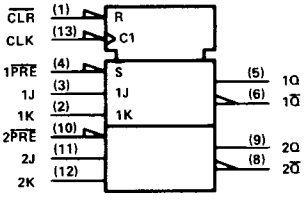
The SN54ALS114A and SN54AS114 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS114A and SN74AS114 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS114A, SN54AS114 . . . . . −55°C to 125°C
SN74ALS114A, SN74AS114 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS114A			SN74ALS114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteistics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS114A			SN74ALS114A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4				V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS114A		SN74ALS114A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	20	3	15	ns
t_{PHL}			4	22	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	18	3	15	ns
t_{PHL}			5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

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recommended operating conditions

			SN54AS114			SN74AS114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS114			SN74AS114			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$					0.5			0.5	
	$\overline{CLR}$					1			1	
	CLK					1			1	
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V			0.02			0.02	mA
	$\overline{PRE}$					0.1			0.1	
	$\overline{CLR}$					0.2			0.2	
	CLK					0.2			0.2	
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V		−1			−1		mA
	$\overline{PRE}$				−5.5			−5.5		
	$\overline{CLR}$				−11.5			−11.5		
	CLK				−10.5			−10.5		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK,and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS114			SN74AS114			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				175			175		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.