

## MM54C174/MM74C174 Hex D Flip-Flop

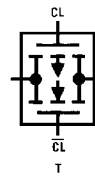
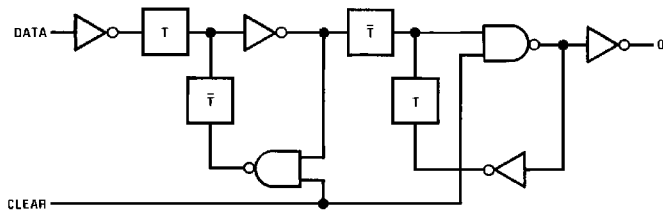
### General Description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to  $V_{CC}$  and GND.

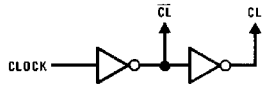
### Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45  $V_{CC}$  (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L

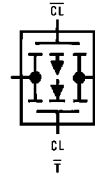
### Logic and Connection Diagrams



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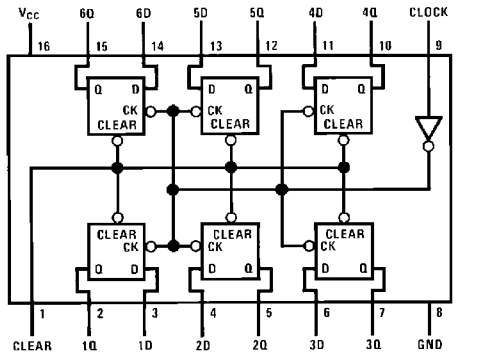


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TL/F/5899-3

### Dual-In-Line Package



TL/F/5899-4

### Top View

Order Number MM54C174 or MM74C174

### Truth Table

Clear	Inputs		Output
	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-55°C to +125°C
MM54C174	-40°C to +85°C
MM74C174	

Storage Temperature Range	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating $V_{CC}$ Range	3.0V to 15V
Absolute Maximum $V_{CC}$	18V
Lead Temperature (Soldering, 10 sec.)	260°C

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$	4.5			V
		$V_{CC} = 10V, I_O = -10 \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_O = 10 \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	300	$\mu A$
<b>CMOS/LPTTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360 \mu A$	2.4			V
		74C, $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360 \mu A$			0.4	V
		74C, $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)</b>						
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 5V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-1.75	-3.3		mA
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 10V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-8.0	-15		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5V$ $T_A = 25^\circ C, V_{OUT} = 0V$	1.75	3.6		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5V$ $T_A = 25^\circ C, V_{OUT} = 0V$	8.0	16		mA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd}$	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		150 70	300 110	ns ns
$t_{pd}$	Propagation Delay Time to a Logical "0" from Clear	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		110 50	300 110	ns ns
$t_{S1}$ , $t_{S0}$	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	75 25			ns ns
$t_{H1}$ , $t_{H0}$	Time after Clock Pulse that Data Must be Held	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	0 0	-10 -5.0		ns ns
$t_W$	Minimum Clock Pulse Width	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		50 35	250 100	ns ns
$t_W$	Minimum Clear Pulse Width	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		65 35	140 70	ns ns
$t_r$ , $t_f$	Maximum Clock Rise and Fall Time	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	15 5.0	>1200 >1200		$\mu\text{s}$ $\mu\text{s}$
$f_{MAX}$	Maximum Clock Frequency	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	2.0 5.0	6.5 12		MHz MHz
$C_{IN}$	Input Capacitance	Clear Input (Note 2) Any Other Input		11 5.0		pF pF
$C_{PD}$	Power Dissipation Capacitance	Per Package (Note 3)		95		pF

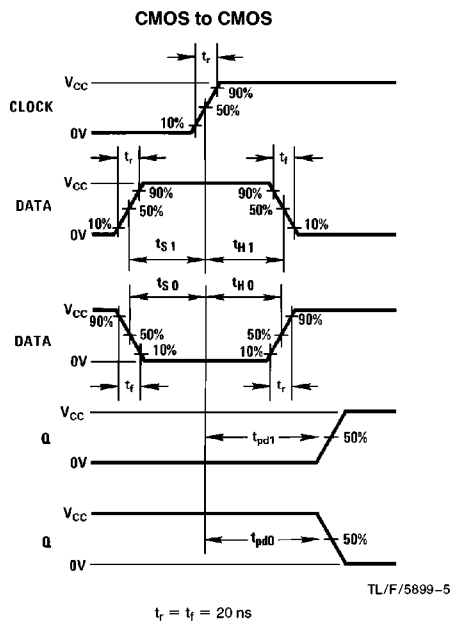
\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

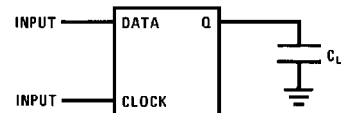
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

### Switching Time Waveforms

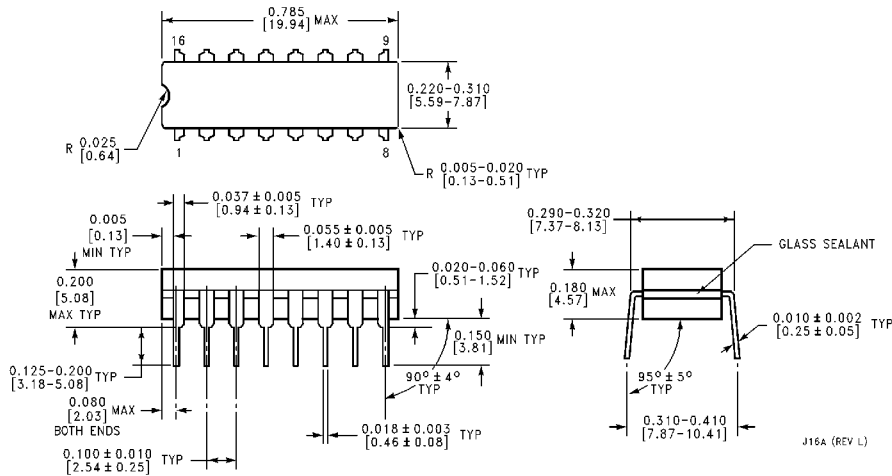


### AC Test Circuit

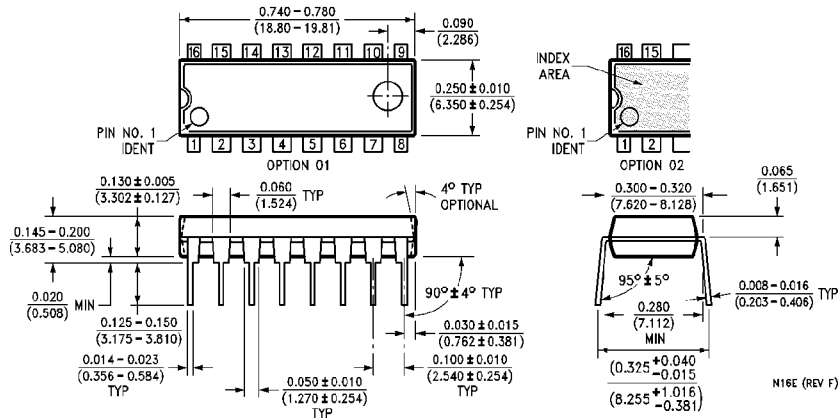


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**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54C174J or MM74C174J**  
**NS Package Number J16A**



**Molded Dual-In-Line Package (N)**  
**Order Number MM54C174N or MM74C174N**  
**NS Package Number N16E**

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