

SN74ALS109A, SN74AS109, SN54ALS109A, SN54AS109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

DZ661, APRIL 1982 - REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109A	50 MHz	6 mW
'AS109	129 MHz	29 mW

description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and trying J high. They also can perform as D-type flip-flops if J and K are tied together

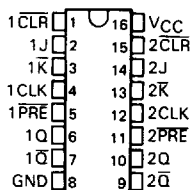
The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS109A and SN74AS109 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

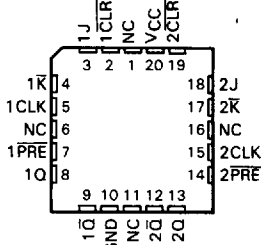
		INPUTS			OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	Q̄ ₀
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	Q̄ ₀

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable, that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS109A, SN54AS109 . . . J PACKAGE
SN74ALS109A, SN74AS109 . . . D OR N PACKAGE
(TOP VIEW)

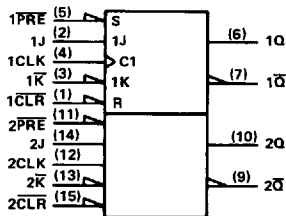


SN54ALS109A, SN54AS109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91 1984 and IEC Publication 617 12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS109A, SN54AS109	-55°C to 125°C
SN74ALS109A, SN74AS109	0°C to 70°C
Storage temperature range	-65°C to 150°C

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SN74ALS109A, SN54ALS109A

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

recommended operating conditions

		SN54ALS109A			SN74ALS109A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage	0.7			0.8			V	
I _{OH}	High-level output current	-0.4			-0.4			mA	
I _{OL}	Low-level output current	4			8			mA	
f _{clock}	Clock frequency	0	30		0	34		MHz	
t _w	Pulse duration	PRE or CLR low		15		15		ns	
		CLK high		16.5		14.5			
		CLK low		16.5		14.5			
t _{su}	Setup time before CLK↑	Data		15		15		ns	
		PRE or CLR inactive		10		10			
t _h	Hold time, data after CLK↑	0			0			ns	
T _A	Operating free-air temperature	-55		125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109A			SN74ALS109A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _J = -18 mA		-1.5			-1.5			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} -2			V _{CC} -2			V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 4 mA		0.25			0.25			V
		V _{CC} = 4.5 V, I _{OL} = 8 mA		0.4			0.4			
I _I	CLK, J, or K	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
	PRE or CLR			0.2			0.2			
I _{IH}	CLK, J, or K	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
	PRE or CLR			40			40			
I _{IL}	CLK, J or K	V _{CC} = 5.5 V, V _I = 0.4 V		-0.2			-0.2			mA
	PRE or CLR			-0.4			-0.4			
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		-30			-112			mA
I _{CC}		V _{CC} = 5.5 V, See Note 1		2.4			4			mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f _{max}			30		34	MHz	
t _{PLH}	PRE or CLR	Q or Q̄	3	17	3	13	ns
t _{PHL}			5	17	5	15	
t _{PLH}	CLK	Q or Q̄	5	21	5	16	ns
t _{PHL}			5	20	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1



SN74AS109, SN54AS109
DUAL J-K POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR AND PRESET

recommended operating conditions

		SN54AS109			SN74AS109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-2			-2	mA
I _{OL}	Low-level output current			20			20	mA
f _{clock}	Clock frequency	0		90	0		105	MHz
t _w	Pulse duration	PRE or CLR low		4			4	ns
		CLK high		4			4	
		CLK low		5.5			5.5	
t _{su}	Setup time before CLK †	Data		5.5			5.5	ns
		PRE or CLR inactive		2			2	
t _h	Hold time, data after CLK †			0			0	ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS109		SN74AS109		UNIT		
		MIN	TYP †	MAX	MIN		TYP †	MAX
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} - 2			V _{CC} - 2		V	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1		0.1	mA	
I _{IH}	CLK, J or K PRE or CLR	V _{CC} = 5.5 V, V _I = 2.7 V		20		20	μA	
				40		40		
I _{IL}	CLK, J or K PRE or CLR	V _{CC} = 5.5 V, V _I = 0.4 V		-0.5		0.5	mA	
				-1.8		-1.8		
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	V _{CC} = 5.5 V, See Note 1		11.5	17		11.5	17	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1 I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS109		SN74AS109		
			MIN	MAX	MIN	MAX	
f _{max}			90		105		MHz
t _{PLH}	PRE or CLR	Q or Q̄	3	9	3	8	ns
t _{PHL}			3.5	11.5	3.5	10.5	
t _{PLH}	CLK	Q or Q̄	3.5	10	3.5	9	ns
t _{PHL}			4.5	10.5	4.5	9	

NOTE 2 Load circuit and voltage waveforms are shown in Section 1

