- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (NT)

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)

| Pin		Pin	
1Y1	1	24	1$\overline{OE}$
1Y2	2	23	1A1
1Y3	3	22	1A2
1Y4	4	21	1A3
GND	5	20	1A4
GND	6	19	V_{CC}
GND	7	18	V_{CC}
GND	8	17	2A1
2Y1	9	16	2A2
2Y2	10	15	2A3
2Y3	11	14	2A4
2Y4	12	13	2$\overline{OE}$
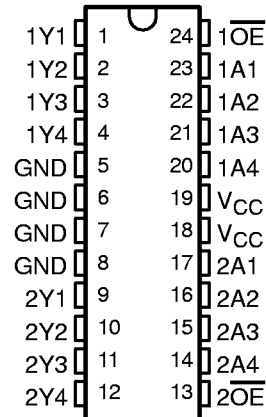
description

This octal buffer or line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'ACT11240, this device provides the choice of various combinations of inverting and noninverting outputs.

The 74ACT11244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

OUTPUT ENABLE $1\overline{OE}$, $2\overline{OE}$	DATA INPUT A	OUTPUT Y
H	X	Z
L	L	L
L	H	H

logic symbol†
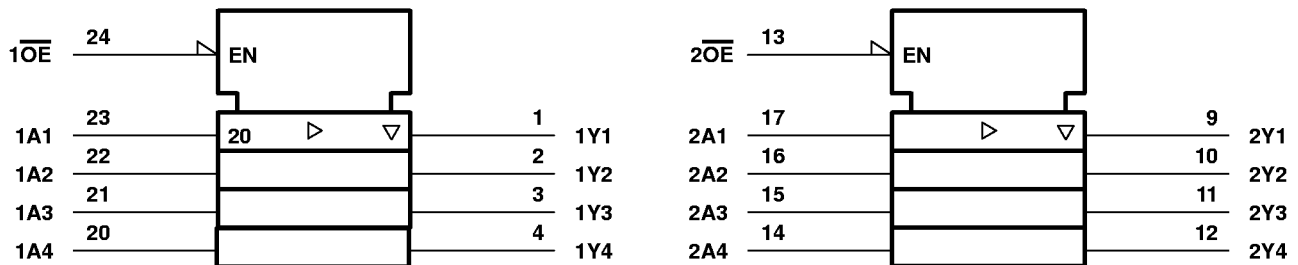
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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TEXAS INSTRUMENTS

logic diagram (positive logic)
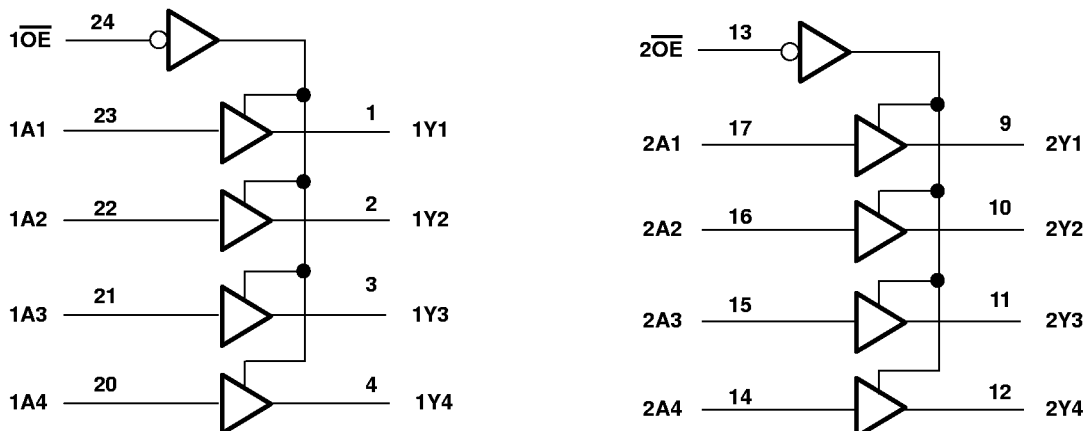
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6 V

Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V

Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA

Continuous current through V_{CC} or GND .... ±200 mA

Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package .... 0.65 W

DW package .... 1.7 W

NT package .... 1.3 W

PW package .... 0.7 W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu A$		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	$I_{OH} = -24$ mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	$I_{OH} = -75$ mA[†]		5.5 V				3.85		
V_{OL}	$I_{OL} = 50 \mu A$		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	$I_{OL} = 24$ mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	$I_{OL} = 75$ mA[†]		5.5 V					1.65	
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V		±0.5			±5	μA
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1			±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V		8			80	μA
ΔI_{CC}[‡]	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V		0.9			1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4				pF
C_o	$V_O = V_{CC}$ or GND		5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5$ V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.5	6	8.9	1.5	9.9	ns
t_{PHL}			1.5	5.4	8.6	1.5	9.2	
t_{PZH}	$\overline{OE}$	Y	1.5	6.6	11.3	1.5	12.5	ns
t_{PZL}			1.5	6.7	10.5	1.5	11.4	
t_{PHZ}	$\overline{OE}$	Y	1.5	7.4	9.8	1.5	10.4	ns
t_{PLZ}			1.5	7.8	10.6	1.5	11.2	

operating characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	$C_L = 50$ pF,	f = 1 MHz	27	pF
		Outputs disabled			9	

PARAMETER MEASUREMENT INFORMATION
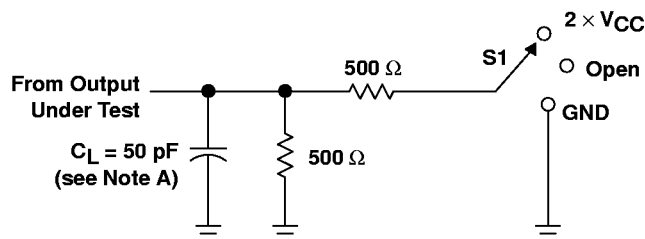
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
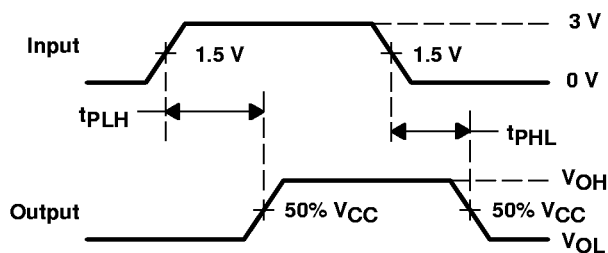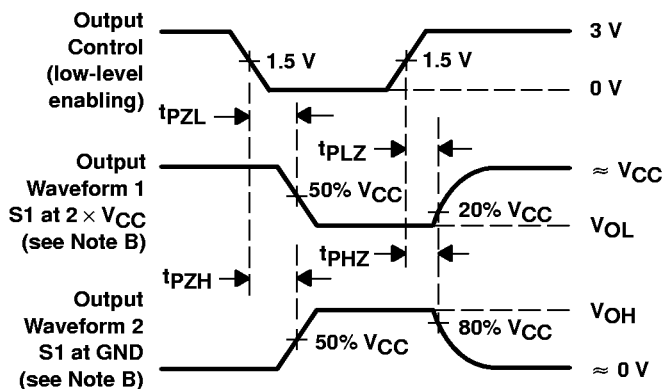
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \ \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms